Application Report
SLVA687–February 2014

TPS65083x Design Guide

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ABSTRACT

This document is meant to be used as a guide or check list for designers to ensure the proper design of the TPS65083x PMIC. It covers schematic, PCB layout, and some information on BOM selection. For controller and converter design please refer to the *Controller and Converter Design Calculations* application note.

Contents

List of Figures

List of Tables

1 TPS65083x Overview

TPS65083x has 4 controllers, 1 converter, and a termination LDO for DDR memories. In addition to these power rails, the PMIC has 8 comparators, 2 level shifters, 2 load switches, system level power goods, enables, interrupts and resets, 3 Power Path Comparators and Switch Controls, 2 temperature monitoring systems and I^2C communication.

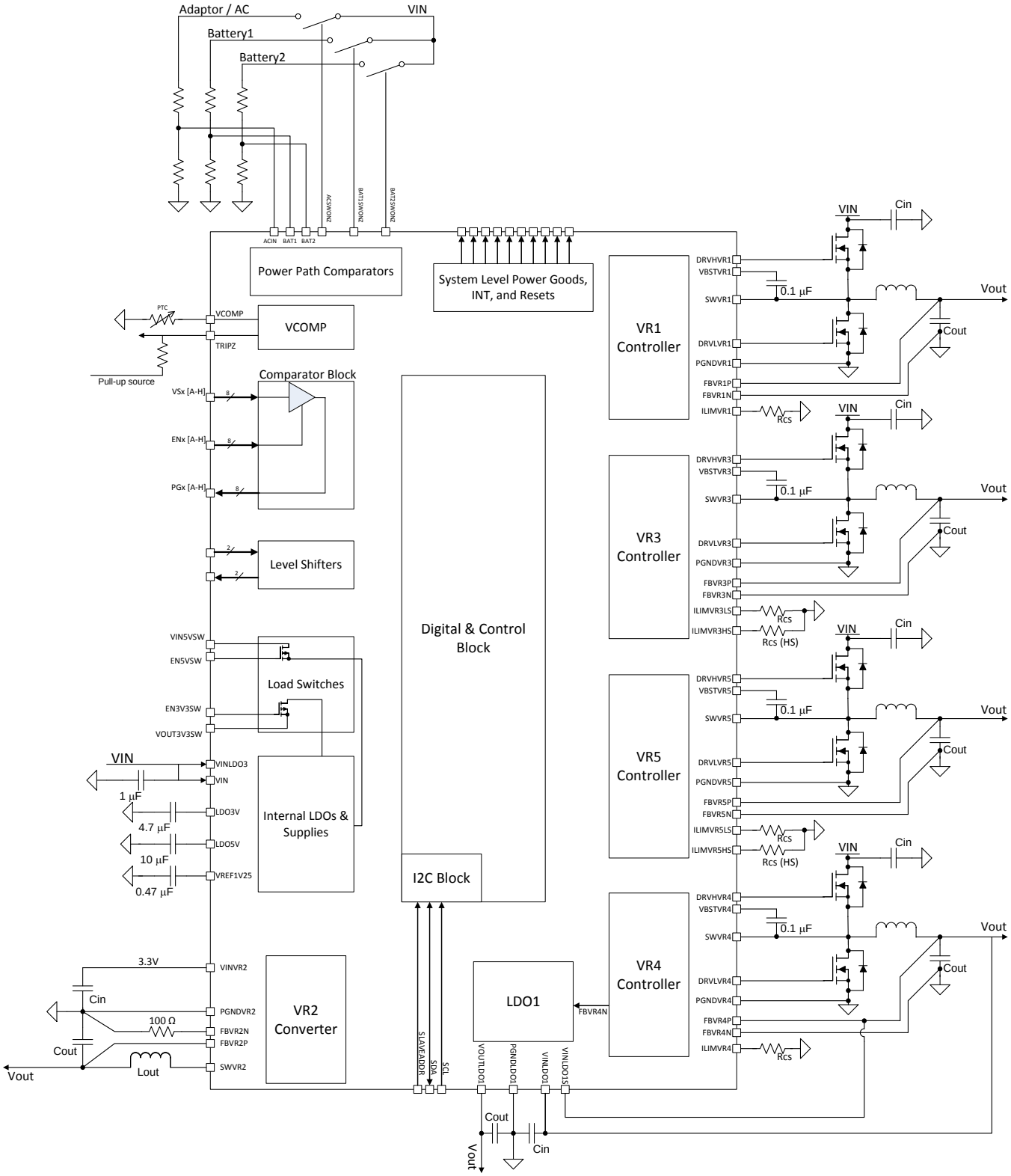

Figure 1. TPS65083x Application Drawing

1.1 VR and VTT Rails

All VRs require an input capacitor, output filter, and feedback connections. The controllers also require 2 power FETs, bootstrap capacitor and Rcs current limit resistor. The VTT LDO requires an input and output capacitors and feedback connection.

For information on how to design the VR power rails, refer to the application section of in the datasheet (SLVSCF4).

2 Schematic Check List

2.1 Bypass Capacitancors

There should be a ceramic X5R or X7R, ±20% bypass capacitor placed close to the respective input pins for input filtering. Be sure to account for the DC bias derating of the ceramic capacitors. Thus, the voltage rating should be approximately twice the max input voltage on the pin. Capacitors should connect to AGND or the common GND if there is no dedicated AGND.

Table 1. Bypass Capacitors

Pin	Supply Voltage	Capacitance
VIN	VBATA or VIN	1 µF
VINLDO3	VBATA or VIN	1 µF
VDDIO (1 capacitor for each pin)	LDO3V	1 µF
VINPP	See Section 2.9	1 µF
VDDPG	See Section 2.3	1 µF or greater
VDDLV	See Section 2.4	0.22 µF
VREGVR1	LDO5V	1 µF
VREGVR4	LDO5V	

2.2 Internal LDOs

There must be output capacitors placed on the outputs of the internal LDOs, LDO5V, LDO3V, VREF1V25 and V3P3A_RTC. Small X5R or X7R, ±20% ceramic capacitors ranging from 0.47 µF to 10 µF. Refer to Table 2 for capacitance values used on TI EVM and reference designs.

Table 2. Internal LDO Output Capacitors

LDO	Output Capacitance	Voltage Rating
LDO5V	10 µF	10 V
LDO3V	4.7 µF	10 V
VREF1V25	0.47 µF	6.3 V
V3P3A_RTC	1 µF	6.3 V

2.3 Power Good Comparators / External Voltage Rail Enablers

For the 8 comparators on the device, (A - H), the VSx signals can be configured as needed for the application in use. The corresponding ENx pin enables the comparating function on the VSx pin with the output logic HIGH or LOW on the corresponding PGx pin. The comparator voltage is configurable. The comparators may also be configured as general logic inputs. This configuration option can be used for power good inputs from other external power devices. The outputs may be configured as push-pull or open-drain outputs. The supply on the VDDPG sets the ENx and PGx, (if push-pull), logic VIH and VIL or VOH and VOL voltages. For a typical 3.3V voltage domain, the LDO3V is available as a supply.

If any of the comparators are not used then:

- VSx should be connected to GND
- ENx should be connected to GND
- PGx can be left floating

If none of the comparators are used then the VDDPG does not require a bypass capacitor. In this case, the LDO3V should be connected to the VDDPG.

Table 3 describes comparator voltage and output configurations for TPS650830, TPS650831, and TPS650832.

Table 3. Comparator Configurations

Comparator	TPS650830		TPS650831		TPS650832	
	Input Comparator Voltage	Output PGx Pin	Input Comparator Voltage	Output PGx Pin	Input Comparator Voltage	Output PGx Pin
A	3.3 V	PP	3.3 V	PP	3.3 V	PP
B	1.8 V	PP	1.8 V	PP	1.8 V	PP
C	-	-	5 V	PP	Logic Input	PP
D	1 V	PP	3.3 V	PP	Logic Input	PP
E	3.3 V	PP	3.3 V	PP	3.3 V	PP
F	1.8 V	PP	1.8 V	PP	1.8 V	PP
G	1 V	OD	1 V	OD	1 V	OD
H	-	-	-	-	-	-

2.4 Level Shifters

There are 2 level shifters on board available for use. The VDDLV is the supply for this domain.

TPS65083x has level shifter LVA programmed for BC_ACOK use, instead of level shifter. BC_ACOK is the output for LVA. A pull up to ECVCC is required because LVA is an open-drain in this configuration. LVB can be left floating and ENLVA should be shorted to ground.

If the level shifter is not used then ENLVA should be connected to GND and the LVA and LVB outputs can be left floating.

2.5 System Level Power Goods, Resets, Interupts and Enables

The device has power good tree integrated inside the PMIC that generates the system level power goods needed for the Intel Skylake system. Table 4 refers to the corresponding Skylake rails for each output signal. DS3_VREN is a push pull output.

Table 4. Pull Up Voltage

Signal	Voltage Rail in the Skylake System
DPWROK	V3.3A_DSW
RSMRST#_PWRGD	ECVCC
VCCST_PWRGD	V1.00S
ALL_SYS_PWRGD	V3.3S
SYS_PWROK	V3.3S
PCH_PWROK	V3.3S
EC_RST#	ECVCC
PCH_PWRBTN#	V3.3A_DSW
EC_ONOFF#	ECVCC
PMIC_INT#	ECVCC
DS3_VREN	Push Pull, no pull up required

If any of the signals are not used, the output can be left floating.

2.6 Load Switches

There are 2 load switches on the TPS65083x. Only the 3VSW is available for use in the system. The 5VSW is an overdrive for the LDO5V to increase the efficiency and reduce the Iq current of the device.

2.6.1 5VSW

The device has a 5 V overdrive load switch feature for reducing power loss on LDO5V. An 5 V SMPS, switch mode power supply, should be driving the VIN5VSW. The EN5VSW can be any logic enabling signal that goes HIGH after the VIN5VSW voltage is present and valid. The recommended configuration is to use the 5 V supply generated by VR5 and the PGVR5 as the enabling signal.

If 5VSW is not to be used then, EN5VSW should be connected to GND and VIN5VSW should be left floating.

2.6.2 3VSW

The 3VSW is available for use for any required 3.3 V load switch in the system. LDO3V is the source for the load switch. EN3VSW enables the load switch. The VOUT3VSW is the output.

If 3V3SW is not to be used then, EN3V3SW should be connected to GND and VOUT3V3SW should be left floating.

2.7 I^2C and SLAVEADDR

SLAVEADDR should be tied to either 3.3V, GND, or left floating. This selects the I2C slave address for the PMIC. I2C bus lines, SCL and SDA require pull up resistors. Any resistor between 1.5 kΩ and 10 kΩ is typically recommended however, bus capacitance does need to be accounted for. To calculate the pull up resistor needed use Equation 1

$$R_{P(max)} = t_r / 0.8473 \times C_b \quad (1)$$

where

- $R_{P(max)}$ is the maximum resistance need for the pull up resistor on SDA and/or SCL.
- t_r is the rise time required for the application's specific I2C clocking frequency.
- C_b is the total capacitance on the bus.

2.8 VBATTBKUP

If a back up battery is used to hold the RTC domain registers and supply for the RTC while the battery and adaptor are disconnected, there should be a resistor placed in series with the battery connection to protect the coin-cell battery from excessive discharge current. To calculate the resistor value use Equation 2

$$R_{MIN} = VBATTBKUP_{MAX} / I_{MAX} \quad (2)$$

where

- R_{MIN} is minimum required series resistance.
- $VBATTBKUP_{MAX}$ is the maximum voltage from the coin-cell battery.
- I_{MAX} is the maximum discharge current from the coin-cell battery. Should be available in the coin-cell datasheet.

If there is no backup battery to be used then, leave VBATTBKUP floating.

2.9 Power Path Comparators

ACIN, BAT1, and BAT2 if used need: a voltage divider from the respective VIN to divide the voltage down to the comparator threshold voltage of 1.25 V. A small ceramic 1 µF, X5R or X7R, ±20%, bypass capacitor placed close to the ACIN, BAT1, and BAT2 pins for input filtering. The ACOUT, BAT1OUT, and BAT2OUT outputs require a pull up resistor to the preferred voltage. A 100 kΩ resistor pull up works well.

Use Equation 3 and Figure 2to calculate the resistor divider needed for proper power path detection.

$$V_{DETECT} = V_{TH} \times (R_1 + R_2) / R_2 \quad (3)$$

where

- V_{TH} is the threshold voltage of the comparator, = 1.25 V.
- V_{DETECT} is the desired detect voltage of the power rail.

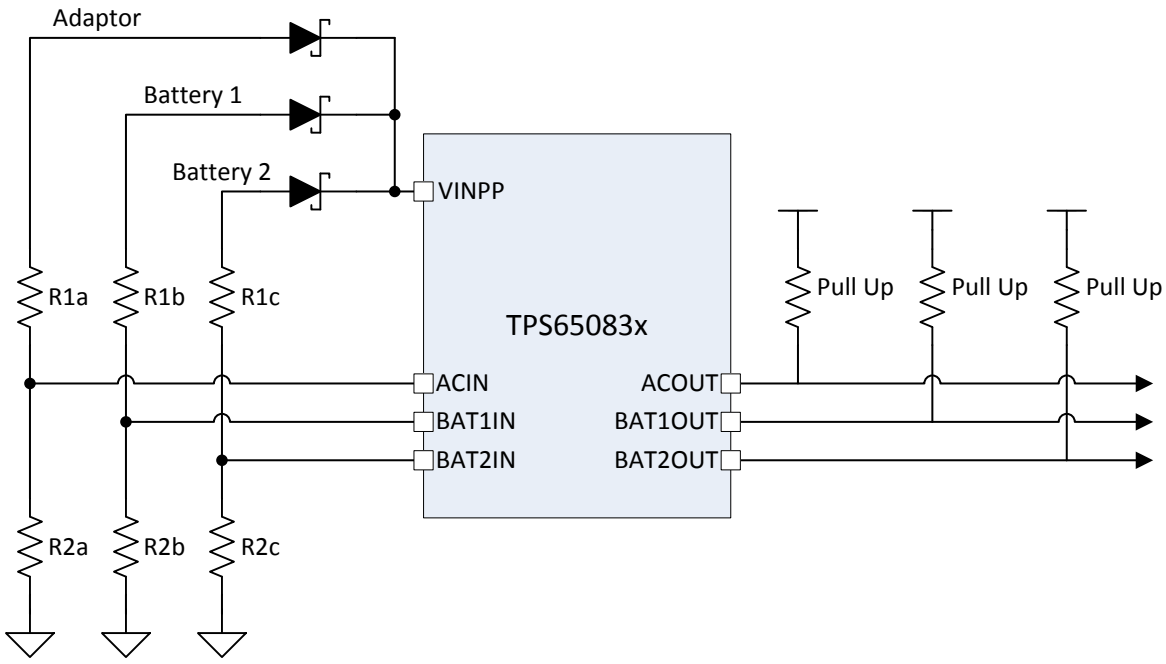

Figure 2. Voltage Divider Diagram

If any of these comparators are not used, the ACIN, BAT1, and BAT2 pins should be shorted to ground and the resistor dividers is not needed. The corresponding output pins, ACOUT, BAT1OUT, and BAT2OUT can be left floating.

2.9.1 VINPP

VINPP should be connected to the highest VIN to the PMIC, (adaptor, battery 1, or battery 2). Using schotkey diodes, the highest VIN can be passed to VINPP without back biasing the other VIN rails.

There should be a ceramic 1 µF, X5R or X7R, ±20%, bypass capacitor placed close to the VINPP pin for input filtering. Be sure to account for the DC bias derating of the ceramic capacitors. Thus, the voltage rating should be approximately twice the max input voltage on the pin. Capacitors should connect to AGND or the common GND if no AGND is used.

If none of the power path comparators are used then, VINPP should be left floating or tied to VIN. The bypass capacitor is not needed.

2.10 Temperature Monitoring System

The TPS65083x can monitor and alert the processor of a critical temperature on the PMIC's die or anywhere on the board. Use the VCOMP and TRIP# for system board temperature monitoring and the TEMP_ALERT# for the PMIC die temperature monitoring.

2.10.1 VCOMP and TRIP#

VCOMP and TRIP# monitor the board system temperature by using PTC thermistors in series and place in various spots on the board. The muRata PRF15BG102RB6RC PTC thermistor is recommended for the RTs.

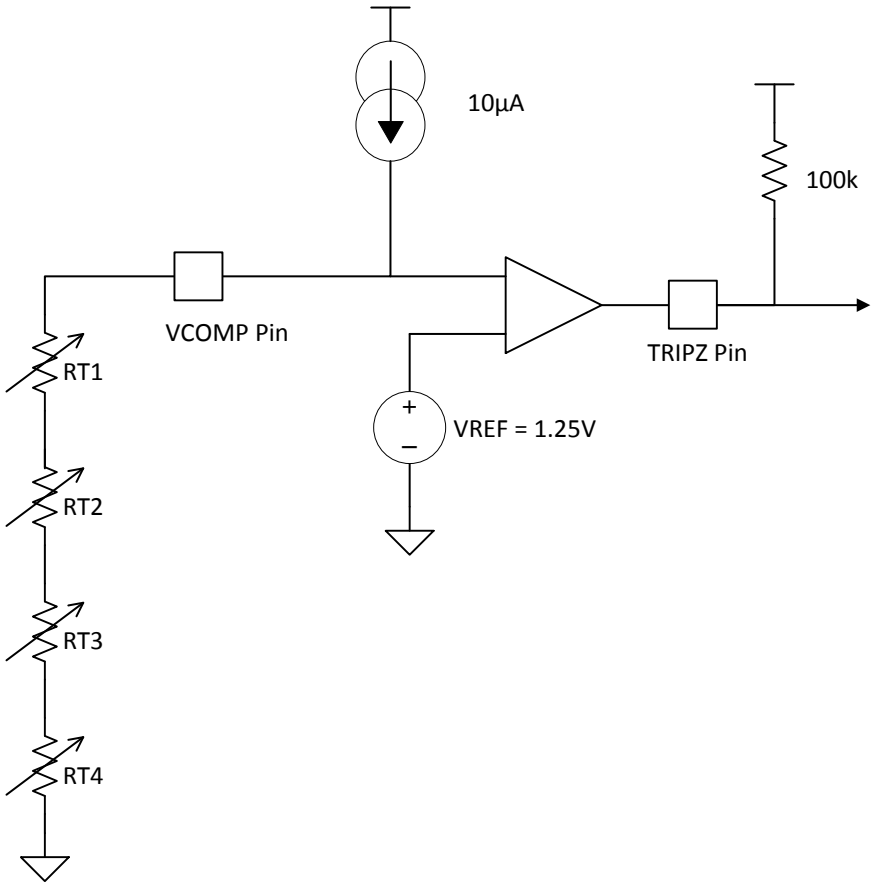

Figure 3. Board Temperature Monitoring Circuit

If this feature is not used then, VCOMP should be connected to GND and TRIPZ can be left floating.

2.10.2 TEMP_ALERT# / PROCHOT#

For the PROCHOT# application a 49.9 Ω resistor pull up from the 1 V rail must be used on the output of TEMP_ALERT#.

For any other application, this feature outputs an active low signal to warn the processor of an immediate shutdown due to the device's die temperature reach the critical temperature. In this case, the pull up resistor can any resistance as desired.

If TEMP_ALERT# is not used then, TEMP_ALERT# can be left floating.

2.11 ECVCC, PWRBTNIN#, ACOK, and VDCSENSE

ECVCC should be connected to the VCC rail of the EC, embedded controller. Connect to LDO3V if EC VCC rail is not applicable.

PWRBTIN# is active low and has an internal pull up resistor, eliminating the need for an external resistor. See schematic for orienation of the push button or if desired a GPIO can drive this signal from an external source. If not used, leave PWRBTNIN floating.

ACOK is a logic input that indicates that the adaptor is pulled in and available for power. If ACOK is not to be used then, connect the ACOK pin to LDO3V.

VDCSENSE, (VDCSNS), needs an external voltage divider to step done the VIN or VBATA voltage to the comparator threshold. It is recommended to use a 1 MΩ resistor as the pull up resistor and a 249 kΩ as the pull down resistor to form the voltage divider appropriate for the VDCSENSE comparator threshold. If VDCSENSE is not to be used then, connect the VDCSNS pin to LDO3V.

2.12 NVDC#

NVDC# selects the controller switching frequency and compensation to optimize the controllers for the VIN range being used for the application.

- NVDC# should be connected to ground if the system is a NVDC system with VIN ranging from 5.4 V to 13.5 V.
- NVDC# should be connected to LDO3V if the system is a non-NVDC system with VIN ranging from 5.4 V to 21 V.
- Never leave NVDC# pin floating.

2.13 SHUTDOWNZ and RESETZ

SHUTDOWNZ will place the device into the OFF mode via emergency reset sequence. Never leave floating either connect to LDO3V if unused or drive it with a logic signal.

RESETZ is an output to alert all other external coneverters that PMIC has shutdown. This can be ANDed with the enables of these external converters in order to shutdown the external converters with the PMIC. Leave floating if unused.

2.14 STANDBY#

Asserting this signal LOW puts the device into ULQ mode, reducing the Iq current of the device. Never leave floating either tie it HIGH, LOW or drive it with a logic signal.

For Intel Skylake applications connect to SLP_S0# signal.

2.15 VPROGOTP

VPROGOTP is used for TI internal purposes only. Connect to LDO5V.

3 PCB Layout Check List

- All inductors, input/output caps and FETs for the converters and controller should be on the same board layer as the IC.
- Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.
- Bootstrap capacitors must be place close to the IC from the SWVRx to VBSTVRx pins.
- DRVLVRx signals must be routed on the same layer as the IC and the FETs and minimize the length and parasitic inductance of the trace as much as possible.
- Each converter and controller should have their own separate ground and each ground should connect to the common ground separately. The input capacitors, output capacitors, and FET grounds for each VRx converter and controller must be connected to the ground plane for the respective VRx rail. Since, the PGNDs for each rail are not connect to each other or AGND, it is required to use the PGNDVRx pins for the input and ouput capacitors for each VRx rail. This ground plane should connect in one place to the common ground close to the input and output capacitor ground pads. See the figure below for a visual representation of the converter layout scheme.
- The internal reference regulators must have their input and output caps close to the IC pins.
- Route the FBVRxP and FBVRxN signals as a differential pair.

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