Level-Shifting Control for an Inverting Buck-Boost

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ABSTRACT

A level-shifting control circuit may be required in applications where the internal ground reference potential of the integrated circuit (IC) is not system ground. A level-shifting circuit is necessary to configure a buck converter in an inverting buck-boost topology. In this application, the IC ground reference is tied to the negative output voltage. The reference potential of external interfacing components must be level shifted to match the ground reference of the IC to stay within the voltage specifications of the signal pins of the IC. All external control circuitry connecting to the inverting buck-boost must be level shifted from the system ground to match the IC's ground reference. This application report demonstrates an inverting buck-boost design with the TPS54260 and level shifting of the enable (EN), external synchronization (RT/CLK), and power good (PWRGD) pins. The same general level-shifting concepts can be applied to other topologies or to other IC pins.

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1   Introduction

A level-shifting control circuit is used to translate the potential of interfacing control circuitry to match a different ground reference. The level shifter is particularly useful when designing an inverting buck-boost generating a negative output voltage from a positive input voltage as shown in Figure 1. In this topology, the ground reference of the IC is the negative output voltage. To use certain features of the IC, interfacing control circuitry needs to be shifted from the system ground to the reference of the IC.
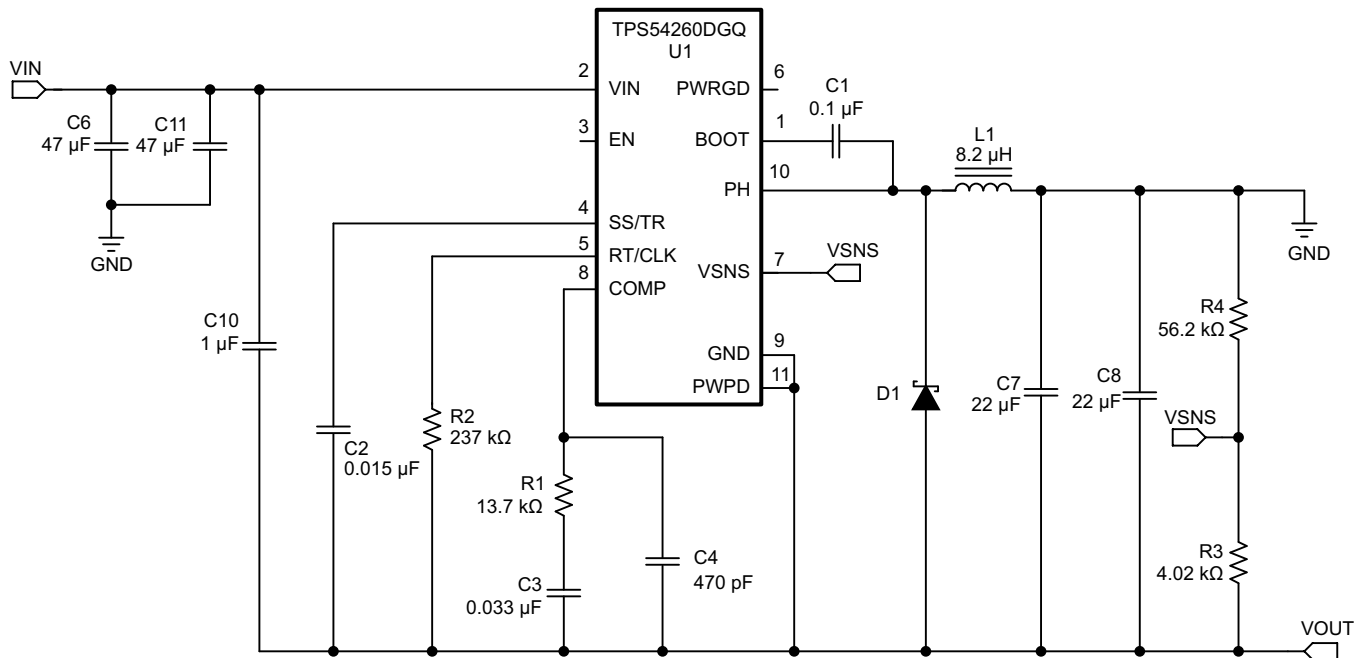

Figure 1. Inverting Buck-Boost Topology

2   TPS54260 Inverting Buck-Boost Design

The inverting buck-boost topology is simply a buck converter with the inductor and catch diode switched places. Additionally, the output capacitors are reversed in polarity. When the FET switch is on, the voltage across the inductor is Vin and the current ramps up at a rate of di/dt = Vin/L. The entire load current is supplied by the output capacitor during the switch on time. When the FET switch turns off, the inductor current must remain continuous, thus turning on the catch diode. The voltage across the inductor becomes approximately Vout, and the inductor current decreases at a rate of di/dt = –Vout/L. The inductor supplies current to both the load and the output capacitor during the FET off time. A more detailed description of the inverting buck boost topology can be found in the "Using a Buck Converter in an Inverting Buck-boost Topology" application note (Ref 1).

Following the inverting buck-boost topology depicted in Figure 1 and the design guidelines in the SLVA317A application report (Ref 2), an inverting buck-boost design was made with the TPS54260 buck converter. The design guidelines can be placed in the Excel document, "Inverting Power Supply Calculator for SWIFT DC/DC with Integrated FETs" (Ref 3) to simplify component selection.

Figure 2 depicts the resultant schematic and Table 1 outlines the design targets. This design uses a 5-V input voltage to provide a convenient pull up for the PWRGD signal.
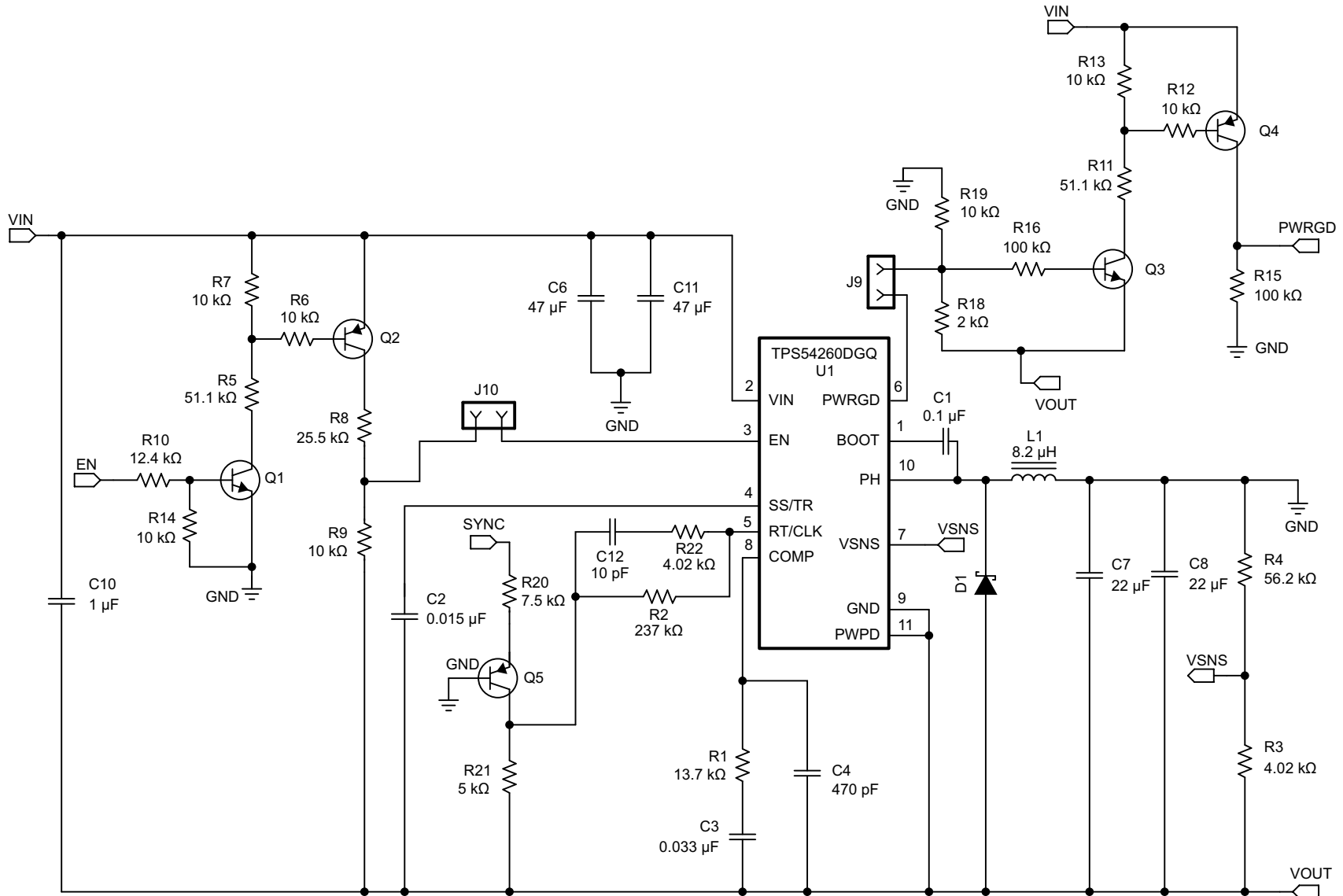
Figure 2. TPS54260 Inverting Buck-Boost Schematic

Table 1. TPS54260 Inverting Buck-Boost Requirements

		VALUE	UNIT
V_I	Input voltage	5	V
	Input voltage ripple	<1%	
V_o	Output voltage	-12	V
dV_o	Output voltage ripple	<0.5%	
I_o	Maximum output current	1	A
f_{sw}	Switching frequency	500	kHz

3 EN level-shifting control Circuitry

A level-shifting control circuit must be designed to externally control the turn-on/turn-off of the TPS54260 in the inverting buck-boost topology. The level-shifting circuit will translate the external EN signal potential down to be referenced to Vout while still ensuring the TPS54260 will be enabled when referenced to system ground. The EN circuit needs to meet four criteria to ensure proper operation. These criteria are outlined inTable 2 .

Table 2. EN Level-Shifting Conditions

	VALUE	UNIT
Turn on relative to Vin = 5 V (Logic High)	>1.36	V
Turn off relative to Vin = 5 V (Logic Low)	<1.36	V
Turn on relative to Vout = −12 V (Logic High)	≥10.64	V
Turn off relative to Vout = −12 V (Logic Low)	≤10.64	V

At startup, the TPS54260 sees a Vin of 5 V with a reference to the system ground. Thus, the EN pin follows the same electrical characteristics outlined in the TPS54260 datasheet. The maximum turn on (logic high) voltage on the pin must be greater than 1.36 V. To obtain this, a simple voltage divider equation is derived from Figure 3.
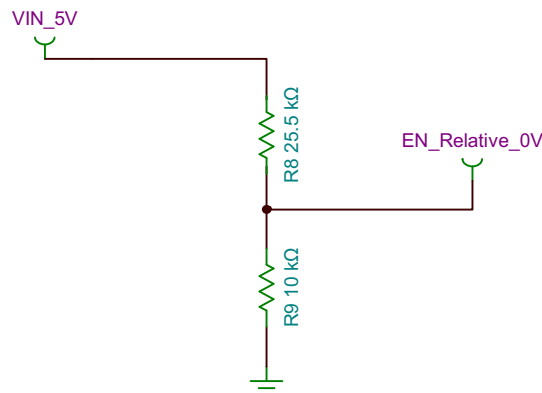
Figure 3. EN Voltage Divider Referenced to the System Ground

$$EN \Rightarrow 5V \times \left(\frac{R9}{R9 + R8} \right) \geq 1.36V \quad or \quad \left(\frac{R9}{R9 + R8} \right) \geq 0.272$$

(1)

When the output of the inverting buck-boost is regulated to −12 V, the TPS54260's "ground" reference becomes −12 V. If a level-shifting circuit is not added to reference the EN signal to −12 V, then the EN pin will see an overall potential of 1.36 V + 12 V = 13.36 V. This potential is more than twice the absolute maximum rating of 5 V, outlined in the TPS54260 datasheet. To prevent damage to the EN pin from overvoltage, the level-shifting circuit will output a potential of −12 V + 1.36 V = −10.64 V or greater to enable the TPS54260. Note, the divider must still ensure that the EN pin does not exceed the maximum pin rating of 5 V (which will be −7 V with a −12 V reference). In this case, the voltage divider in Figure 3 is modified to be referenced to −12 V. The following EN equation is derived from Figure 4.
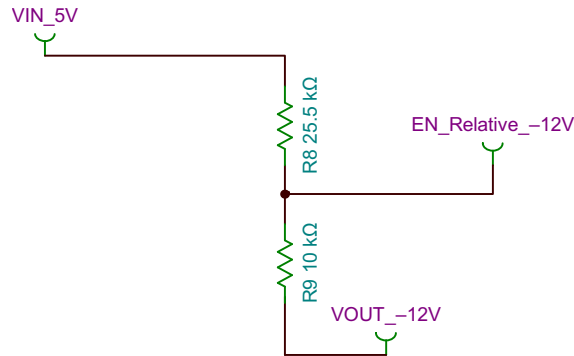
Figure 4. EN Voltage Divider Referenced to Vout

$$EN \Rightarrow -12V + (5V + 12V) \times \left(\frac{R9}{R9 + R8} \right) \geq -10.64V \quad \text{or} \quad \left(\frac{R9}{R9 + R8} \right) \geq 0.08 \tag{2}$$

From Equation 1 and Equation 2, R9 and R8 were chosen to be 10 kΩ and 25.5 kΩ respectively. Placing the values for R9 and R8 back into Equation 1 and Equation 2 gives the following results.

$$EN = 5V \times \left(\frac{10k}{10k + 25.5k} \right) = 1.408V \quad \text{and} \quad EN = -12V + (17V) \times \left(\frac{10k}{10k + 25.5k} \right) = -7.21V \tag{3}$$

With the resistor divider values calculated, the remainder of the level-shifting circuit is implemented as shown in Figure 5.
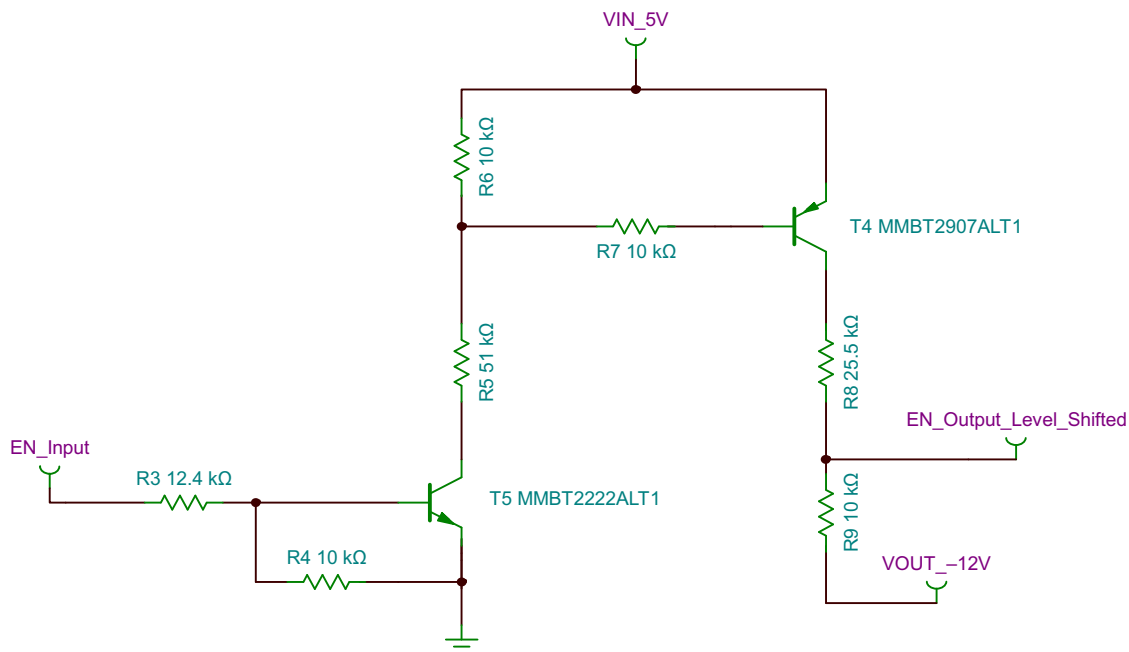
Figure 5. EN Level-Shifting Control Circuit

Resistors R10 and R14 form a voltage divider to turn on the npn BJT. From the MMBT2222A datasheet, the VBE saturation voltage minimum is 0.6 V. Given this value and the goal to level shift once EN is equal to 1.36 V, Equation 4 can be derived.

$$EN \Rightarrow 1.36V \times \left(\frac{R14}{R10 + R14} \right) = 0.6V \quad \text{or} \quad \left(\frac{R14}{R10 + R14} \right) = 0.44 \tag{4}$$

Thus R10 is picked to be 12.4 kΩ while R14 is 10 kΩ. With Q1 on, current will flow through R5, creating another voltage divider shown in Equation 5.

$$5V \times \left(\frac{R5}{R5+R7} \right) \leq (5V - 0.6V) \text{ or } \left(\frac{R5}{R5+R7} \right) \leq 0.88$$

(5)

From Equation 5, R7 was chosen to be 10 kΩ while R5 to be 51 kΩ. With VBE > 0.6 V, Q2 turns on, and the EN output is derived by Figure 3 and Figure 4. Another resistor, R6, was added to the base of Q2 to limit the current into Q2. Figure 6 shows the waveform of the EN level-shifting output. Notice that the EN level-shifting output will follow the EN input until the TPS54260 turns on. Once the IC is on, the level-shifting output follows the output voltage until it reaches –7.21 V (as calculated in Equation 3).
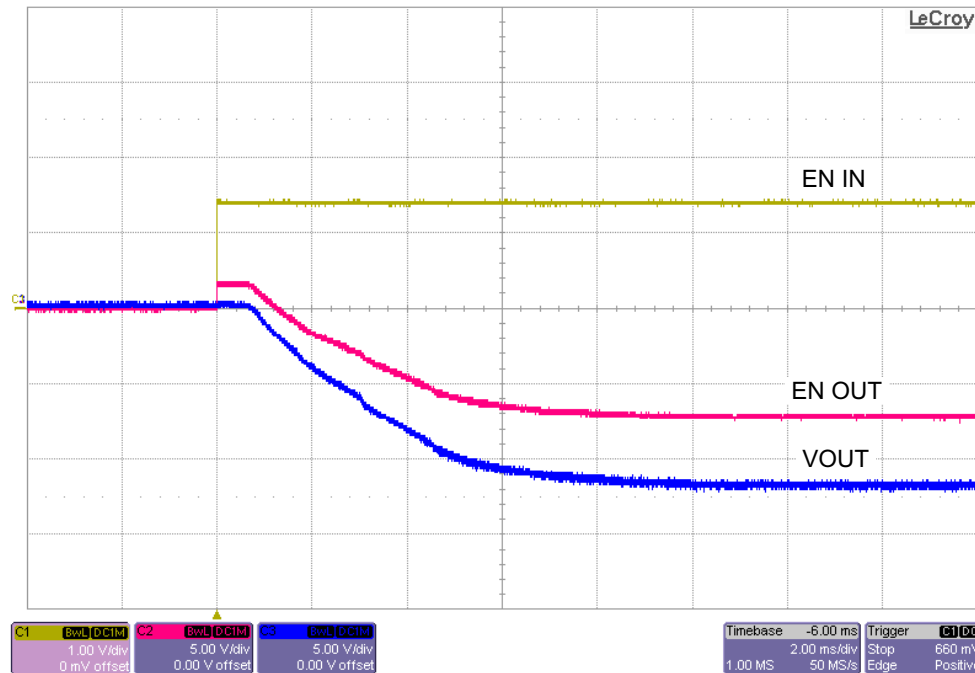
Figure 6. EN Startup

When the EN input is pulled to ground, the EN level-shifting output is pulled to –12 V, turning off the TPS54260. As the output voltage rises back to 0 V, the EN level-shifting output follows the output voltage back to 0 V as depicted in Figure 7.
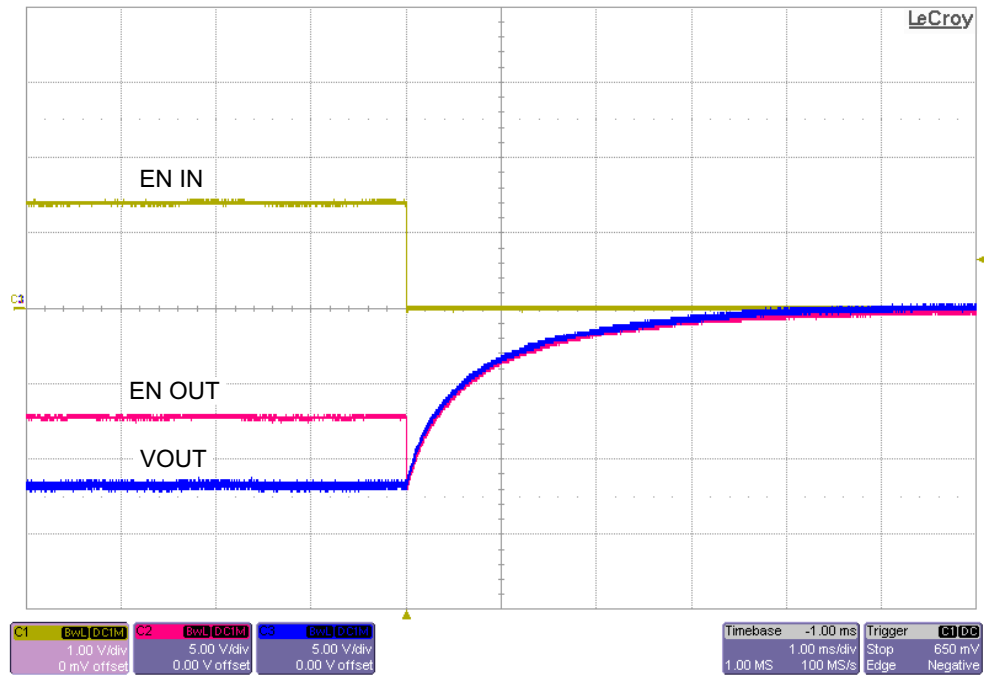
Figure 7. EN Shutdown

4   RT/CLK level-shifting control Circuitry

Like the EN level-shifting control circuitry, the RT/CLK level shifting needs to translate the external clock synchronization signal from the system ground reference to IC reference of Vout without exceeding the RT/CLK pin's absolute maximum rating. Additionally, this circuitry must ensure that if no external clock is present or if the external clock is held low, the device still switches at a frequency set by the RT resistor. Figure 8 shows the RT/CLK level-shifting control circuitry which allows synchronization through the use of the RT clock resistor or an external PLL.
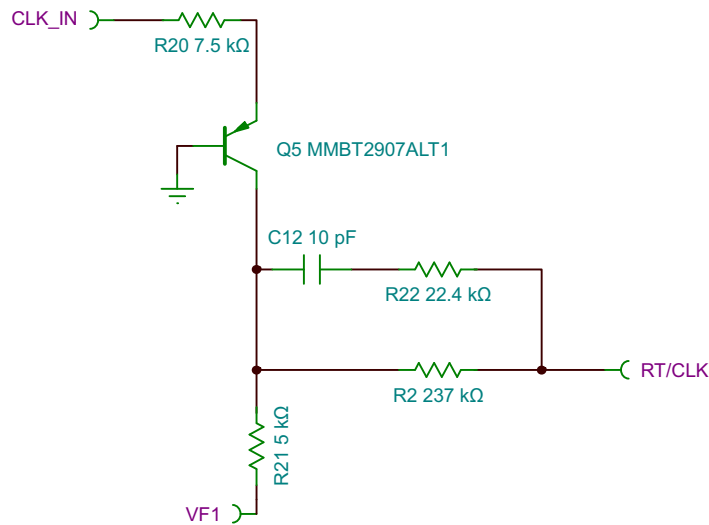
Figure 8. CLK Level-Shifting Control Circuitry

NOTE: If your external clock is held high during power up or shut down, this circuit is not the optimal solution. This circuit provides a very simple solution to level shift the RT/CLK pin but is designed to follow the operation of the RT/CLK pin outlined in the TPS54260 datasheet.

The PNP transistor will turn on when the potential of the external clock source is above the saturation voltage of the transistor. This will create a current which will force a voltage at the collector node of the Q5 BJT. Using an external clock source of 0 V to 5 V, the following equation is derived

$$CLK \Rightarrow \left(\frac{5-0.6}{R20} \right) \times R21 - 12V \le -8.4 \quad \text{or} \quad \left(\frac{R21}{R20} \right) \le 0.818$$

(6)

The output voltage calculated from the equation above must not exceed the RT/CLK pin's maximum rating of 3.6 V or –12 V + 3.6 V = –8.4 V with the level shifting. Additionally, the voltage at this node must satisfy the RT/CLK pin's high and low thresholds from the TPS54260 datasheet. The high threshold must exceed 2.2 V or greater than -9.8 V for the RT/CLK pin to register a high. It also needs to be lower than 0.5 V or less than –11.5 V for a low. Given these conditions, R20 was chosen to be 7.5 kΩ while R21 is 5 kΩ. These values will output a –9 V potential at the RT/CLK pin when the external clock is high and a–12 V potential when it is low. Figure 9 shows the external clock signal, the PH node, the regulated output voltage and the potential at the RT/CLK pin at 500kHz.
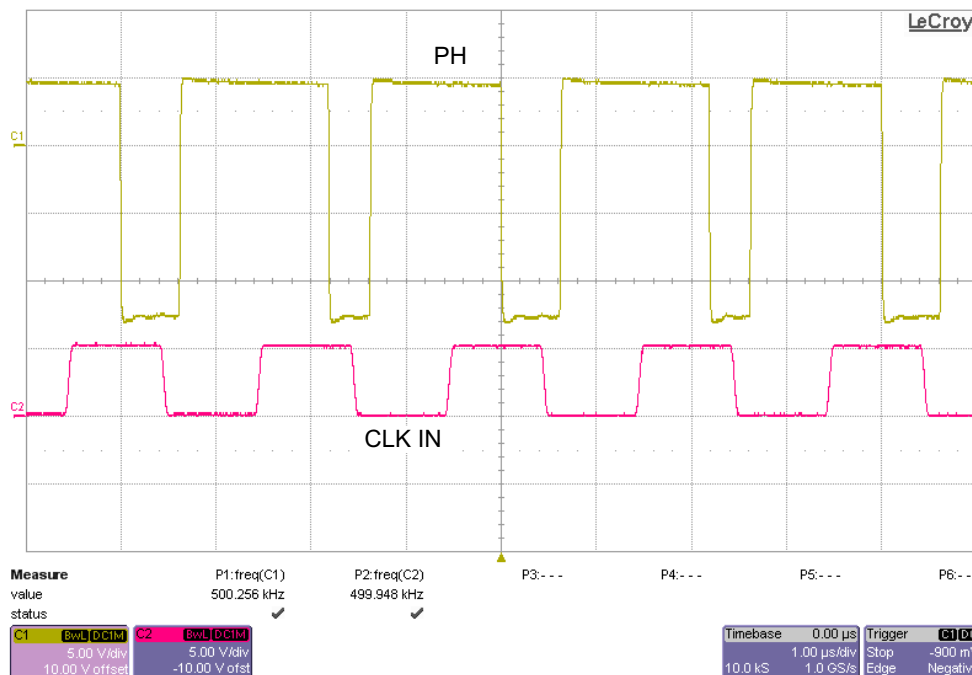
Figure 9. CLK Level Shifting at 500 kHz

When the external clock signal is held low or when it is left floating, the switching frequency will be set by the RT resistor R2. A detailed description for the calculation of the RT resistor and the operation of the RT/CLK pin can be found in the "How to Interface to RT/CLK" in the TPS54260 datasheet. This same section describes components C12 and R22 in Figure 8, which AC couples the external clock signal to reduce jitter. Figure 10 shows the operation of the circuit when the external clock is held low.
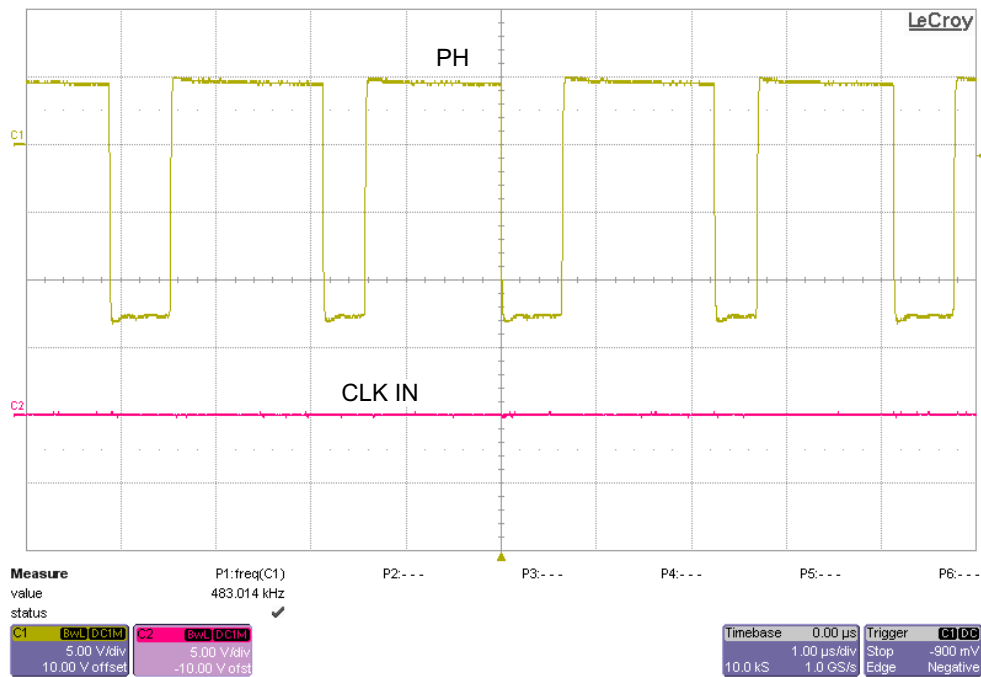
Figure 10. CLK Level Shifting in RT Mode

5 PWRGD level-shifting control Circuitry

The PWRGD level-shifting control circuitry follows the same basic principles as the EN level-shifting circuit, except the PWRGD pin needs to be level shifted up from the Vout reference potential to the system ground. The PWRGD level shifting will need to meet the criteria outlined in Table 3.

Table 3. PWRGD Level-Shifting Conditions

Power is good and output in regulation	Logic High or 5 V
Power is not good (both Vout or system ground referenced)	Logic Low or 0 V

Figure 11 shows the level-shifting control circuit connected with the open drain PWRGD MOSFET, which is internal to the TPS54260.
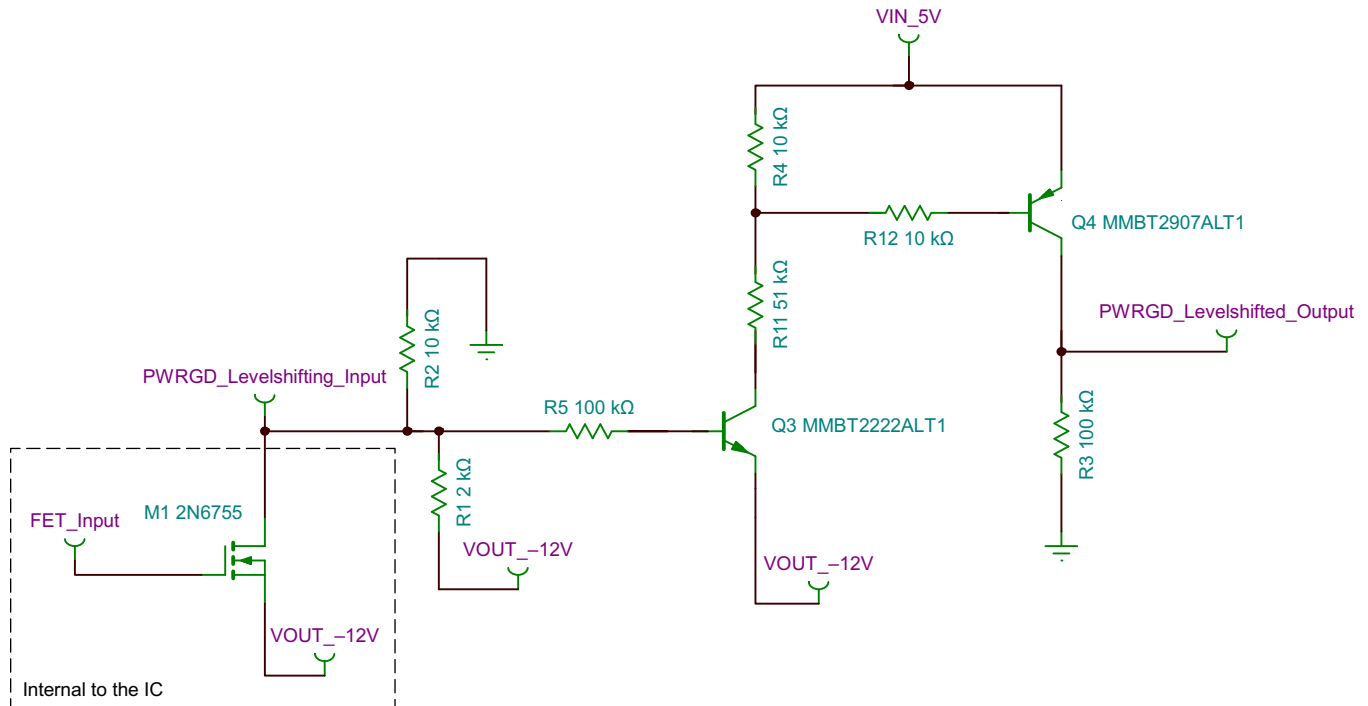
Figure 11. PWRGD Level-Shifting Control Circuit

When power is good, the internal MOSFET will be off and therefore an open circuit. The resistor divider for R1 and R2 will pull up the potential at the gate of Q3 to –10 V to turn on the BJT. Equation 6 shows the resistor divider equation to calculate R18 and R19.

$$PWRGD \Rightarrow -12V \times \left(\frac{R19}{R18+R19} \right) \geq -12V + 0.6V \text{ or } \left(\frac{R19}{R18+R19} \right) \leq 0.95 \tag{7}$$

The resistor divider potential must be greater than Q3's saturation voltage. To ensure Q3 turns on, a potential of –10 V was chosen for correct operation. Therefore, R18 is calculated to be 2 kΩ while R19 is 10 kΩ. Additionally, R16 = 100 kΩ was added to limit the current flowing into Q3, therefore preventing any damage to the BJT. With Q3 on, the gate potential at the base of Q4 will be lower than its emitter potential. Equation 7 shows how to calculate R11 and R13. Note that it is the same configuration as Figure 4 and the equation's output needs to be less than 5 V–0.6 V = 4.4 V to ensure the gate potential exceeds the saturation voltage.

$$-12V + (5V+12V) \times \left(\frac{R11}{R11+R13} \right) \leq 4.4V \text{ or } \left(\frac{R11}{R11+R13} \right) \leq 0.976 \tag{8}$$

Therefore, R11 is 51 kΩ while R13 is 10 kΩ and R12 = 12 kΩ is added to limit the current into the base of Q4. Lastly R15 is needed to pull the output of the level-shifting circuit to 0 V when PWRGD is low. When Q4 turns on, the level-shifting PWRGD output is pulled up to 5 V. Figure 12 shows the case when power is good and the output is regulated.

PWRGD level-shifting control Circuitry
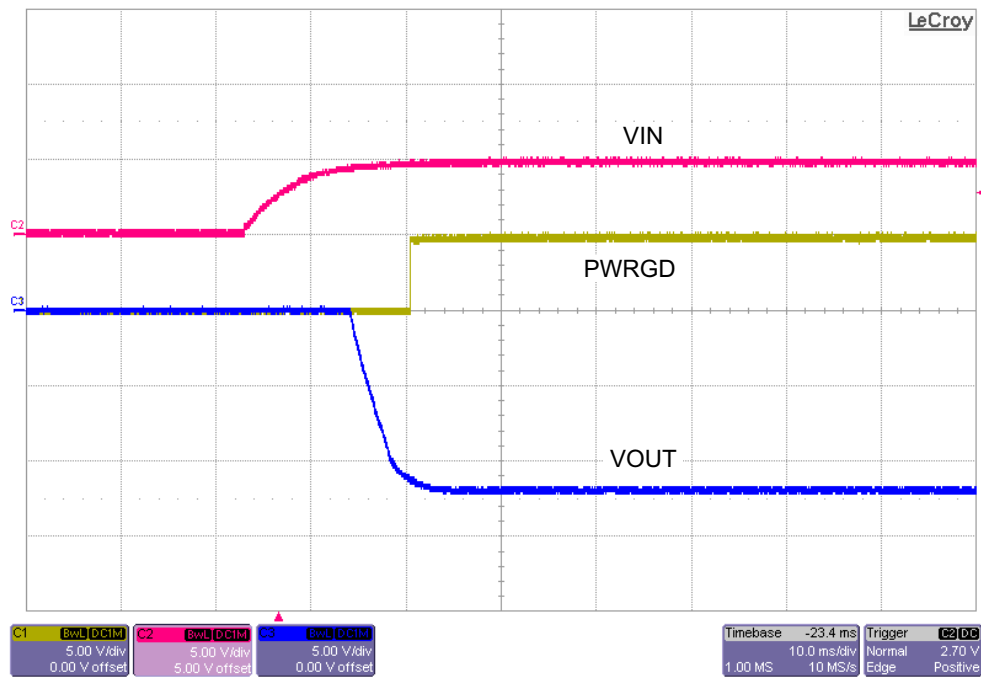
Figure 12. Power Good Startup

When power is not good, the MOSFET will be turned on and will pull the gate of Q3 to Vout. This will force Q3 and Q4 to be off and PWRGD is pulled to 0 V through R15. This is also true during startup when the TPS54260 is referenced to the system ground and the output is not yet in regulation. In this case, Vout is still 0 V and power is not good. Figure 13 shows the case when the PWRGD pin is pulled to 0 V.
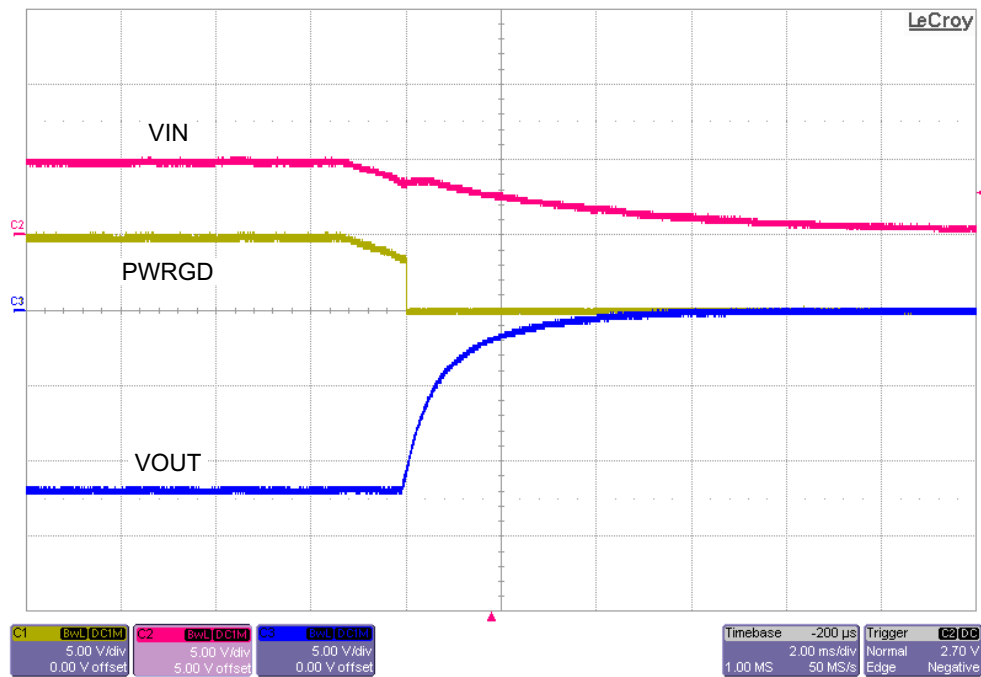
Figure 13. Power Good Shutdown

6 Conclusion

To use certain features of an IC, a level-shifting control circuit may be necessary for a circuit in which the ground reference of the IC is not system ground. The level-shifting circuit allows external control circuits to interact with the IC without exceeding any absolute maximum pin ratings. This application report has demonstrated a design to level shift the EN, PWRGD, and RT/CLK pins in an inverting buck-boost topology. The same principles used in the design of these circuits can be implemented to other topologies and to other external control circuitry.

7 References

1. *Using a Buck Converter in an Inverting Buck-boost Topology*
2. *Create an Inverting Power Supply From a Step-Down Regulator* application report (SLVA317A)
3. *Inverting Power Supply Calculator for SWIFT DC/DC with Integrated FETs*

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