Application Report
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Ultra Small 5A, Adjustable Output Reference Design Using TPS54620

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ABSTRACT

The TPS54620, in a thermally enhanced 3.5mm × 3.5mm QFN package, is a full featured 17V, 6A synchronous step down converter which is optimized for small designs through high efficiency and integration of the high-side and low-side MOSFETs. This report describes the design procedure adopted for ultra small (8mm × 12mm) design and its physical implementation. Additional space saving designs are achieved through current mode control, which reduces component count, and by reducing the inductor's footprint through selecting a high switching frequency.

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1 Design Procedures

1.1 System Requirements

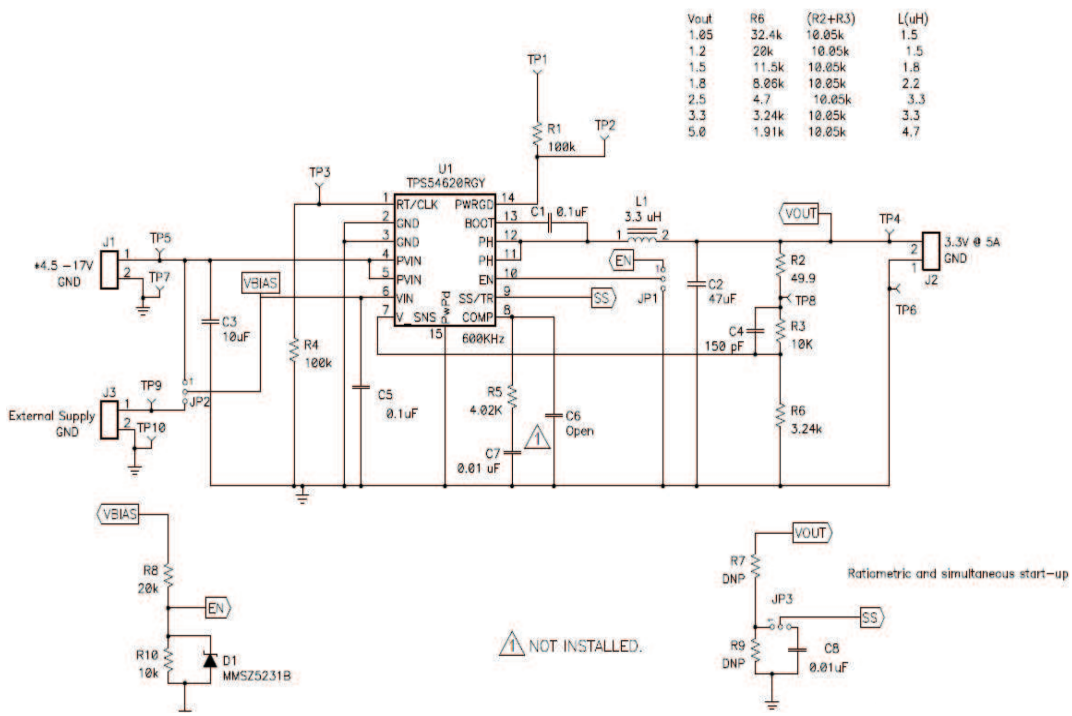
The design requirements for this example are provided in Table 1.

Table 1. Design Requirements Examples

PARAMETER	VALUE
Output Voltage	Adjustable output output
Output Current	5 A
Input Voltage	5 V ± 10%
Transient Response	50 mV
Switching Frequency	480 kHz

1.2 Schematic

The following application schematic shows the TPS54620 configured for adjustable output voltage for 5 ampere of load current.



1.3 Selecting Operating Frequency

The RT/CLK pin can be used to set the switching frequency of the device. To determine the RT resistance for a given switching frequency, use Equation 1. To reduce the solution size, set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered. Higher switching frequencies may produce a smaller solution size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency; however, the higher switching frequency causes extra switching losses, which will affect the converter's efficiency. We have selected 480kHz as the switching frequency according to the tradeoff discussed above.

$$Rrt(k\Omega) = 4800 \times Fsw\ (kHz)^{-0.997} - 2 \quad (1)$$

1.4 Adjustable Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Referring to the application schematic, start with a 10kΩ for R3 and use Equation 2 to calculate R6.

$$R6 = (Vref) \times (R3) / (Vout - Vref) \tag{2}$$

For example, For Vout = 1.5V, R6 comes out to be 11.5kΩ

1.5 Selecting Output Inductor

To calculate the value of the output inductor, use Equation 3. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, KIND is normally from 0.1 to 0.3 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{3}$$

For this design example, use KIND = 0.3 and the inductor value is calculated. For Vout= 1.5V a nearest standard value was chosen: 1.8 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 4 and Equation 5.

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{V_o \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{4}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{5}$$

For Vout = 1.5V ILrms and ILpeak comes out to be 5.018A and 5.75A respectively.

1.6 Input Capacitor Selection

The TPS54620 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 µF of effective capacitance on the PVIN input voltage pins and 4.7 µF on the VIN input voltage pin. In some applications, additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. For this design, the PVIN and VIN pins are tied together to use a common input voltage supply. But VIN can be tied to external supply as per user’s requirement. Additional jumper are provided for this purpose.

1.7 Output Capacitor Selection

The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria. Equation 6 shows the minimum output capacitance necessary to accomplish this.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} \tag{6}$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example ΔIout = 1A, ΔVout = 5% of Vout, Fsw = 480kHz gives us value around 33µF, so we selected 47µF ceramic capacitor on output which usually has very low ESR.

1.8 Slow Start Capacitor Selection

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54620 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 7.

$$C7(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{7}$$

1.9 Compensation Design

The compensation design is a tradeoff between stability and the load transient response. Lesser phase margin means a great transient response, but the stability of the system suffers whereas a higher phase margin degrades the transient response and improves stability. For most conditions, the regulator has a phase margin between 60 and 90 degrees.

The following steps are adopted for compensating the design:

1. Select cross over frequency somewhere between 1/10 Fsw to1/6 Fsw
2. Then R5 can be calculated using Equation 8

$$R5 = \frac{2 \times Pie \times Fc \times V_{out} \times C_{out}}{Gm_{EA} \times GMm_{PS} \times V_{REF}} \tag{8}$$

Where:

F_{co} = Closed-loop crossover frequency
V_{OUT} = Output voltage
C_{OUT} = Output capacitance
Gm_{EA} = Error amplifier transconductance
V_{REF} = Reference voltage
Gm_{PS} = Power stage transconductance

3. $$C7 = \frac{1}{2 \times Pie \times Fc \times R5}$$

2 Performance Parameters

2.1 Startup Waveform

Figure 1 shows the startup waveform for TPS54620. Input was set at 10V and output voltage was 1.5V at full load of 5A.

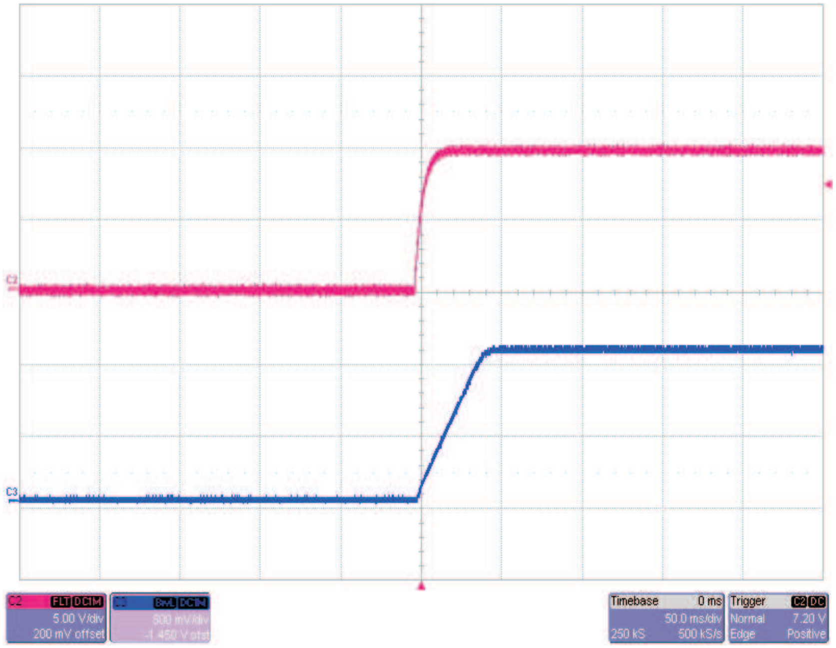


Figure 1. Startup Waveform

2.2 Load Transient

The Figure 2 and Figure 3 show the 1.5 volt output response to load transients. The input voltage was set to 10V.

Channel 3 : Vout (AC coupled)
Channel 4 : Load current (Varies between 500mA to 3.5A)

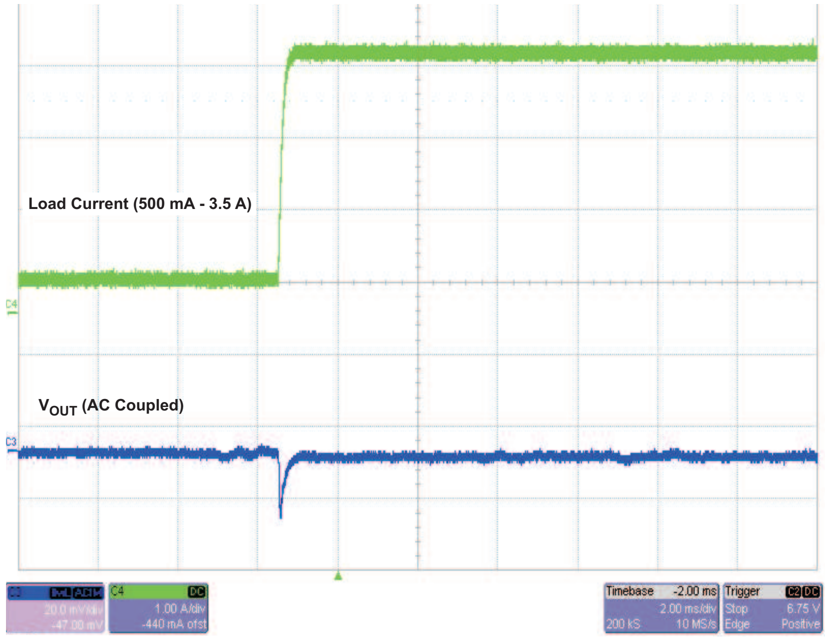


Figure 2. Output Response to Load Transients

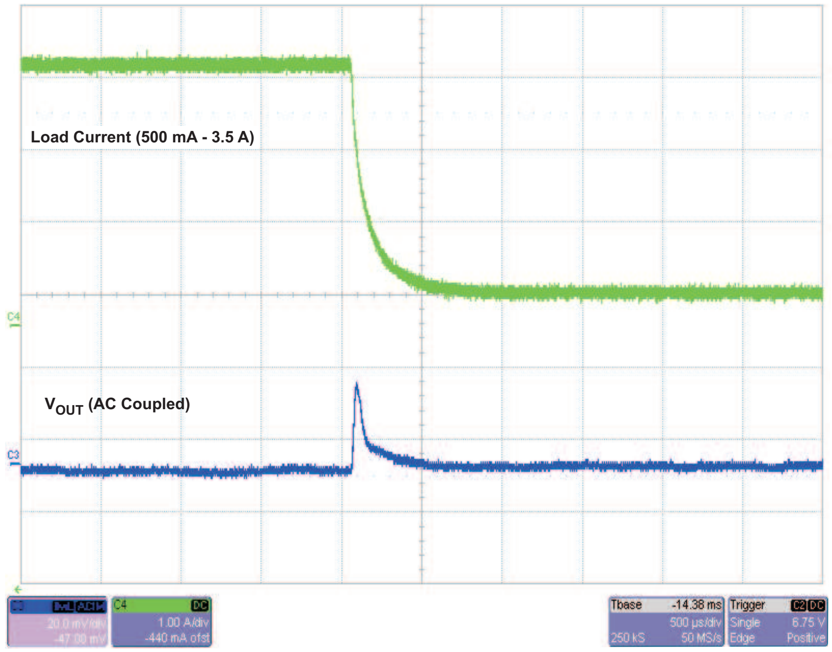


Figure 3. Output Response to Load Transients

2.3 Output Ripple Waveform

Figure 4 shows the output ripple at full load current.

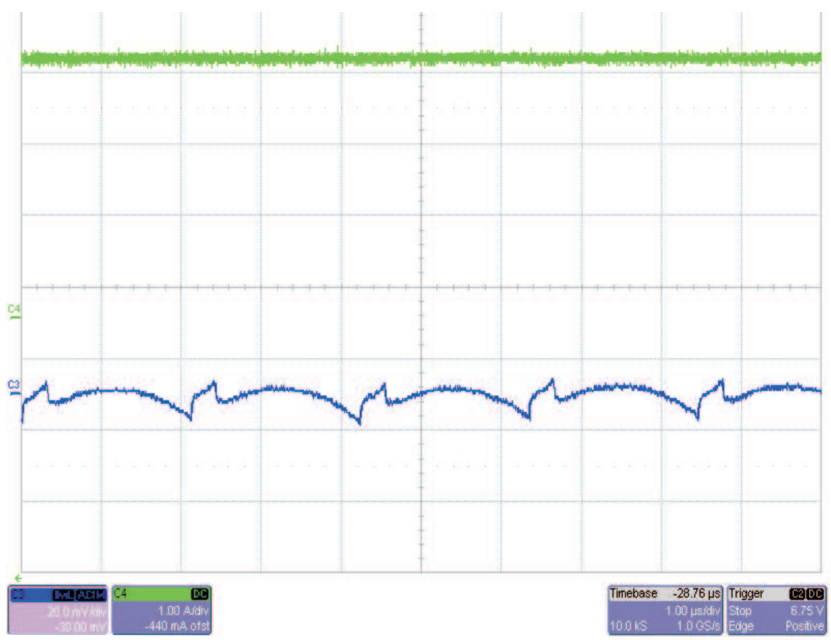


Figure 4. Output Ripple Waveform

2.4 Control Loop Response

Figure 5 shows control loop response for this design. Phase margin was around 55 degrees while Fc was around 100kHz

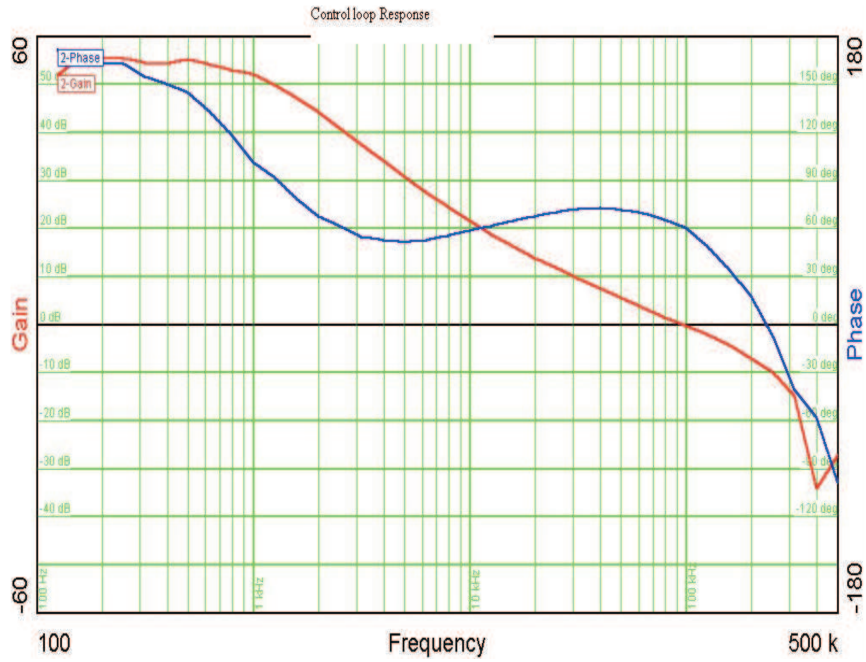


Figure 5. Control Loop Response

3 Physical Implementation

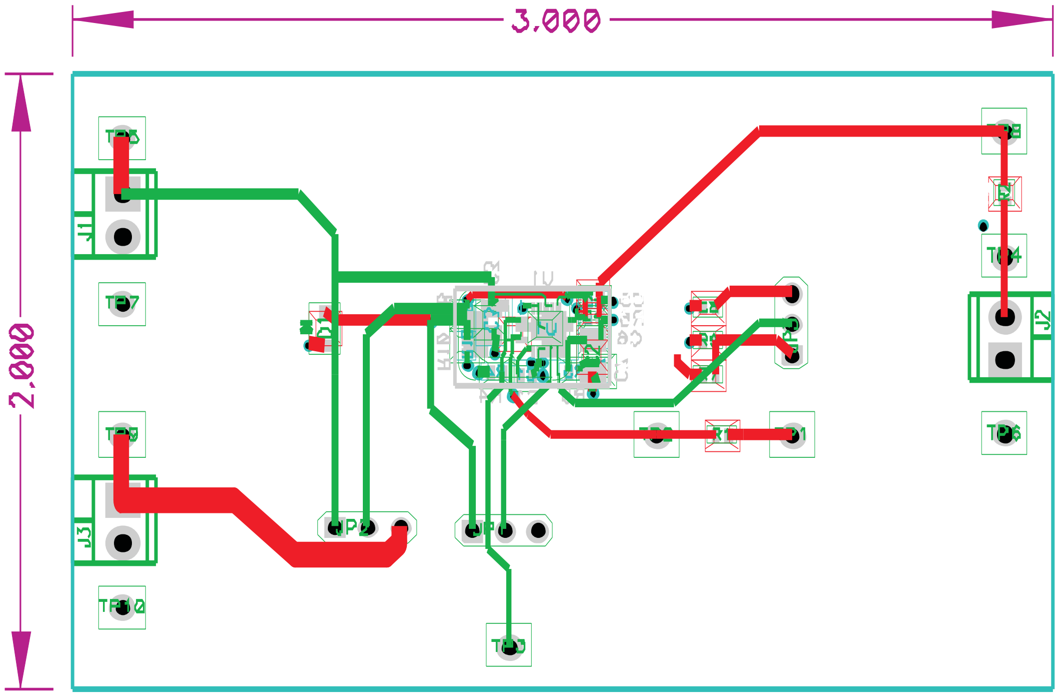


Figure 6. Top Layer

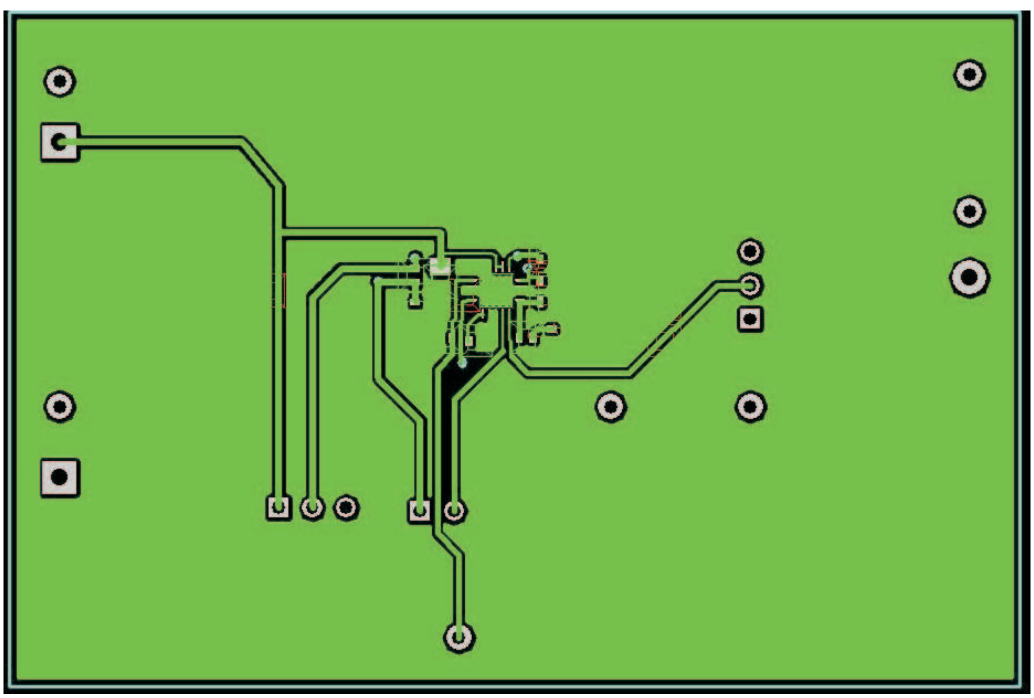


Figure 7. Bottom Layer

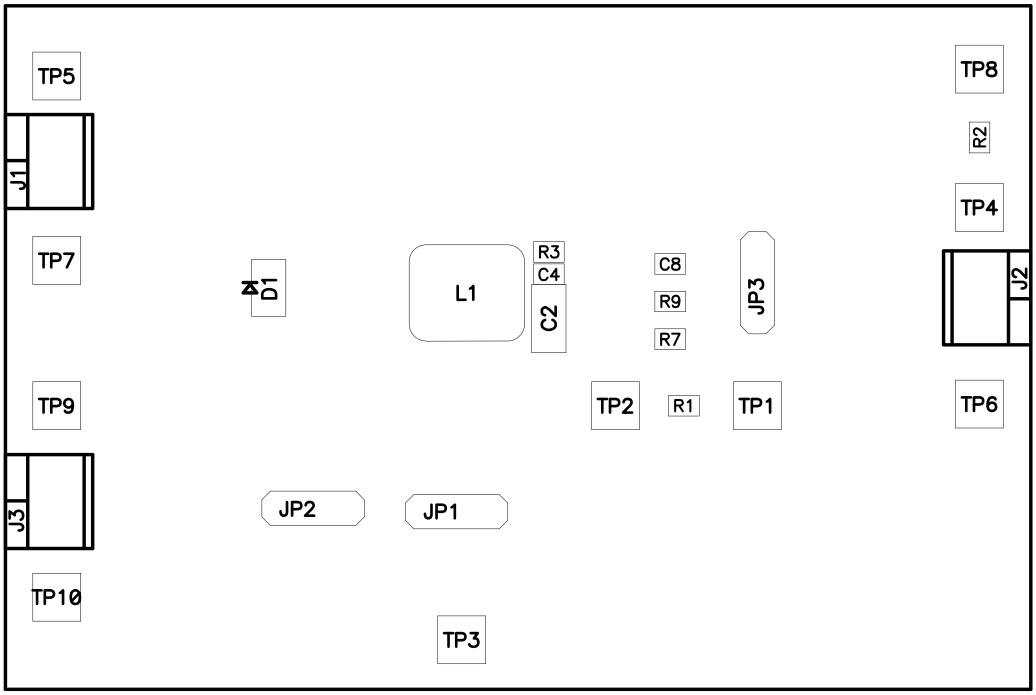


Figure 8. Top Assembly

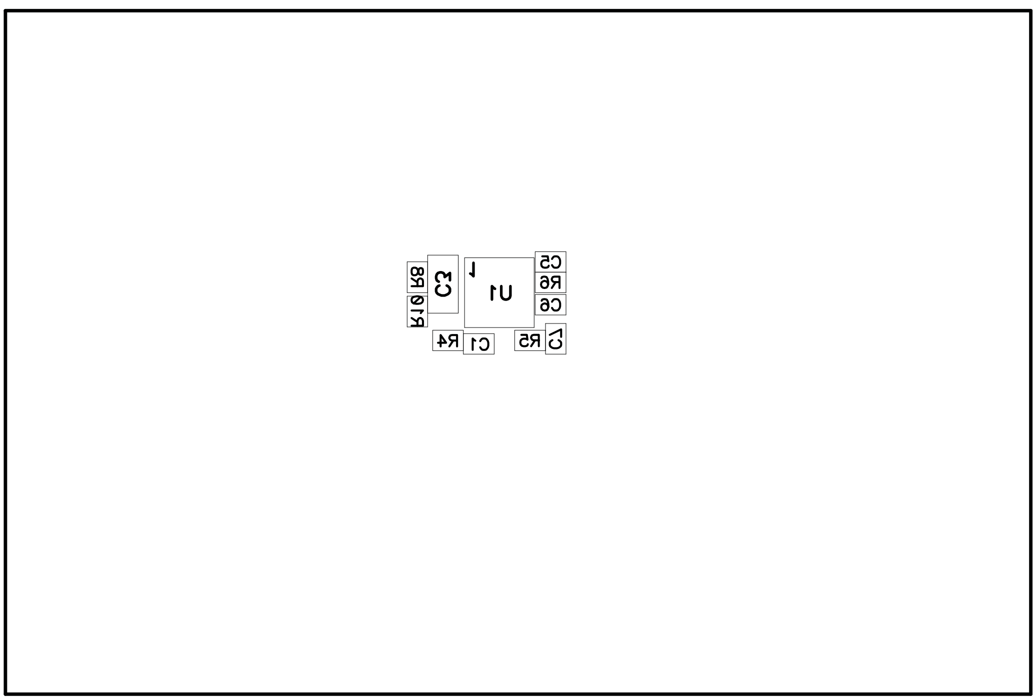


Figure 9. Bottom Assembly

4 Bill of Materials

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	0.1uF	Capacitor, Ceramic, 16V, X5R, 20%	402	STD	STD
1	C2	47uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	Std	TDK
1	C3	10uF	Capacitor, Ceramic, 16V, X5R, 20%	805	C2012X5R1C106M	TDK
1	C4	150 pF	Capacitor, Ceramic, 25V, NPO, 10%	402	Std	{MFR}
1	C5	0.1uF	Capacitor, Ceramic, vvV, [temp], [tol]	402	Std	{MFR}
1	C6	Open	Capacitor, Ceramic, 25V, NPO, [tol]	402	Std	{MFR}
1	C7	0.01uF	Capacitor, Ceramic, 25V, X7R, 20%	402	Std	{MFR}
1	C8	0.01uF	Capacitor, Ceramic, 25V, NPO, 10%	402	Std	{MFR}
1	D1	MMSZ5231B	Diode, Zener, 5.1V, -mA	SOD-323	MMSZ5231BS	Diodes
3	J1, J2, J3	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
3	JP1, JP2, JP3		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 x 3	PTC36SAAN	Sullins
1	L1	3.3 uH	Inductor, SMT, yyA, zz-milliohm	0.255 x 0.270 inch	IHLP2525CZ-01	Vishay
1	R1	100k	Resistor, Chip, 1/16W	402	Std	Std
1	R10	10k	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	R2	49.9	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	R3	10K	Resistor, Chip, 1/16W	402	Std	Std
1	R4	100k	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	R5	4.02K	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	R6	3.24k	Resistor, Chip, 1/16W	402	Std	Std
2	R7, R9	DNP	Resistor, Chip, 1/16W, 1%	402	Std	Std
1	R8	20k 5	Resistor, Chip, 1/16W, 1%	402	Std	Std
8	TP1, TP2, TP3, TP4, TP5, TP8, TP9, TP10	000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
2	TP6, TP7	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54620RGY	IC, 1.62V-17V Synchronous Buck PWM Converter with Integrated MOSFET	QFN14	TPS54620RGY	TI
	Note:					
		1. These assemblies are ESD sensitive, ESD precautions shall be observed.				
		2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.				
		3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.				
		4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.				

5 Conclusion

The practical design of TPS54620 operates close to required specifications. The actual board size excluding jumpers and test points is ultra small (8mm × 12mm). The board is two sided with four layers. Different tests were performed to ensure proper working of the circuit. Circuit implementation and actual test reports available as PMP5382.