Application Report
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Powering OMAP-L132/L138, C6742/4/6, and AM18x with TPS65070

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ABSTRACT

This documents details the design consideration of a power management unit (PMU) solution for the OMAP-L132/-L138 low-power applications processors with a TPS65070 five-channel power management device.

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1 OMAP-L132/L138 Power and Sequencing Requirements

1.1 Power Requirements

Table 1 summarizes the power requirements for the OMAP-L132/L138 processor.

Table 1. OMAP-L132/L138 Power Requirements[1][2][3]

	Pin Name [4]	Voltage	I_{MAX}	Tolerance	Sequencing Order	Timing Delay
I/O	RTC_CVDD	1.2 V	1 mA	–25%, +10%	1[5]	n/a
Core	CVDD	1.0 V / 1.1 V / 1.2 V	600 mA	–9.75%, +10%	2	n/a
I/O	VDDARNWA.,VDDARNW1, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2 V	200 mA	–5%, +10%	3	n/a
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8 V	180 mA	±5%	4	n/a
I/O	USB0_VDDA33, USB1_VDDA33	3.3 V	24 mA	±5%	5	n/a
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 V / 3.3 V	50 mA / 90 mA[6]	±5%	4 / 5	n/a

(1) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.
(2) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1)
(3) There is no specific required voltage ramp rate for any of the supplies LVCMOS33 never exceeds STATIC18 by more than 2 V.
(4) SATA, USB1 not available on OMAP-L132.
(5) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.
(6) If DVDD3318_A, B, and C are powered independently, the maximum power for each rail will be 1/3 the max power shown in this table.

1.2 Power-Up Sequence

The power-up sequence is divided into groups of the same voltages.

Use the power-up sequence described in Table 2. DCDC3, DCDC2, LDO1, and LDO2 are part of the automatic power-up sequence.

Table 2. OMAP-L132/L138 Power Groups

Order	Group	Voltage
1	RTC12	1.2 V
2	STATIC12	1.2 V
3	STATIC18	1.8 V
4	STATIC33	3.3 V

DCDC1 is not part of the power-up sequence. DCDC1 is controlled by its ENABLE pin (EN_DCDC1). EN_DCDC1 is driven from a supervisor circuit (SVS) that monitors DVDD3318 (DCDC2). Once the output voltage of DCDC2 increases above the threshold set with R1 and R2, the SVS pulls tEN_DCDC1 up to V_{SYS}, thereby enabling DCDC1; see Figure 1.

If DVDD3318 (DCDC2) is configured for 1.8 V (DEFDCDC2 = low), LDO1 is isolated from the OMAP-L132/L138 with an external transistor, T2. T2 connects the output of LDO1 to the OMAP-L132/L138 delayed by an external circuit consisting of T1, T2, R3, and R4 to meet the correct power-up sequence requirements. If DVDD3318 (DCDC2) is configured for 3.3 V (DEFDCDC2 = high), this external delay circuit is not required. The LDO output can be directly connected to the OMAP-L132/L138.

1.3 Power-Down Sequence

The power supplies can be powered off in any order as long as LVCMOS supplies operated at 3.3 V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed static 1.8-V supplies by more than 2 V. There is no specific required voltage ramp-down rate for any of the supplies (except as required to meet the stated voltage condition). The power-down sequence of the TPS65070 is the reversed power-up sequence.

To meet the power-down requirements described here, an additional resistor divider R1 and R2 is required to disable DCDC1 fast enough to ensure that the voltage difference between DCDC2 and DCDC1 does not exceed 2.0 V. The TPS3805 does have a threshold voltage of 1.226 V at the SENSE input. Using an external resistor divider, with R1 = 100kΩ and R2 = 390kΩ, sets the trip voltage when DCDC1 is disabled to 1.55 V. This configuration should ensure the difference between DCDC1 and DCDC2 never exceeds 2.0 V.

2 Sequencing with TPS65070

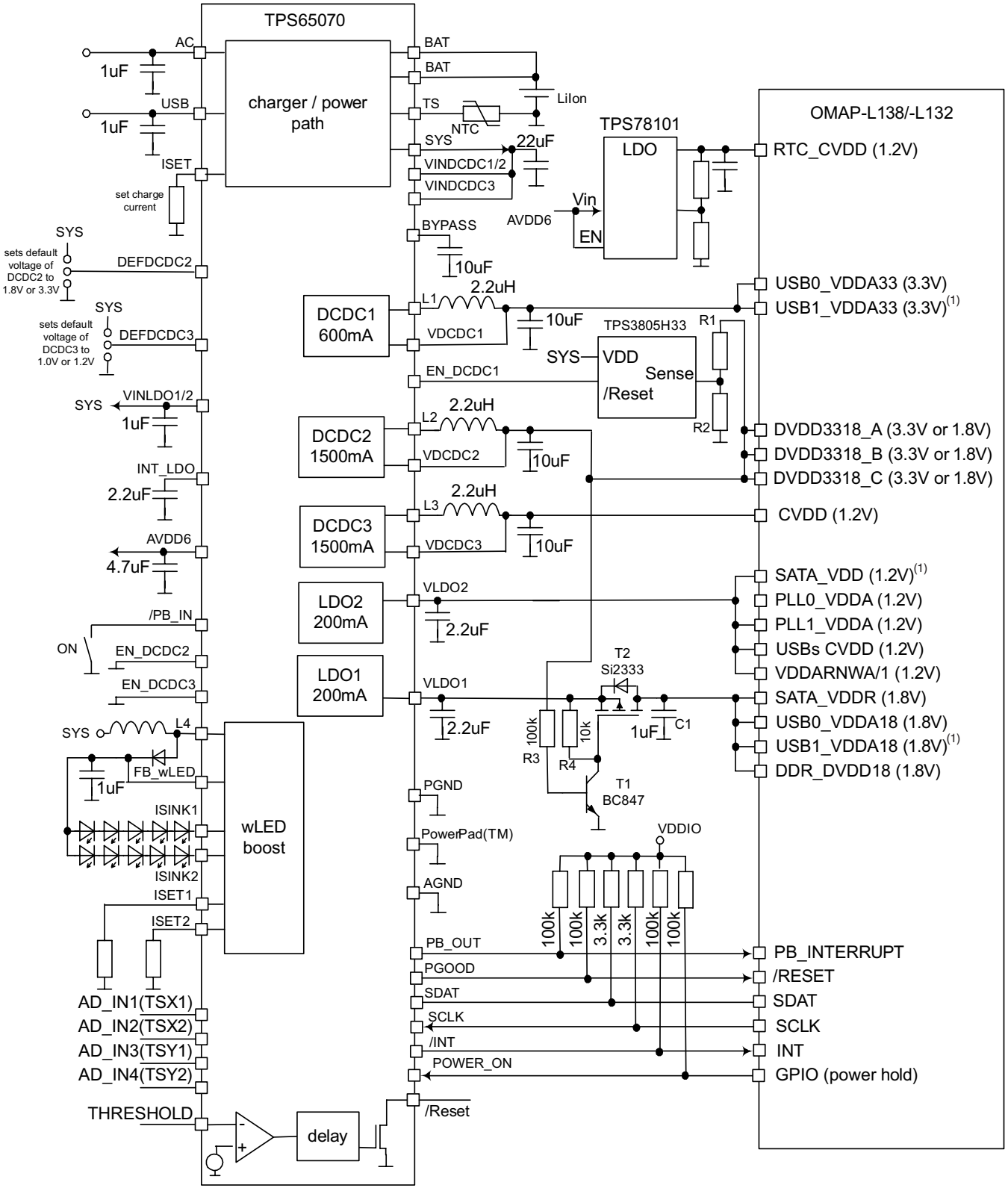
The TPS65070 power management unit supports the power requirements of the OMAP-L132/L138; the single highly-integrated Power Management device provides the voltage settings and sequencing for the OMAP-L132/L138. Table 3 lists the output rail configuration for the TPS65070.

Table 3. TPS65070 Output Rail Configuration

Rail [1]	Voltage	Converter	Sequencing Order
RTC_CVDD	1.2 V	External LDO	1
USB0_VDDA33, USB1_VDDA33	3.3 V	DCDC1	5
DVDD3318_A, DVDD3318_B, DVDD3318_C	3.3 V / 1.8 V	DCDC2	4 / 5 (part of automatic sequence)
CVDD	1.2 V	DCDC3	2 (part of automatic sequence)
VDDARNWA. VDDARNW1, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2 V	LDO2	3 (part of automatic sequence)
USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8 V	LDO1	4[2]

(1) USB1, SATA are not available on OMAP-L132.
(2) If VDVV3318 is configured for 3.3 V, LDO1 and LDO2 can ramp up together.

Figure 1 shows a complete application diagram that details how to connect the TPS65070 to power an OMAP-L132/L138 application processor.



(1) Not available on OMAP-L132.

Figure 1. TPS65070 Power Solution Diagram

Figure 2 and Figure 3 illustrate the power-up sequence timing for 1.8-V and 3.3-V I/O, respectively.

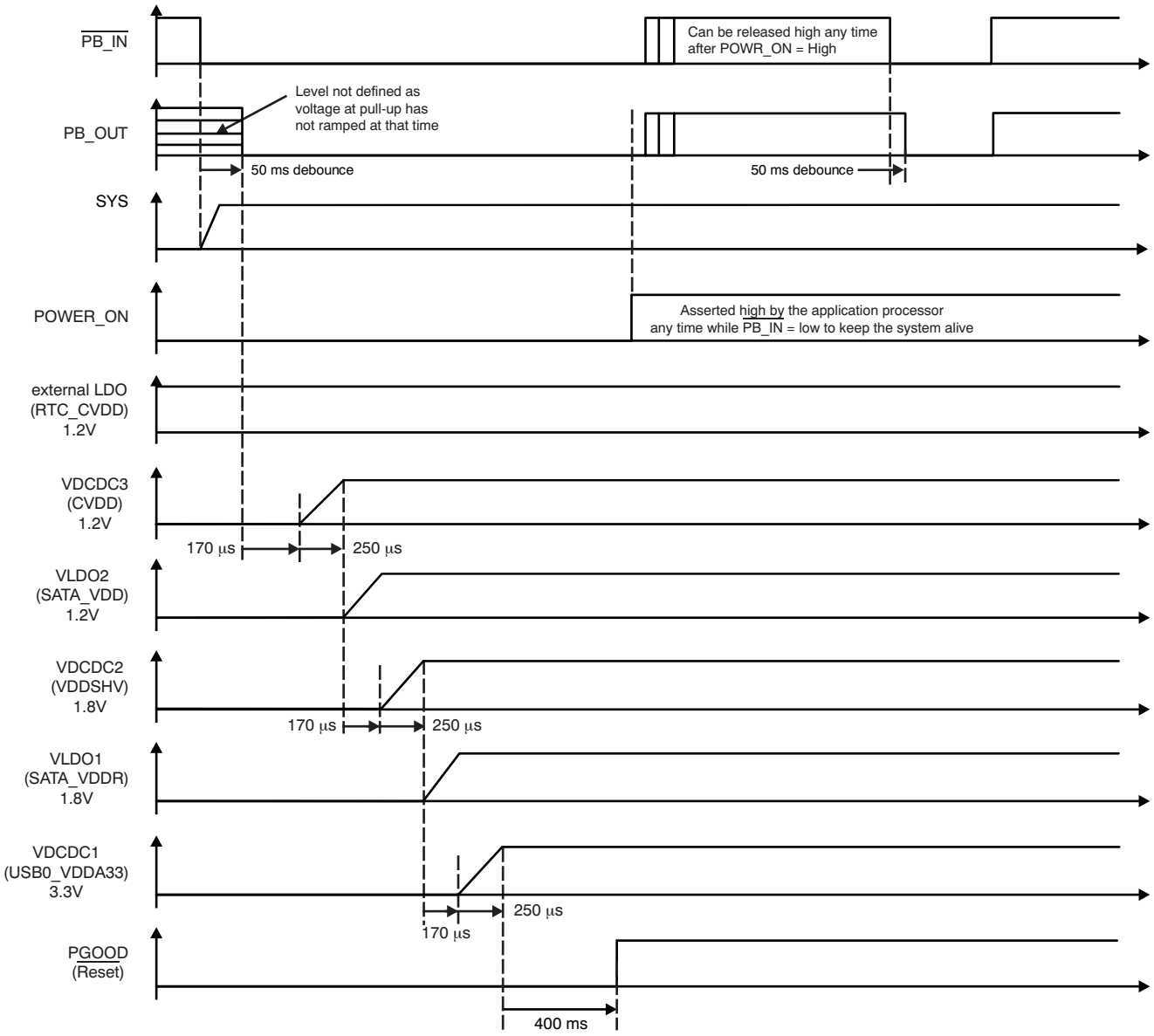


Figure 2. Power-Up Sequencing Timing Diagram (1.8-V I/O)

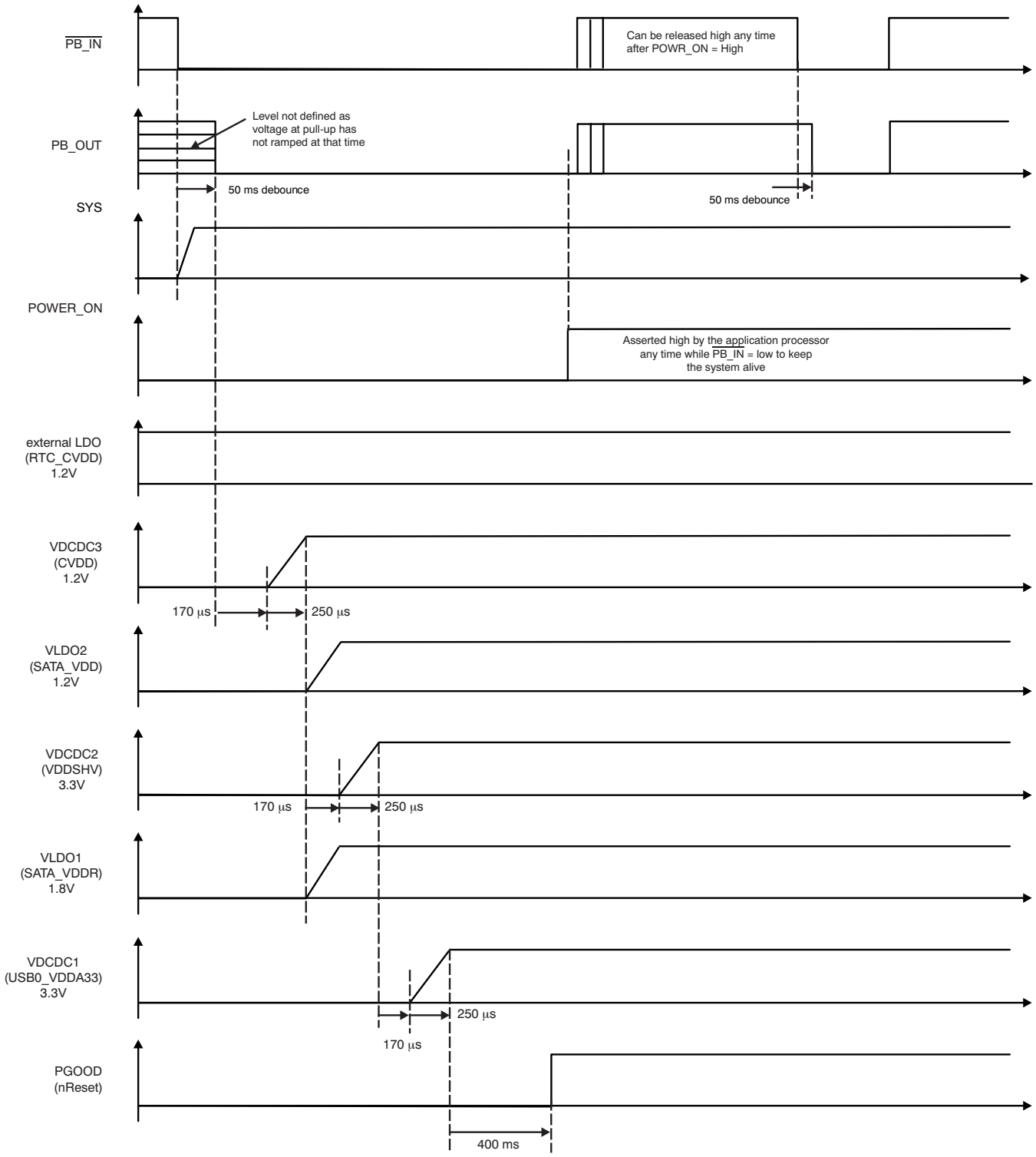


Figure 3. Power-Up Sequencing Timing Diagram (3.3-V I/O)

3 Detailed Power Sequence

1. The 1.2-V Real-Time Clock supply RTC_CVDD is supplied by an external LDO that is powered and enabled by AVDD6. AVDD6 is an output of the TPS65070 that is always on. As soon as input power is applied to the TPS65070, the external LDO is supplied and starts up.
2. The sequencing begins when the pushbutton input PB_IN is pulled low. When PB_IN is pulled low, the TPS65070 begins with the automatic sequencing for dc-to-dc converters and low-dropout regulators (LDOs) defined in the registers CTRL_1 and LDO_CTRL.
3. DCDC Converter 3 is the first rail to start up in the automatic sequence.
4. After PGOOD goes high (400 ms after DCDC3 is within regulation), DCDC2, LDO1, and LDO2 become enabled. DCDC2 and LDO2 ramp up immediately. LDO1 will be connected by delay to the OMAP-L1x8 with an external transistor from DCDC2 in case the OMAP-L1x8 is working with 1.8-V I/O (with DCDC2 configured for 1.8 V). If OMAP-L1x8 is working with 3.3-V I/O (that is, with DCDC2 configured for 3.3 V), LDO1 can be directly connected to the OMAP-L1x8; there is no need for the external delay circuit T1, T2, R3, and R4.
5. DCDC1 will be enabled after DCDC2 ramps up. The EN_DCDC1 pin is controlled from an external supply voltage supervisor (SVS) that pulls the enable pin to SYS after DCDC2 ramps up.
6. In order to keep the converters and LDOs of the TPS65070 enabled, the POWER_ON input of the TPS65070 must be driven high before PB_IN is released high. POWER_ON is connected to a GPIO of the OMAP-L132/L138 that drives PWR_ON high after the processor starts up.

4 Test Results

Figure 4 through Figure 7 illustrate the test results.

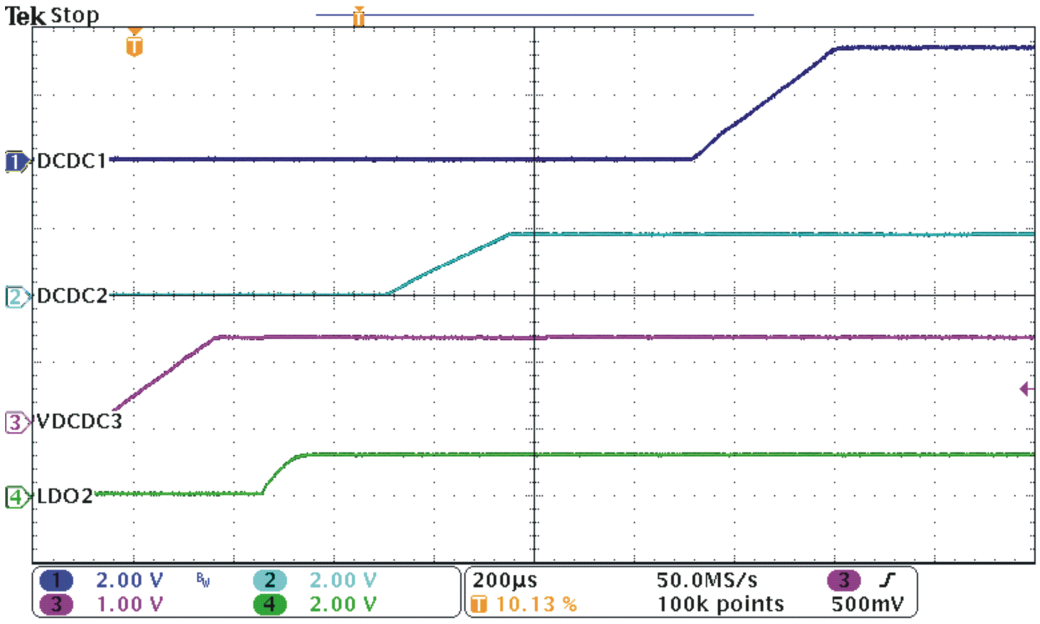


Figure 4. Startup of DC/DC Converters and LDO2 (DCDC2 = 1.8 V)

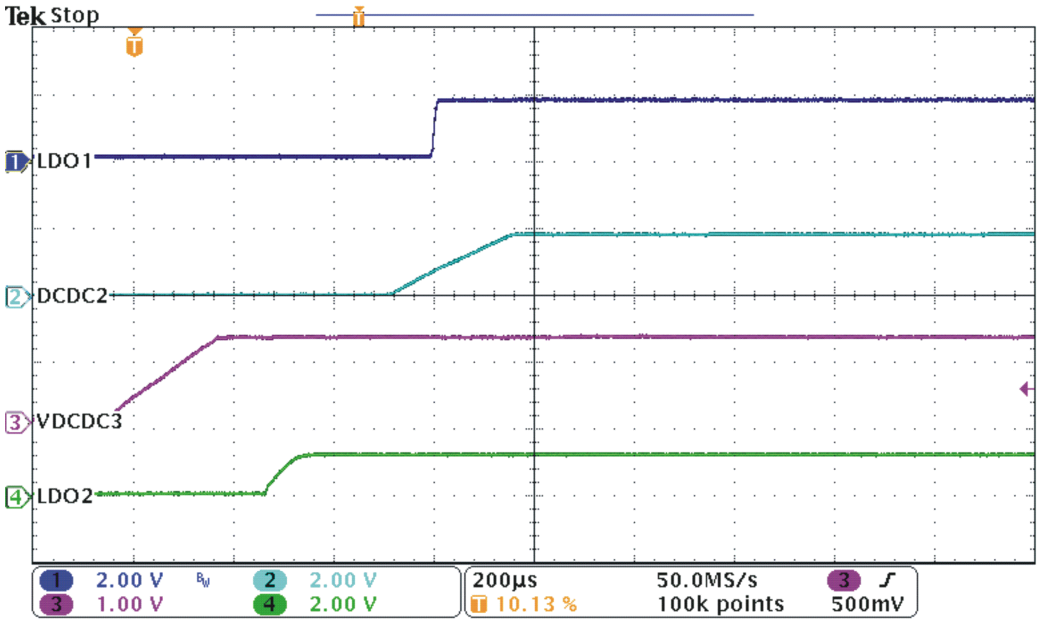


Figure 5. Startup of LDO1 and LDO2 (DCDC2 = 1.8 V)

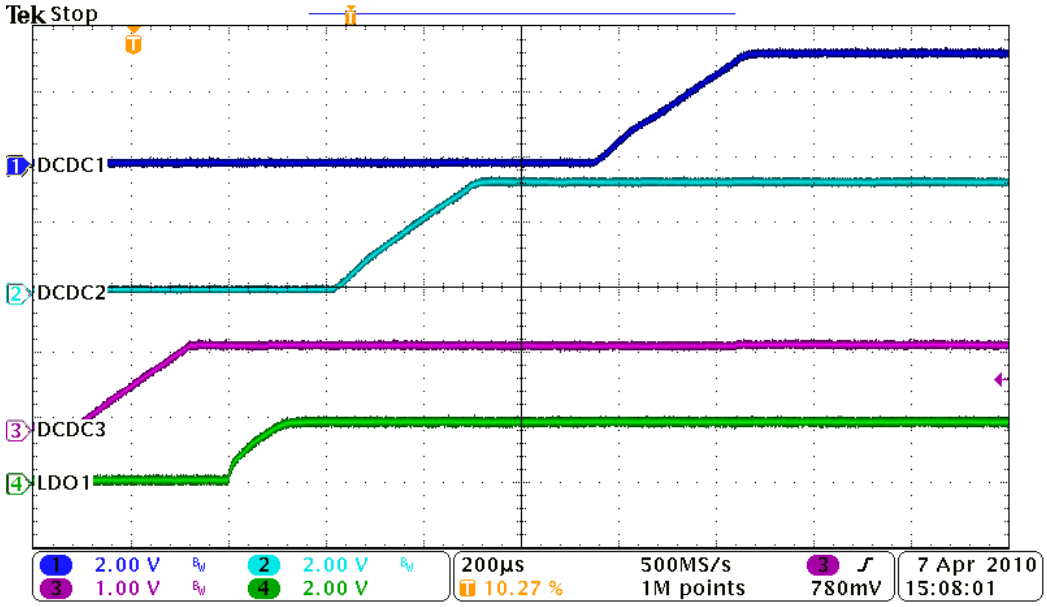


Figure 6. Startup of DC/DC Converters and LDO1 (DCDC2 = 3.3 V)

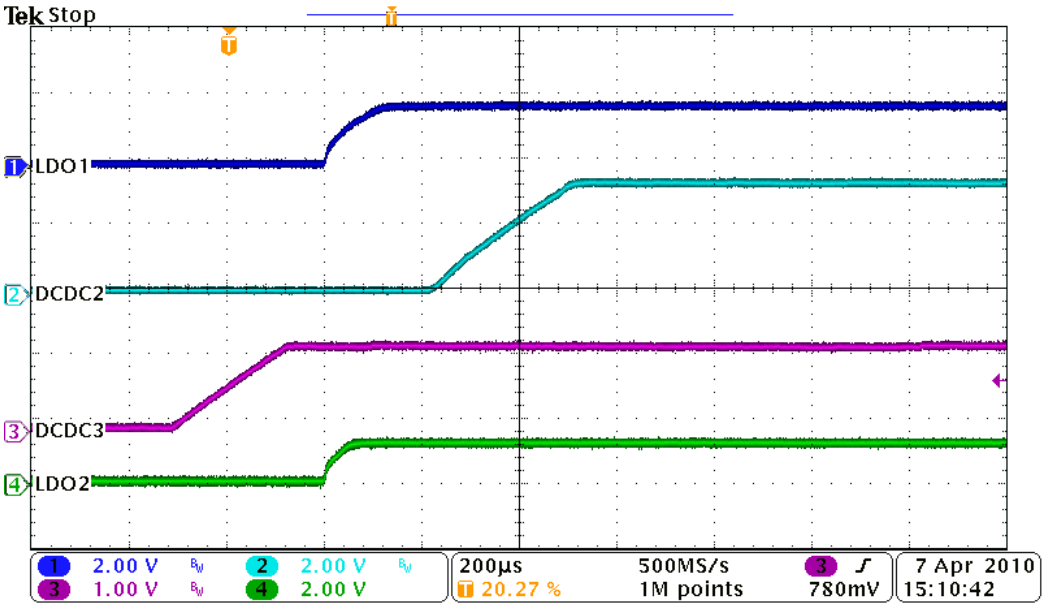


Figure 7. Startup of LDO1 and LDO2 (DCDC2 = 3.3 V)

Revision History

Changes from A Revision (April, 2010) to B Revision **Page**

- Changed document title to reflect relevant devices 1
- Updated references to *OMAP-L138* to include *OMAP-L132* devices 1
- Changed Figure 1 to show OMAP-L132 configuration; added footnote 4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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