Application Report
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Understanding LDO Dropout

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ABSTRACT

Not all low dropout (LDO) linear regulator data sheets provide the voltage dropout information needed for all applications. This application report shows a designer how to use an LDO data sheet's specified dropout performance to determine the dropout voltage at other operating conditions.

1 LDO Data Sheets

Most LDO data sheets provide both a typical and maximum specified dropout voltage. This information is found in the Electrical Characteristics table. Unfortunately, dropout is usually only specified at the LDO's maximum rated output current. Some data sheets provide a graph of typical dropout voltage vs current, but this graph only contains typical data that is not specified. Fortunately, the information that is available in the data sheet can be used to calculate specified voltage dropout at all operating currents.

2 Calculating LDO Dropout

First, it is necessary to understand what is happening to the LDO during dropout. A typical LDO has an n-channel or a p-channel FET pass element. The control circuitry modulates the gate of the FET so that it operates in the linear region. Figure 1 shows a typical FET V-I curve. An LDO that is operating with Vin = 5 V, Vout = 3.3 V, and an output current of 500 mA would be operating at point *A*. Note that the x-axis in the figure is the FET's drain-to-source voltage, which is Vin-Vout for an LDO. As the load current or input voltage changes, the control circuit changes the gate-to-source voltage to keep the output in regulation. Under steady-state conditions, the FET behaves like a resistor and simply drops voltage across its terminals. The FET has a minimum resistance that is shown by the Saturation Line in Figure 1. If the circuit conditions require that the FET operate with a lower resistance than the Saturation Line allows, the LDO is in dropout. The static FET resistance in this example is calculated by dividing the change in voltage by the change in current. The line extending from the origin through point *A* represents this resistance, 1.7 V/0.5 A, or 3.4 Ω. The Saturation Line in Figure 1 represents a resistance of 0.8 Ω. The LDO can operate anywhere to the right of the Saturation Line. For example, the same LDO with Vin = 4 V, Vout = 3.3 V, and Iout = 700 mA would operate at point *B*. This is 2.4 Ω, which is still to the right of the Saturation Line; so, the LDO is not in dropout. If the input voltage drops from 4 V to 3.8 V, the new operating point would be point *C*, which is to the left of the Saturation Line. At this point, the circuit requires that the LDO operate with a resistance of 0.71 Ω, but it can not go any lower than 0.8 Ω. The LDO is now operating in dropout.

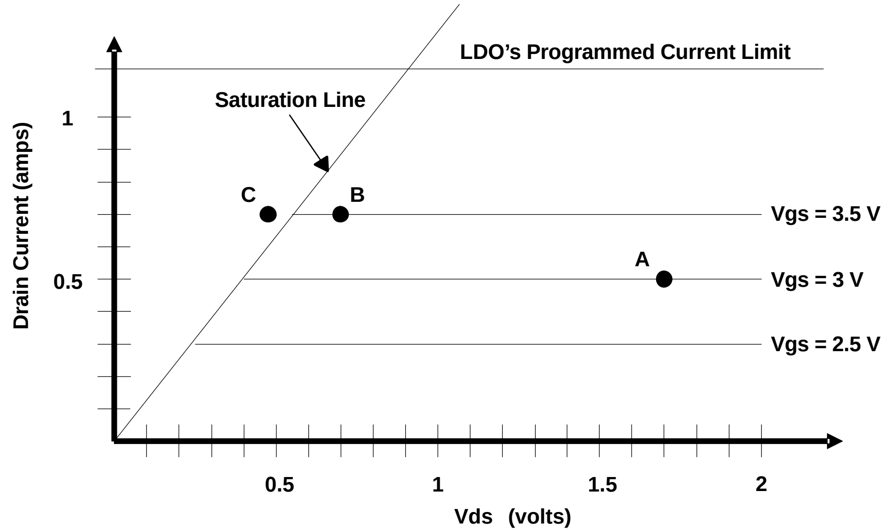

Figure 1. Typical FET V-I Graph

Some data sheets show a variation of the typical FET V-I curve shown in Figure 1 with the load current on the x-axis and the LDO dropout voltage on the y-axis. Figure 2 shows this graph for the 2.85-V option of the TPS79901 LDO. Most graphs like this are only typical data and are not specified over temperature or process variation. Also, the voltage option in the graph may not be the one of interest. In order to specify dropout, a worst case graph of Figure 2 is necessary. The Electrical Characteristics table provides the necessary information. Table 1 shows that the TPS79901 specified dropout is 160 mV at 200 mA for the 3.3-V option. This data point can be plotted and a line drawn between the origin and the data point. Using this graph, the user can determine the dropout voltage at any operating current. Note that the dropout voltage becomes extremely low when the LDO is operated at currents significantly lower than the rated maximum. The equivalent FET resistance is the dropout voltage divided by the test current, or 160 mV / 200 mA = 0.8 Ω for this LDO. The actual dropout voltage at any operating current is the FET resistance times the operating current. For example, if an application requires 100 mA from this LDO, the specified dropout voltage is 0.8 Ω× 100 mA = 80 mV. Note that this dropout voltage is slightly higher than the typical dropout voltage in Figure 2.

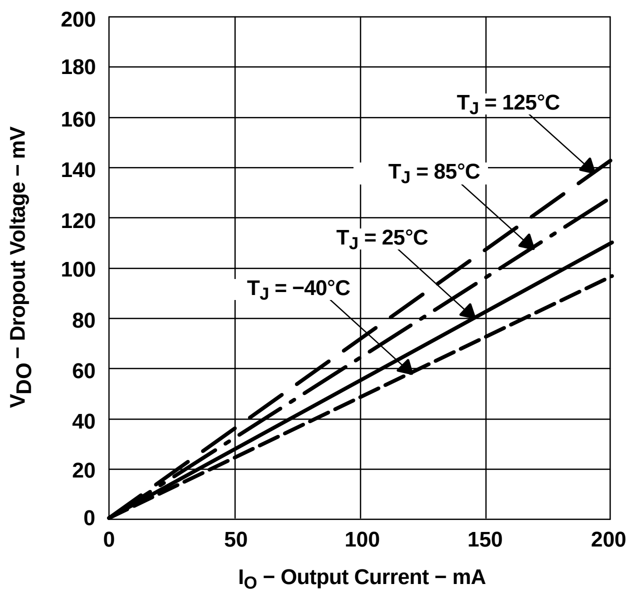

Figure 2. TPS799285 Dropout Voltage vs Output Current

Table 1. Dropout Voltage

				MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage ($V_{IN} = V_{OUT(NOM)} - 0.1$ V)	$V_{OUT} < 3.3$ V	$I_{OUT} = 200$ mA		100	175	mV
		$V_{OUT} \geq 3.3$ V			90	160	

To summarize the design procedure for determining the dropout voltage at currents not specified in the data sheet:

1. Calculate the LDO's minimum resistance

$$LDO_{min\_resistance} = \frac{Dropout\_Voltage}{Test\_Current} \quad (1)$$

2. Calculate the LDO's dropout at the operating current

$$LDO_{dropout} = LDO_{min\_resistance} \times Load\_Current \quad (2)$$

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