User's Guide

TPS92682EVM Constant Current and Constant Voltage SEPIC Controller

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ABSTRACT

This user's guide describes the specifications, board connection description, characteristics, operation, and use of the TPS92682-Q1 constant current (CC) and constant voltage (CV) mode in coupled inductor SEPIC configurations. The TPS92682-Q1 device implements a fixed-frequency peak current mode control technique with programmable switching frequency, slope compensation, and soft-start. Additional features include wide input voltage range (4.5 V to 65 V), programmable spread spectrum frequency modulation, programmable fault handling, and adjustable output current setting. A complete schematic diagram, printed circuit board layouts, and bill of materials are included in this document.

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Trademarks

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General Texas Instruments High Voltage Evaluation (TI HV EMV) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, it is always good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1 Description

The TPS92682EVM-125 solution provides a two channel, constant current and constant voltage coupled inductor SEPIC controller, which is configurable via serial peripheral interface (SPI). The EVM is designed to operate with an input voltage in the range of 7 V to 20 V. The EVM provides maximum output power of 15 W per channel. The TPS92682EVM-125 provides high efficiency, SPI programmable fault handling, I_{LED} setting, and spread-spectrum. The channel-1 of the EVM is configured as CV and channel-2 as CC mode.

1.1 Typical Applications

This document outlines the operation and implementation of the TPS92682-Q1 as a two-channel CV and CC coupled inductor SEPIC controller with the specifications listed in Table 3-1. For applications with a different input voltage range or different V_{OUT} or I_{LED} range, refer to the TPS92682-Q1 data sheet. The MSP-EXP432E401Y SimpleLink™ Ethernet MSP432E401Y MCU LaunchPad™ Development Kit controls the TPS92682EVM-125 evaluation board. The MSP-EXP432E401Y is available on TI website. However, any SPI controller can be used to program the TPS92682EVM board. Ensure that the LaunchPad board from TI has been programmed before running the GUI. The programming instructions are provided in Section 6.

1.2 Warnings

Observe the following precaution when using the TPS92682EVM-125 evaluation module.

Caution hot surface. Contact may cause burns. Do not touch.

1.3 Connector Description

Table 1-1 describes the connectors and Table 1-2 lists the test points on the EVM and how to properly connect, set up, and use the TPS92682EVM-125.Figure 1-1 shows the connection diagram and the default jumper locations of the TPS92682EVM-125.

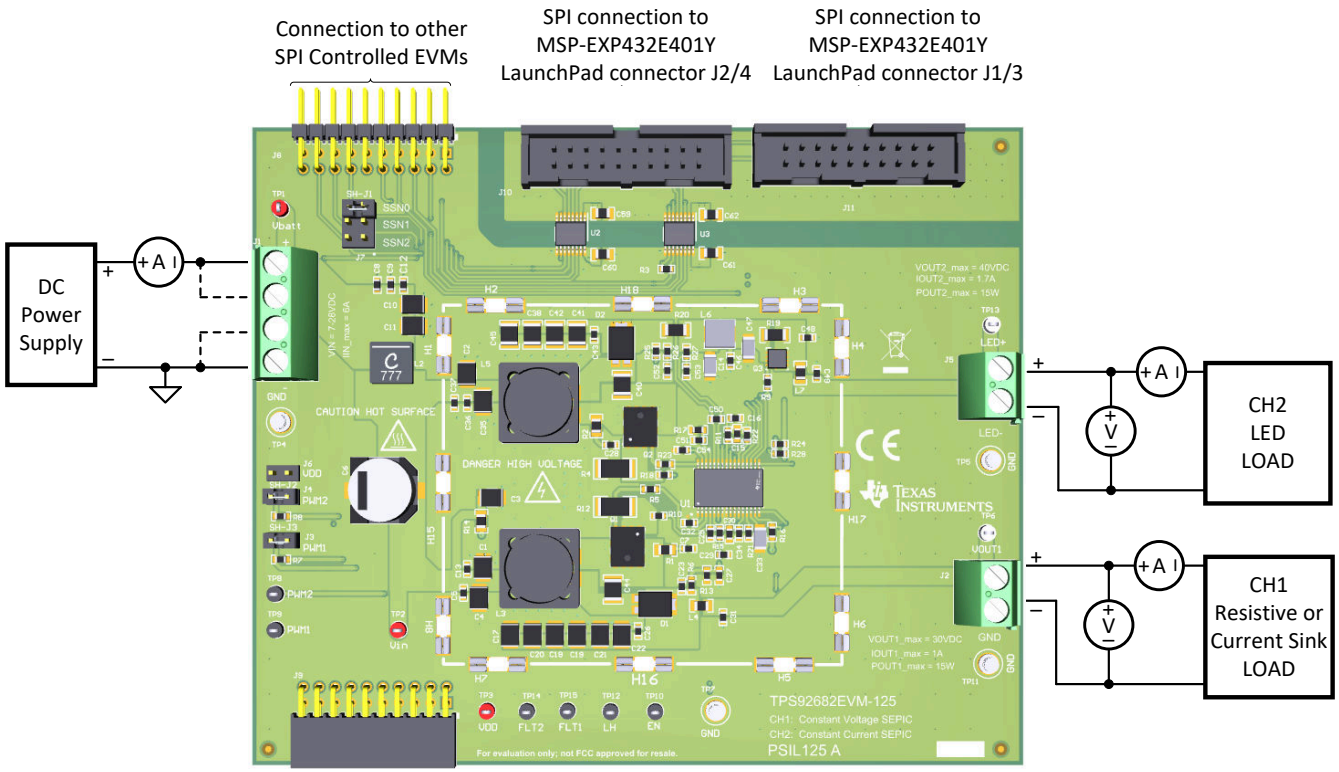


Figure 1-1. Component Connections

Table 1-1. Connector Descriptions

Connector	Label	Description
J10	SPI control from the MSP-EXP432E401Y LaunchPad	J10 and J11 allow attachment of a header cable for SPI control of the TPS92682-Q1 to the TI SimpleLink™ Ethernet MSP-EXP432E401Y MCU LaunchPad™ Development Kit, part number MSP-EXP432E401Y
J11		
J8	SPI control signals to other SPI controlled EVM	J8 and J9 allow star connection of TPS92682EVM-125 boards to each other with one MSP-EXP432E401Y control board.
J9		
J1	VIN, GND	J1 connects the input power to the TPS92682EVM-125. The board silkscreen identifies VIN pins with "Vbatt" and the "GND" markings.
J2	Channel-1 and Channel-2 and GND	J2 is connected to the channel-1 output and J5 is connected to the channel-2 output of the TPS92682EVM-125.
J5		
J6	VDD jumper	J6 is a jumper provided to share VDD with other SPI controlled EVM, in case a digital supply is needed. For the operation of this EVM, leave this jumper open.
J3	PWM1 and PWM2 jumpers	J3 and J4 are jumpers to apply external PWM signals to the two channels. When the jumpers are removed and the R28 and R29 resistors are installed, the PWM signals can be generated from the MSP-EXP432E401Y controller board. When the jumpers are populated (by default), the PWM1 and PWM2 pins of the TPS92682-Q1 are connected to VDD.
J4		
J7	SSN configuration jumper	J7 allows configuration of the SSN chip select line, when multiple chips on the same SPI bus are used. By default, evaluation module is configured to be connected to the SSN0 of the MSP-EXP432E401Y controller board.

Table 1-2. Test Points

Test Point	Description
Metal turrets	All metal turrets are grounds.
Vbatt	The VBAT test point allows for voltage measurement of the external power supply applied to the evaluation board.
Vin	The VIN test point allows for voltage measurement of the power applied to the boost and boost-to-battery channels after the EMI filter.
VDD	The VDD test point allows for voltage measurement of the VDD output of the TPS92682-Q1.
LH	The LH test point allows for applying a voltage to the LH pin and placing the TPS92682-Q1 in Limp Home mode

Table 1-2. Test Points (continued)

Test Point	Description
FLT1	The FLT1 test point can be used to monitor the fault occurrence of the channel-1. When a fault occurs, FLT1 voltage level goes low. Note that during power up, FLT1 is low (due to POR). The Fault pins can be reset by setting bit-7 of the EN register 0x00.
FLT2/SYNC	The FLT2 test point can be used to monitor the fault occurrence of the channel-2. When a fault occurs, FLT2 voltage level goes low. Note that during power up, FLT2 is low (due to POR). The Fault pins can be reset by setting bit-7 of the EN register 0x00. The FLT2 test point can also be used for synchronizing of the TPS92682-Q1 with an external clock.
EN	EN test point is connected to the EN-pin of the TPS92682-Q1 device
PWM1	PWM1 test point is connected to the PWM1-pin of the TPS92682-Q1 device
PWM2	PWM2 test point is connected to the PWM2-pin of the TPS92682-Q1 device
LED+	The LED+ test point allows for voltage measurement of the channel-2 LED positive output.
LED-	The LED- test point is connected to the channel-2 LED negative output. This test point is connected to the EVM ground plane
Vout1	The Vout1 test point is connected to the channel-1 CV regulator.

2 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one substance of very high concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1-ton per year. The SVHC specifications include the following:

Component Manufacturer	Component part number	SVHC Substance	SVHC CAS (when available)
PHOENIX CONTACT GmbH & Co. KG	1715721 and 1715747	Lead (Pb)	7439-92-1

3 Performance Specifications

This section provides the performance specifications and requirements for the CV and CC coupled inductor SEPIC controller.

3.1 SEPIC Voltage Regulator

Table 3-1 provides the EVM electrical performance specifications for the SEPIC voltage regulator, channel-1.

Table 3-1. TPS92682EVM-125 Channel-1 CV Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage, V_{IN}		7	12	28	V
Maximum Input Current, I_{IN}				2.7	A
Output Characteristics					
Output voltage V_{OUT}	VOUT+ to GND			30	V
Maximum output current, I_{LED}				1	A
Maximum Output Power, P_{OUT}				15	W
Systems Characteristics					
Switching frequency F_{SW}			400		kHz
Dither modulation f_{DM}		400		600	Hz

3.2 SEPIC Current Regulator

Table 3-2 provides the EVM electrical performance specifications for the SEPIC current regulator, channel-2.

Table 3-2. TPS92682EVM-125 Channel-2 CC Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage, V_{IN}		7	12	28	V

Table 3-2. TPS92682EVM-125 Channel-2 CC Performance Specifications (continued)

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
Maximum Input Current, I_{IN}				2.7	A
Output Characteristics					
LED forward voltage, $V_{F(LED)}$		2.8	3.0	3.2	V
Number of LEDs N_{LED}				12	
Output voltage V_{OUT}	LED+ to LED–			40	V
Maximum output current, I_{LED}				1.7	A
Maximum Output Power, P_{OUT}				15	W
PWM dimming frequency f_{PWM}			400		Hz
Systems Characteristics					
Switching frequency F_{SW}			400		kHz
Dither modulation f_{DM}		400		600	Hz
Output over-voltage threshold $V_{O(OV)}$				45	V

4 Performance Data and Typical Characteristic Curves

Figure 4-1 and Figure 4-2 show the efficiency results for the CC and CV channels of the coupled inductor SEPIC controller. The results are shown for different input voltage V_{IN}. It is important to note that the efficiency results include the power loss in the input EMI filter.

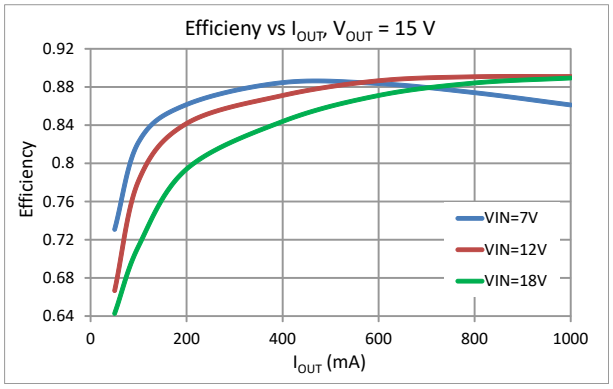


Figure 4-1. CV SEPIC Efficiency for V_{OUT} = 15 V

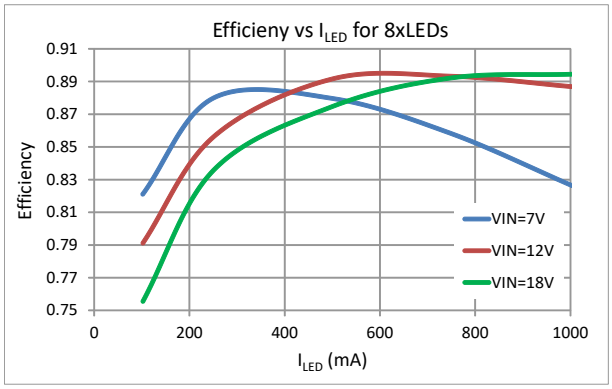


Figure 4-2. CC SEPIC Efficiency for V_{OUT} = 22 V

4.1 Startup Waveforms

Figure 4-3 and Figure 4-4 show the startup waveforms for the CC and CV channels of the TPS92682EVM-125. Channel-1: V_{OUT} is set to 30 V and a resistive load of 60 Ω is connected to the output. Channel-2: A string of 5×LEDs are connected to the output. The LED current is set to 1 A.

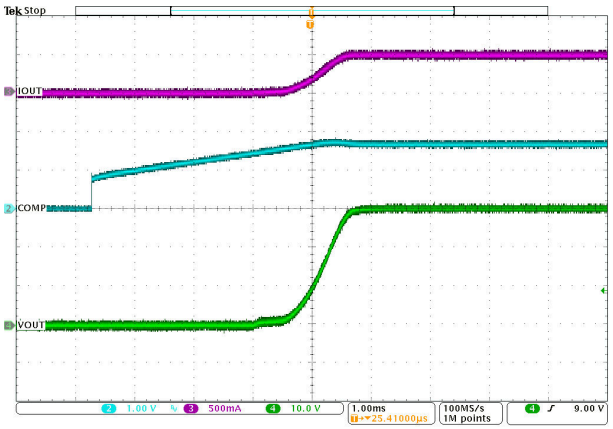


Figure 4-3. CV SEIPC Softstart Waveform, CH1SS3:0 = 7

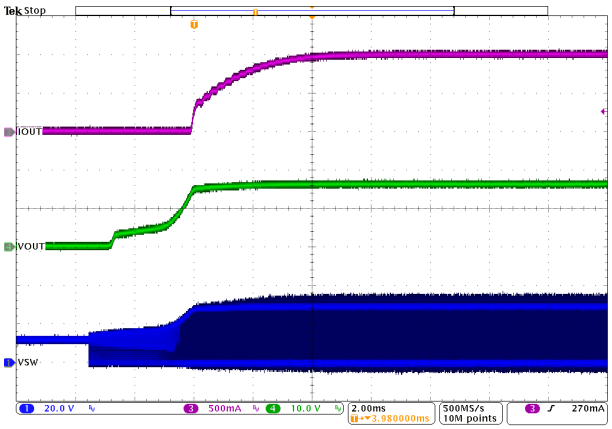
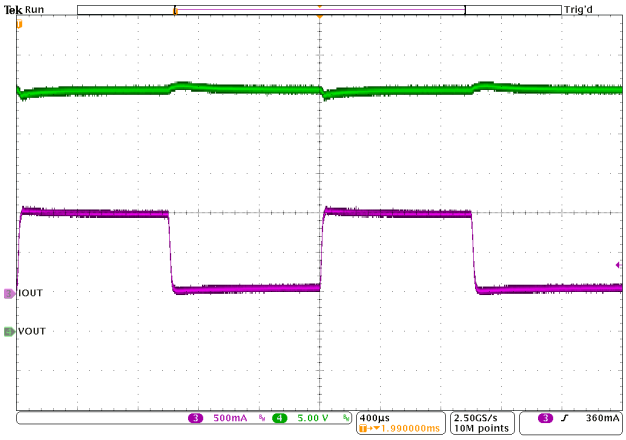


Figure 4-4. CC SEPIC Softstart Waveform, CH2SS3:0 = 15

4.2 Dynamic Performance

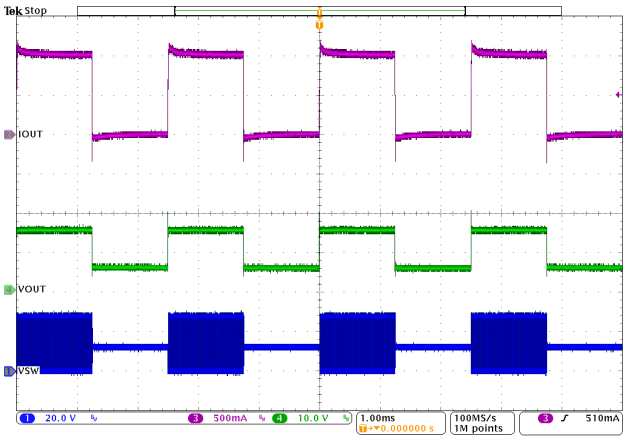
Figure 4-5 shows the load transient on the output of the CV channel-1. VOUT is set to 30 V and the output current is changed from 50mA to 1 A. The overshoot and undershoot caused by load transient is less than 1 V.



V_{IN} = 12 V

Figure 4-5. CV SEPIC Load Transient Performance

Figure 4-6 shows PWM dimming of the CC channel-2. The I_{LED} is programmed to 1A. A string of 5×LEDs are connected to the output of the channel-2. Internal PWM dimming is used and the frequency is set to 400 Hz.



V_{IN} = 12 V

Figure 4-6. CC SEPIC PWM Dimming Performance

4.3 Faults

TPS92682-Q1 include various fault handling and diagnostic features. Figure 4-7 and Figure 4-8 show the LED short and LED open protection for CC SEPIC channel.

As shown in Figure 4-7, when a short across the LED load occurs, Under Voltage protection is triggered (if UV Fault is enabled), the COMP-pin is pulled low, and the associated channel is turned off. The channel remains off for the programmed main fault timer (MFT). When the MFT count completes, channel performs a soft-start sequence. The CC SEPIC can regulate the output current into an output short. If there is a continuous short on the output, UV fault is triggered, when the soft-start ramp completes. UV is disabled during soft-start ramp. If the output short is removed, the controller continues regulating current into the LEDs on the output. In the test in Figure 4-7, output PFET is removed.

As shown in Figure 4-8, when open LED load occurs, the load voltage increases above the programmed overvoltage (OV) threshold, and the associated channel turns off. The channel remains off until the load voltage

drops below a OV hysteresis value, when the channel performs a soft-start sequence. Set the OV threshold by programming the OV register and the adjusting the resistor divider connected to the FB2/OV2 pin.

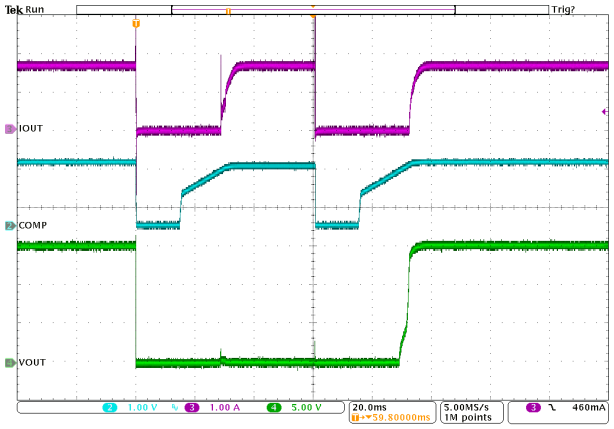


Figure 4-7. CC SEPIC LED Output Short

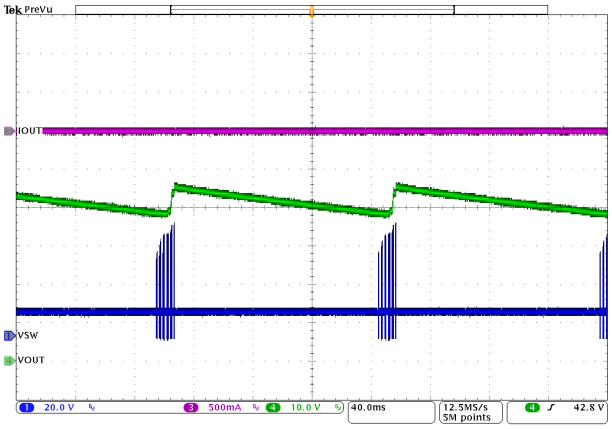
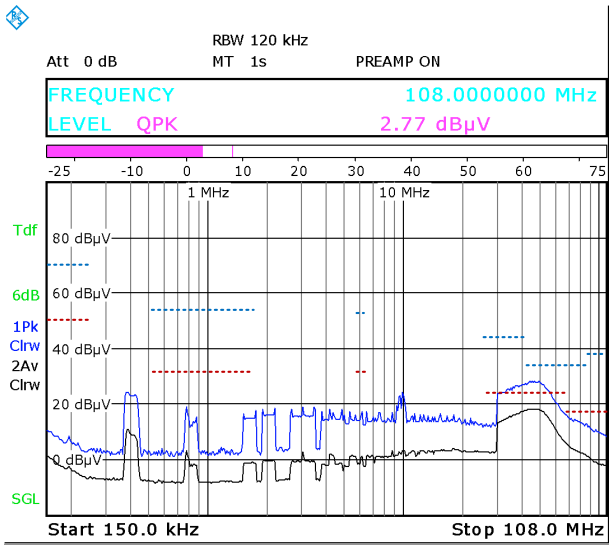


Figure 4-8. CC SEPIC LED Open and Over-Voltage Protection

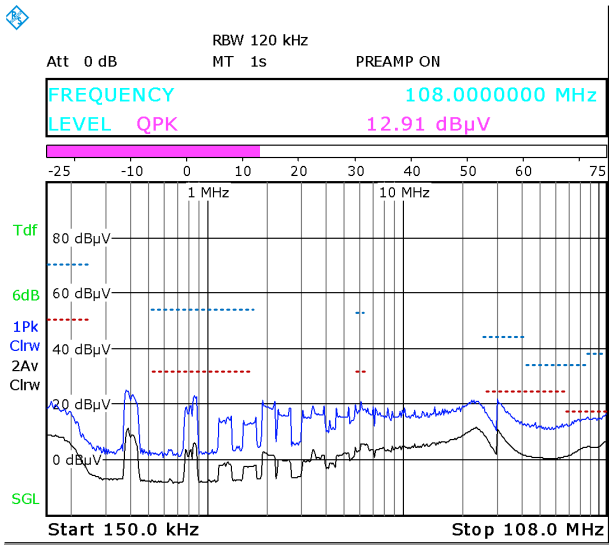
4.4 EMI Scan

Figure 4-9 shows the conducted EMI for the CV channel-1 with 38 Ω resistive load, and V_{OUT} set to 24 V (P_{OUT} = 15 W). Figure 4-10 shows the conducted EMI for the CC channel-2 with 10 series connected LED load and I_{LED} = 500 mA.



V_{IN} = 12 V, FMMAG = 2, FMFREQ = 5

Figure 4-9. CV SEPIC EMI Scan



V_{IN} = 12 V, FMMAG = 2, FMFREQ = 5

Figure 4-10. CC SEPIC EMI Scan

5 Schematic, PCB Layout, and Bill of Materials

This section contains TPS92682EVM-125 schematic, PCB layout, and bill of material (BOM).

5.1 Schematic

Figure 5-1 illustrates the TPS92682EVM-125 schematic.

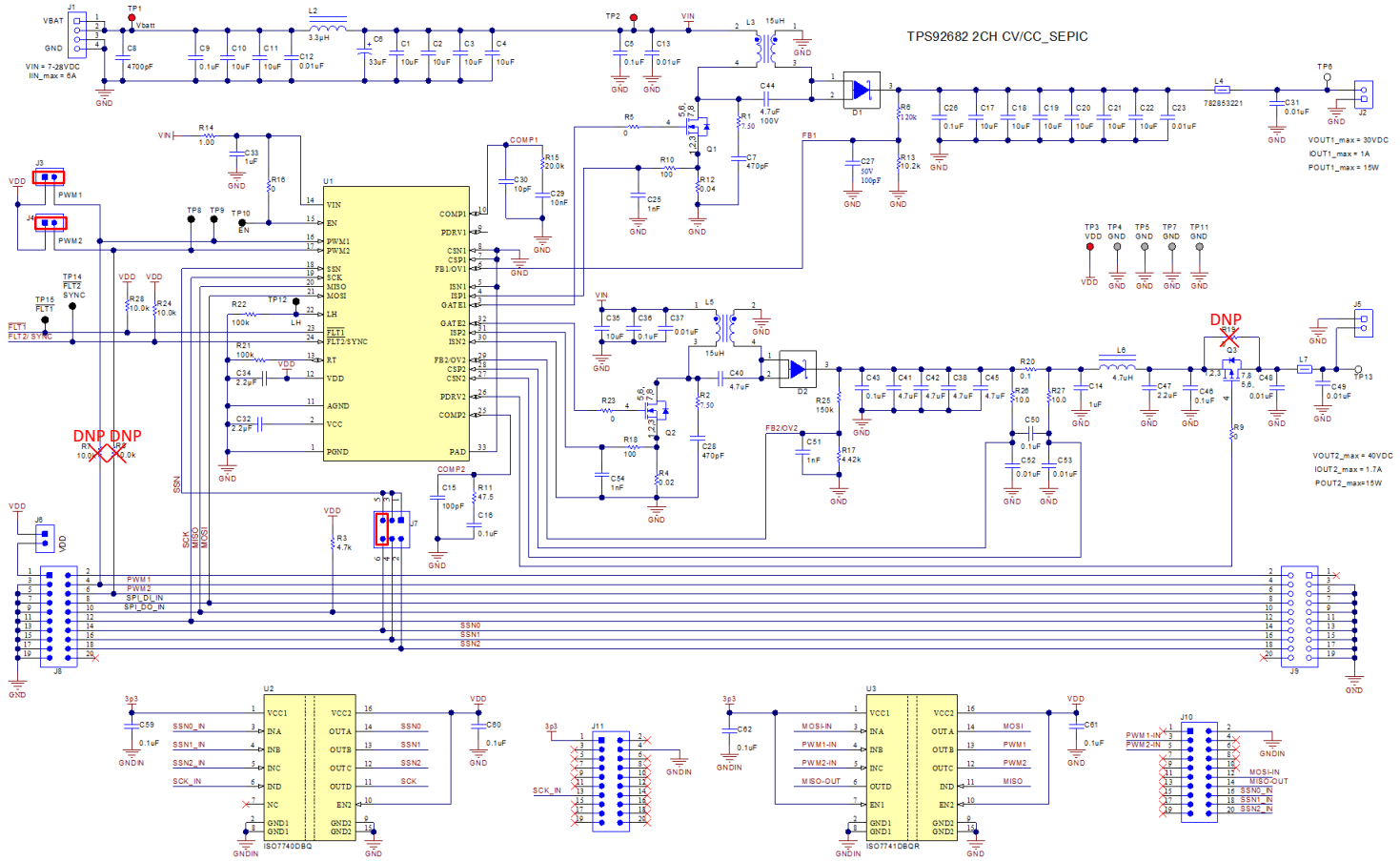


Figure 5-1. TPS92682EVM-125 Schematic

5.2 Layout

The TPS92682EVM-125 is a four-layer board. Figure 5-2, Figure 5-3, Figure 5-4, Figure 5-5, and Figure 5-6 illustrate the assembly, the top, the inner-layer1, the inner-layer2 and the bottom layer of the TPS92682EVM-125 PCB layout.

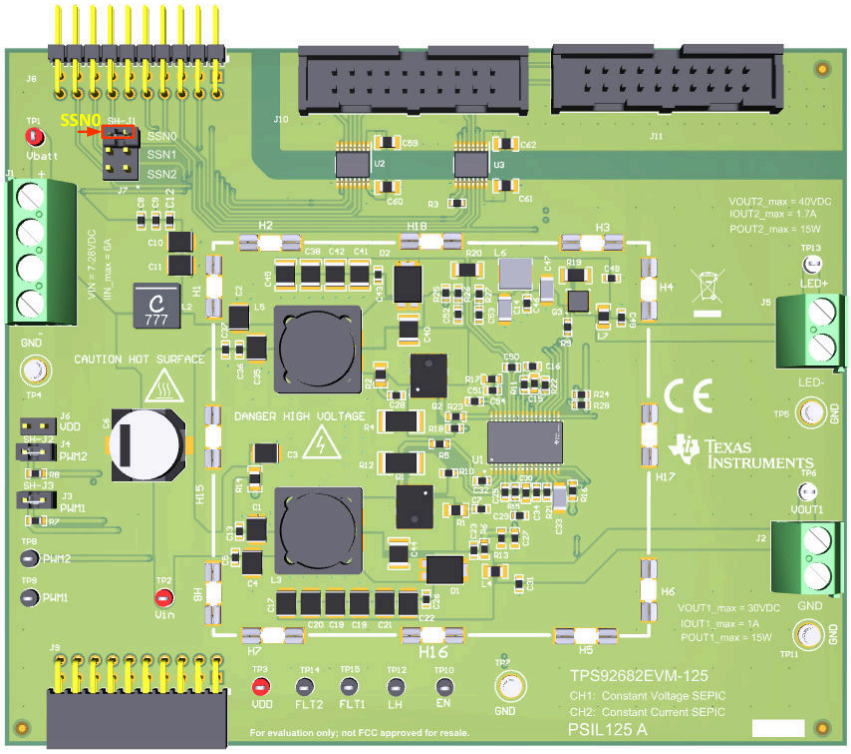


Figure 5-2. TPS92682EVM-125 Assembly

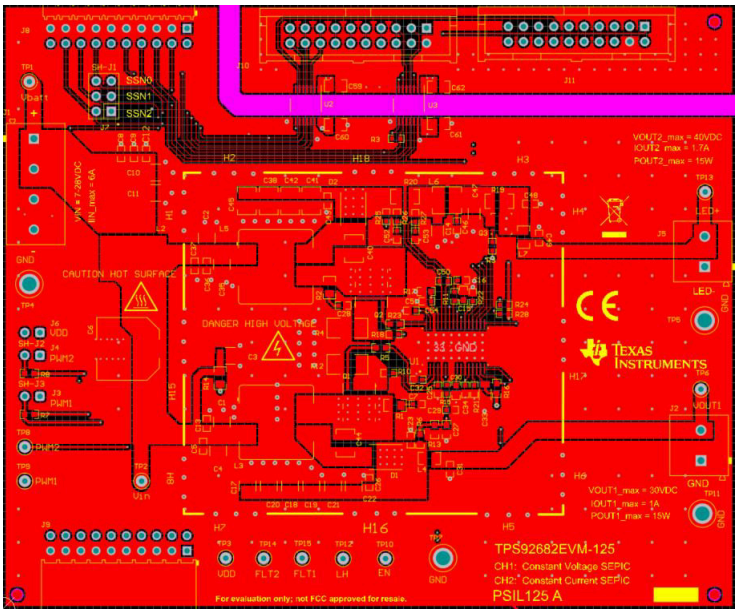


Figure 5-3. TPS92682EVM-125 Top Layer and Top Overlay (Top View)

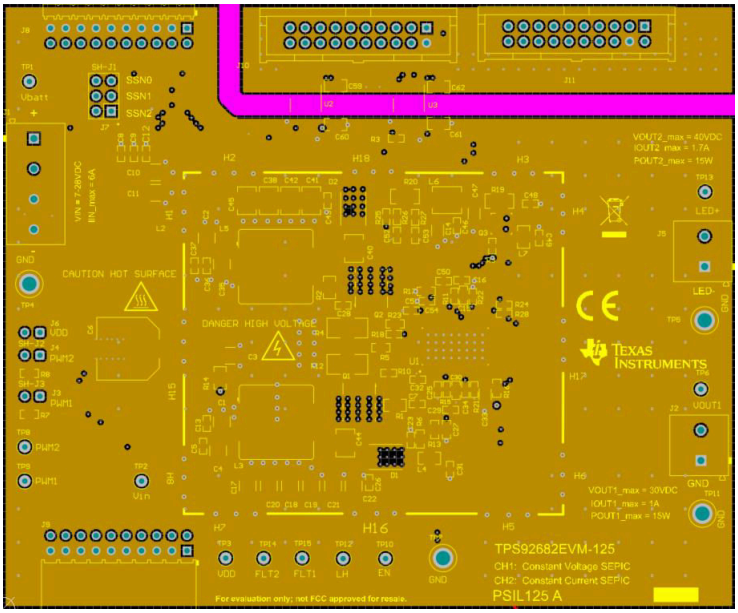


Figure 5-4. TPS92682EVM-125 Inner-layer 1

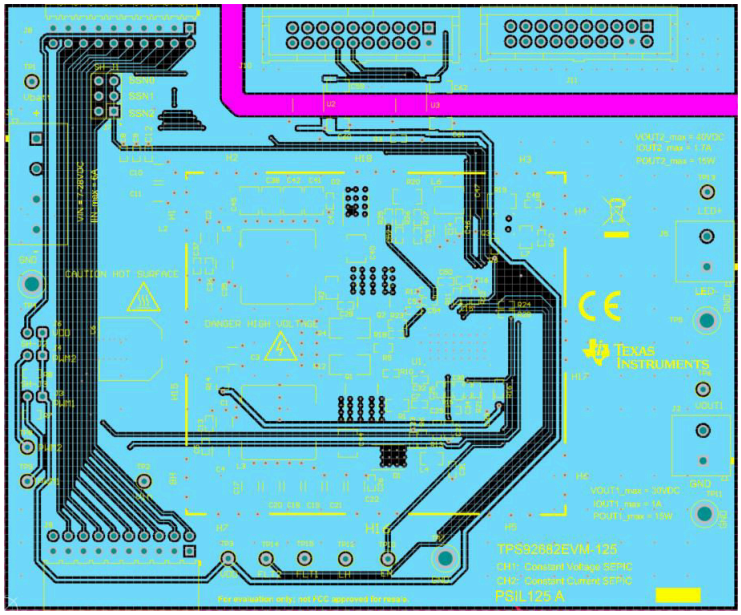


Figure 5-5. TPS92682EVM-125 Inner-layer 2

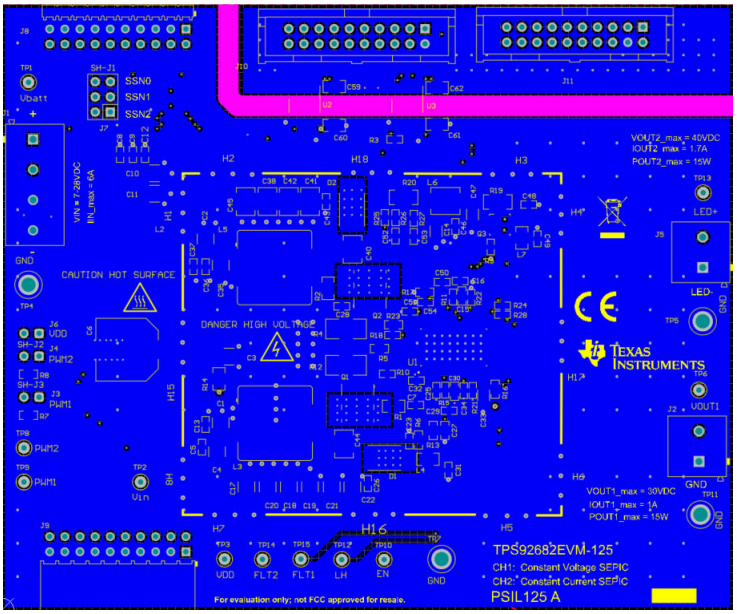


Figure 5-6. TPS92682EVM-125 Bottom Layer (Bottom View)

5.3 Bill of Materials

Table 5-1 lists the TPS92682EVM-125 bill of materials.

Table 5-1. TPS92682EVM-125 Bill of Materials

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
C1, C2, C3, C4, C10, C11, C17, C18, C19, C20, C21, C22, C35	13	10 µF	CAP, CERM, 10 uF, 50 V, ±20%, X7R	1210	C3225X7R1H106M250AC	TDK
C5, C9, C26, C36, C43, C46, C50	7	0.1 µF	CAP, CERM, 0.1 uF, 100 V, ±10%, X7S	0603	C1608X7S2A104K080AB	TDK
C12, C13, C23, C29, C31, C37, C48, C49, C52, C53	10	0.01 µF	CAP, CERM, 0.01 uF, 100 V, ±10%, X7R, AEC-Q200 Grade 1	0603	CGA3E2X7R2A103K080AA	TDK
C6	1	33 µF	CAP, AL, 33 uF, 100 V, ±20%, AEC-Q200 Grade 2, SMD	D10xL10mm	MAL215097904E3	Vishay
C7, C28	2	470 pF	CAP, CERM, 470 pF, 50 V, ±10%, X7R	0603	C0603X471K5RACTU	Kemet
C8	1	4700 pF	CAP, CERM, 4700 pF, 100 V, ±10%, X7R, AEC-Q200 Grade 1	0603	CGA3E2X7R2A472K080AA	TDK
C25, C51, C54	3	1000 pF	CAP, CERM, 1000 pF, 100 V, ±10%, X7R	0603	C1608X7R2A102K080AA	TDK
C38, C41, C42, C45	4	4.7 µF	CAP, CERM, 4.7 uF, 100 V, ±10%, X7S	1210	C3225X7S2A475K200AB	TDK
C40, C44	2	4.7 µF	CAP, CERM, 4.7 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1	1210	CGA6M3X7S2A475K200AB	TDK
C27	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 0	0603	CGA3E2NP01H101J080AA	TDK
C15	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0	0603	885012006057	Wurth Elektronik
C33	1	1 µF	CAP, CERM, 1 uF, 100 V, ±10%, X7R	1206	CL31B105KCHNNNE	Samsung
C14	1	1 µF	CAP, CERM, 1 uF, 100 V, ±10%, X7R, AEC-Q200 Grade 1	1206	CGA5L2X7R2A105K160AA	TDK
C32, C34	2	2.2 µF	CAP, CERM, 2.2 uF, 16 V, ±10%, X7R	0603	EMK107BB7225KA-T	Taiyo Yuden
C47	1	2.2 µF	CAP, CERM, 2.2 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1, 1206	1206	CGA5L3X7S2A225K160AB	TDK
C16	1	0.1 µF	CAP, CERM, 0.1 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1	0603	CGA3E3X7S2A104K080AB	TDK
C59, C60, C61, C62	4	0.1 µF	CAP, CERM, 0.1 uF, 50 V, ±10%, X7R	0805	C0805C104K5RACTU	Kemet
C30	1	10 pF	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 1	0603	CGA3E2C0G1H100D080AA	TDK
D1, D2	2	100 V	Diode, Schottky, 100 V, 3 A, AEC-Q101	POWERDI5	PDS3100Q-13	Diodes Inc

Table 5-1. TPS92682EVM-125 Bill of Materials (continued)

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
H1, H2, H3, H4, H5, H6, H7, H8, H15, H16, H17, H18	12		RFI SHIELD CLIP TIN SMD		S2711-46R	Harwin
J1	1		Terminal Block, 5.08 mm, 4x1, TH	4POS Terminal Block	1715747	Phoenix Contact
J2, J5	2		Terminal Block, 5.08 mm, 2x1, TH	2POS Terminal Block	1715721	Phoenix Contact
J3, J4, J6	3		Header, 100 mil, Gold, TH	2x1	TSW-102-07-G-S	Samtec
J7	1		Header, 100 mil, Gold, TH	3x1	TSW-103-07-G-D	Samtec
J8	1		Header, 2.54 mm, Tin, R/A, TH	10x2	TSW-110-08-T-D-RA	Samtec
J9	1		Receptacle, 2.5 mm, Gold, R/A, TH	10x2	SSW-110-02-G-D-RA	Samtec
J10, J11	2		Header (shrouded), 100 mil, Gold, TH	10x2	5103309-5	TE Connectivity
L2	1	3.3 µH	Inductor, Shielded, Composite, 3.3 µH, 8 A, 0.02081 Ω, AEC-Q200 Grade 1, SMD	6.4x3.1x6.6	XAL6030-332MEB	Coilcraft
L3, L5	2	15 µH	Coupled Inductor, 15 µH, 6.5 A, 0.0355 Ω	12.5x 12.5mm	B82477D4153M000	TDK
L4, L7	2	220Ω	Ferrite Bead, 220 ohm @ 100 MHz, 2 A	0805	782853221	Wurth Elektronik
L6	1	4.7 µH	Inductor, Shielded Drum Core, Powdered Iron, 4.7 µH, 1.7 A, 0.095 Ω	4.7x4.3mm	IHLP1616BZER4R7M11	Vishay
Q3	1	- 60 V	MOSFET, P-CH, -60 V, -3.6 A	PowerPAK 1212	SI7415DN-T1-GE3	Vishay
Q1, Q2	2	100 V	MOSFET, N-CH, 100 V, 20 A, AEC-Q101	8-PowerVDFN	STL8N10LF3	STMicroelectronics
R1, R2	2	7.5 Ω	RES, 7.5, 1%, 0.125 W, AEC-Q200 Grade 0	0805	CRCW08057R50FKEA	Vishay
R3	1	4.7 kΩ	RES, 4.7k, 5%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06034K70JNEA	Vishay
R4	1	20 mΩ	RES, 0.02, 1%, 1 W	2010	CSRN2010FK20L0	Stackpole Electronics
R5, R9, R16, R23	4	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06030000Z0EA	Vishay
R6	1	120 kΩ	RES, 120 k, 0.1%, 0.1 W	0603	RT0603BRD07120KL	Yageo
R26, R27	2	10 Ω	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060310R0FKEA	Vishay
R10, R18	2	100 Ω	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW0603100RFKEA	Vishay
R12	1	40 mΩ	RES, 0.04, 1%, 1 W	2010	CSRN2010FK40L0	Stackpole
R14	1	1.0 Ω	RES, 1.00, 1%, 0.125 W, AEC-Q200 Grade 0	0805	CRCW08051R00FKEA	Vishay
R21, R22	2	100 kΩ	RES, 100k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW0603100KFKEA	Vishay
R24, R28	2	10 kΩ	RES, 10k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060310K0FKEA	Vishay
R25	1	150 kΩ	RES, 150 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW0603150KFKEA	Vishay
R17	1	4.42 kΩ	RES, 4.42k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06034K42FKEA	Vishay
R11	1	47.5 Ω	RES, 47.5, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060347R5FKEA	Vishay

Table 5-1. TPS92682EVM-125 Bill of Materials (continued)

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
R13	1	10.2 kΩ	RES, 10.2k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060310K2FKEA	Vishay
R15	1	20 kΩ	RES, 20k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	ERJ-3EKF2002V	Panasonic
R20	1	0.1 Ω	RES, 0.1, 1%, 0.5 W, AEC-Q200 Grade 1	1206	UR73V2BTTDR100F	KOA Speer
SH-J1, SH-J2, SH-J3	3		Shunt, 2.54mm, Gold, Black	2x1, 2.54mm	60900213421	Wurth Elektronik
TP1, TP2, TP3	3		Test Point, Miniature, Red, TH	TH	5000	keystone
TP4, TP5, TP7, TP11	4		Terminal, Turret, TH, Double	Turret	1502-2	keystone
TP6, TP13	2		Test Point, Miniature, White, TH	TH	5002	keystone
TP8, TP9, TP10, TP12, TP14, TP15	6		Test Point, Miniature, Black, TH	TH	5001	keystone
U1	1		Dual Channel Constant Voltage and Constant Current Controller with SPI Interface, DAP (HTSSOP-32)	HTSSOP32	TPS92682QDAPQ1	Texas Instruments
U2	1		High-Speed, Low-Power, Robust EMC Quad-Channel Digital Isolator, DBQ0016A (SSOP-16)	DBQ0016A	ISO7740DBQ	Texas Instruments
U3	1		High Speed, Robust EMC Quad-Channel Digital Isolators, DBQ0016A (SSOP-16)	DBQ0016A	ISO7741DBQR	Texas Instruments

6 Software

This section describes the installation of the GUI software and the drivers needed to operate the TPS92682EVM-125.

6.1 Demonstration Kit Software Installation for MSP-EXP432E401Y LaunchPad Board

1. Right-click on *TPS92682 LaunchPad Evaluation Software Installer.exe* and select **Run As Administrator**.
2. *Windows Account Control* asks to allow the program to make changes to the computer. Click **Yes**.
3. Select **Agree** to the installation license terms and install in the recommended location.
4. Installation may take a while, as it may need to install Microsoft .NET Framework.
5. If the installer asks to reboot after installing Microsoft .NET, click **restart later** to complete the driver installation.
6. After running the *TPS92682 LaunchPad Evaluation Software Installer.exe*, the evaluation software window appears as shown in Figure 6-1.

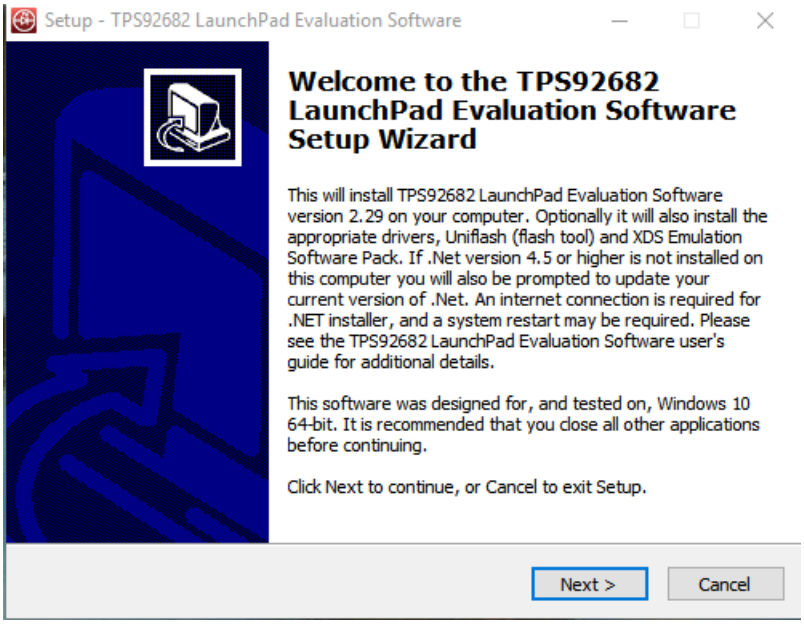


Figure 6-1. Setup Screen 1

Click **Next >** to install.

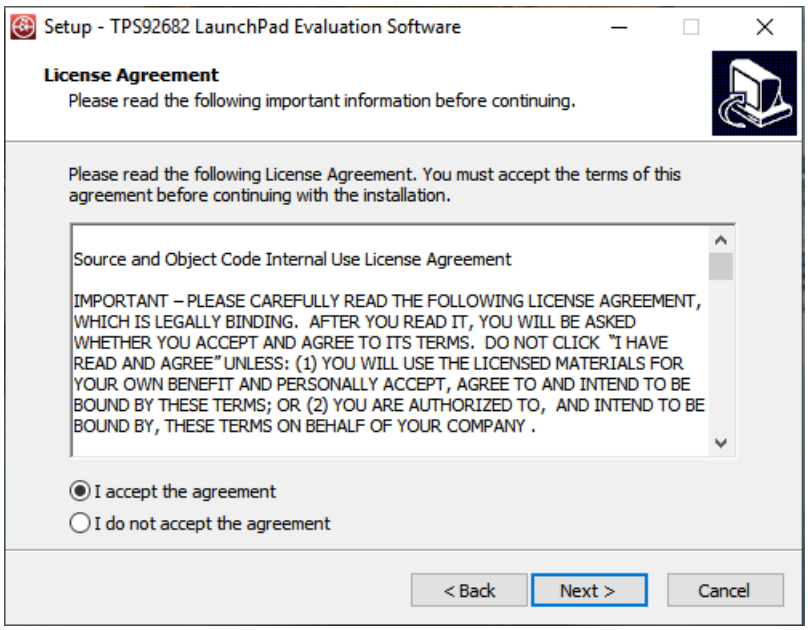


Figure 6-2. Setup Screen 2

Click **Next >** to accept the License Agreement.

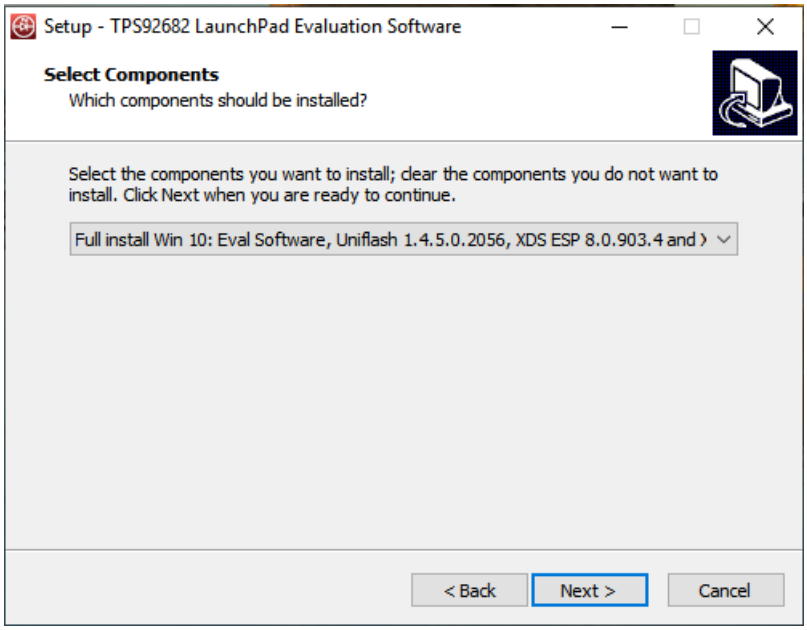


Figure 6-3. Setup Screen 3

Select **Full Install** and click **Next >** to install the evaluation software, the UniFlash, and the required XDS drivers. Full installation for both Windows 10 and 7 are provided.

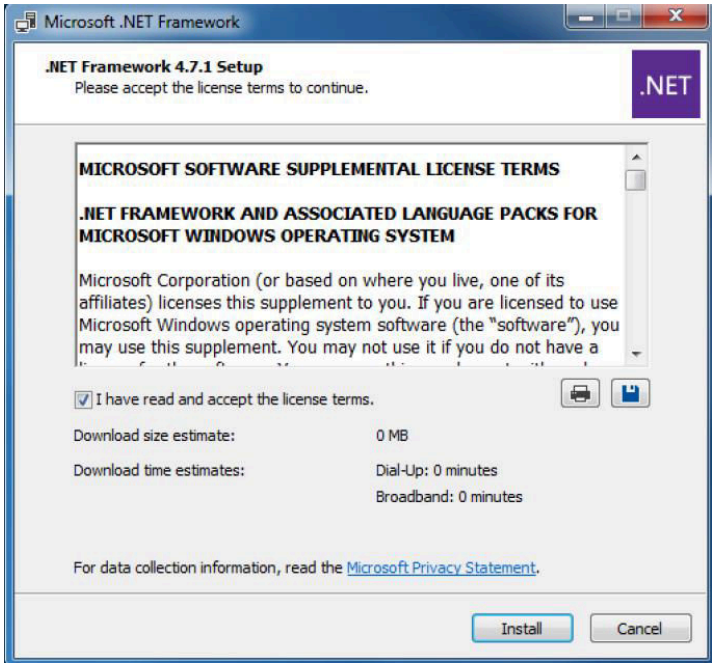


Figure 6-4. Setup Screen 4

If .NET Framework 4.5 or higher does not exist on the computer, the .NET Framework installation begins. Installation of .NET Framework will take several minutes. If .NET Framework 4.5 or higher exists on the computer, the installation jumps to the XDS driver installation.

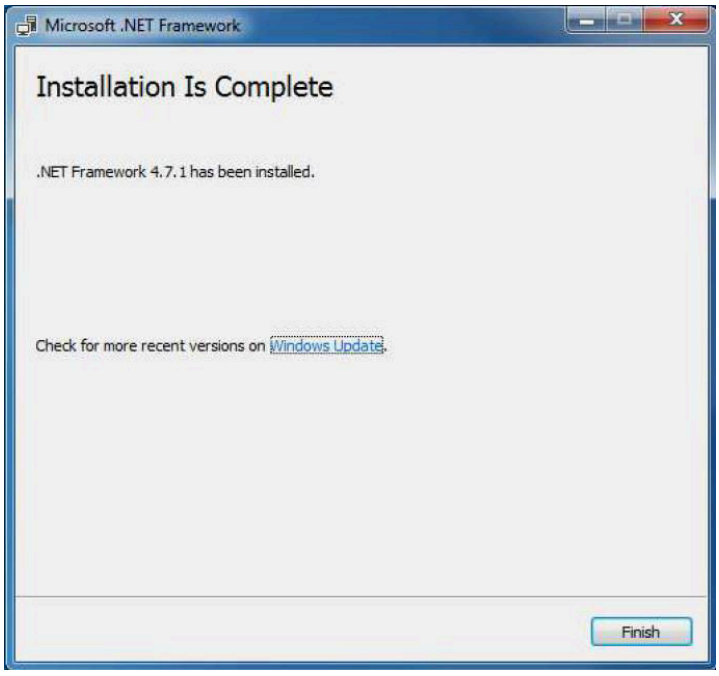


Figure 6-5. Setup Screen 5

A window appears indicating the completion of the .NET Framework installation.

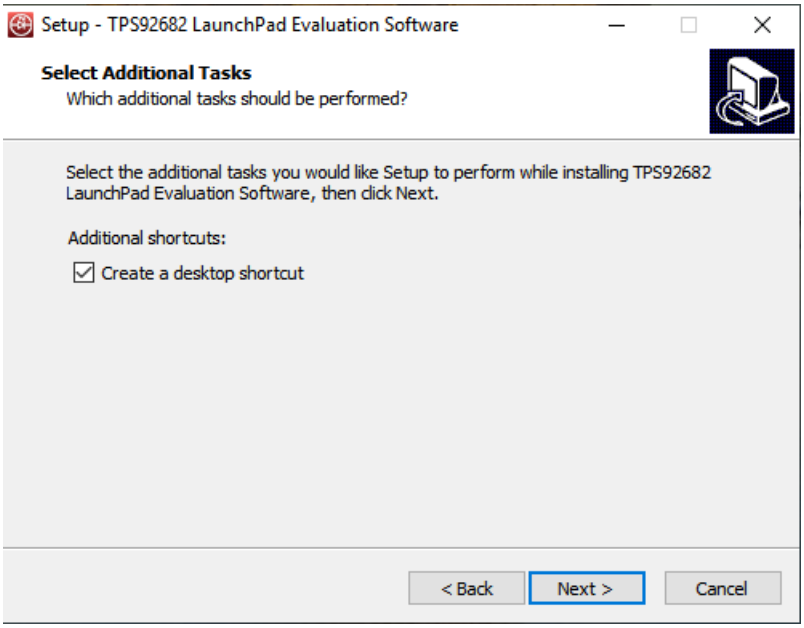


Figure 6-6. Setup Screen 6

Click **Next >** to continue the installation.

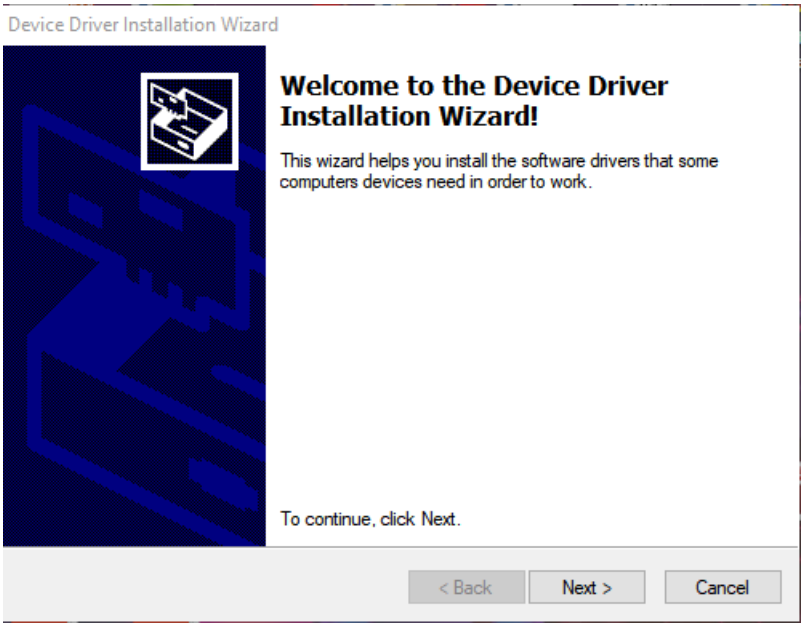


Figure 6-7. Setup Screen 7

Click **Next >** to install the XDS driver.

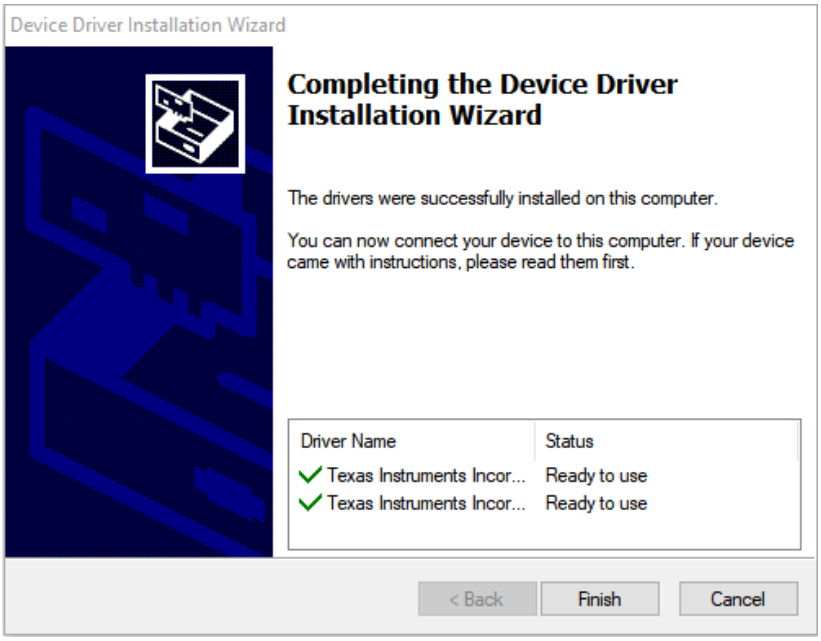


Figure 6-8. Setup Screen 8

The completion of the XDS driver installation is shown in Figure 6-8.

The TI-Emulators installation starts at this point. This will install the necessary drivers for running the application. In the next few steps as shown in Figure 6-9, Figure 6-10 and Figure 6-11 click **Next >** to perform the installation.

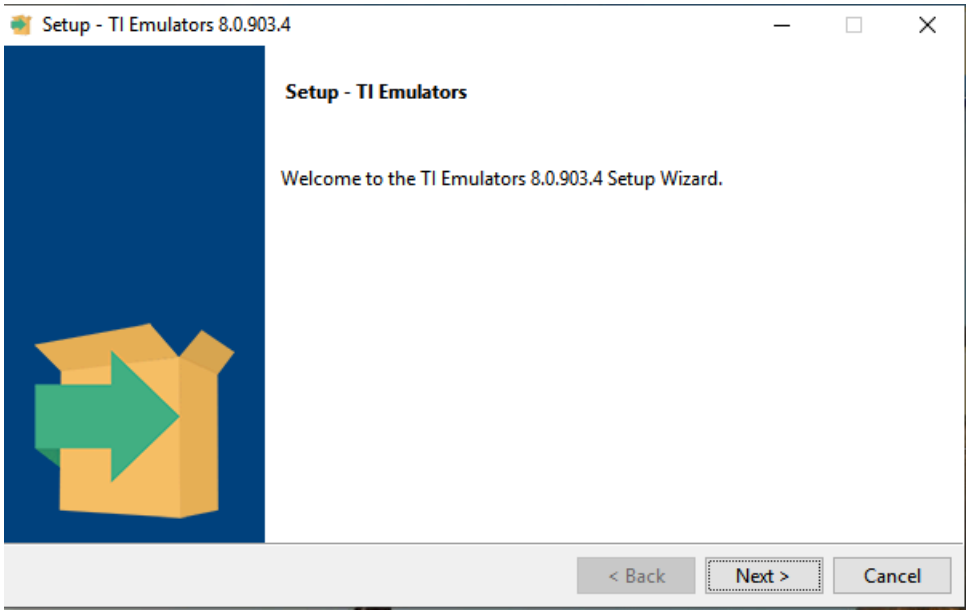


Figure 6-9. Setup Screen 9

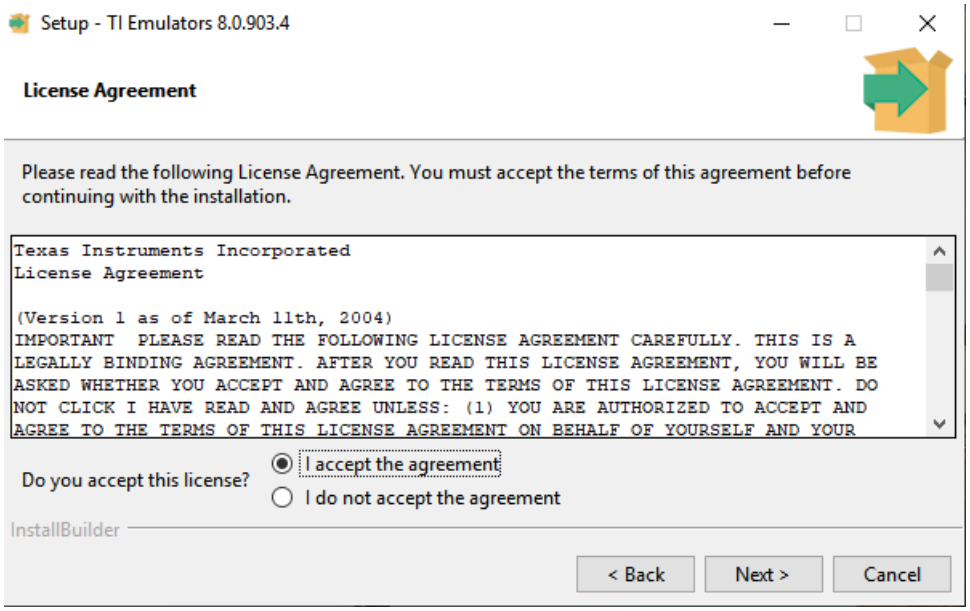


Figure 6-10. Setup Screen 10

Accept the license agreement in Figure 6-10.

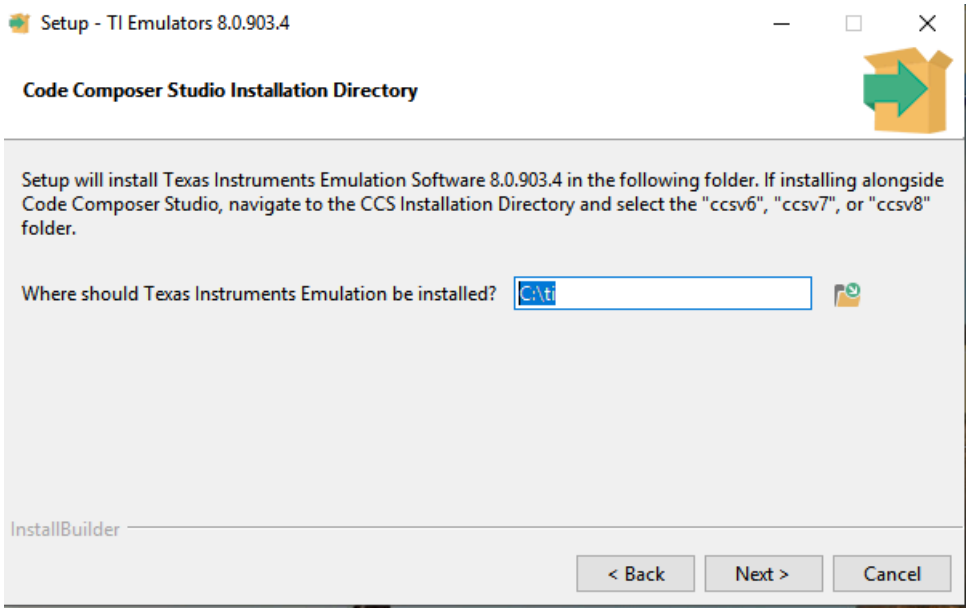


Figure 6-11. Setup Screen 11

In the next few windows click **Next >**, and if prompted by Windows Security about software installation as shown in Figure 6-12, select **Install**.

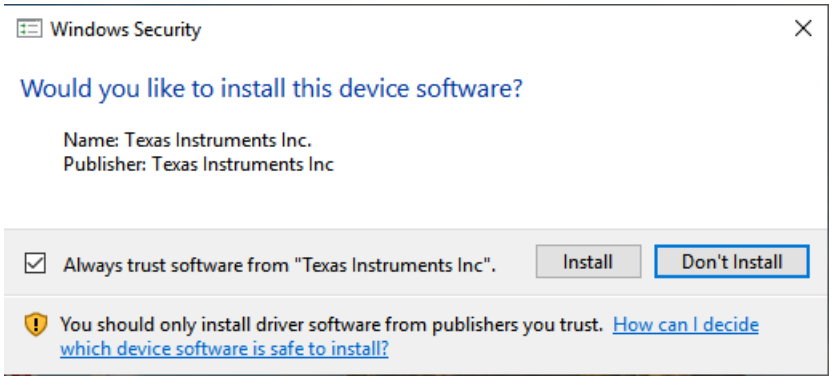


Figure 6-12. Setup Screen 12

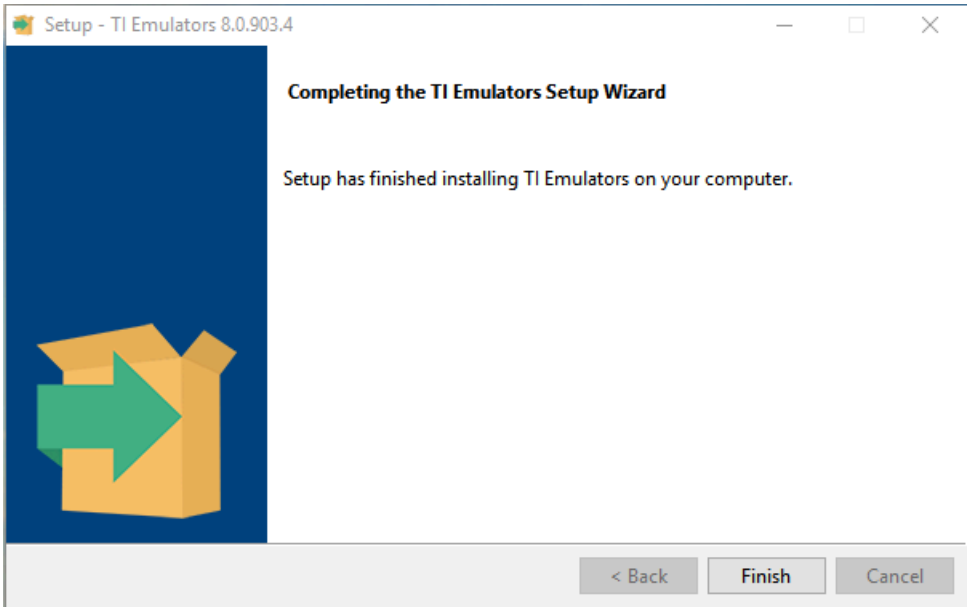


Figure 6-13. Setup Screen 13

The screen showing the completion of the TI Emulators installation is shown in Figure 6-13. Click **Finish** to move to the next step.

The UniFlash installation starts at this point. UniFlash is required to program the LaunchPad. In the next few steps as shown in Figure 6-14, Figure 6-15 and Figure 6-16 click **Next >** to start the installation.

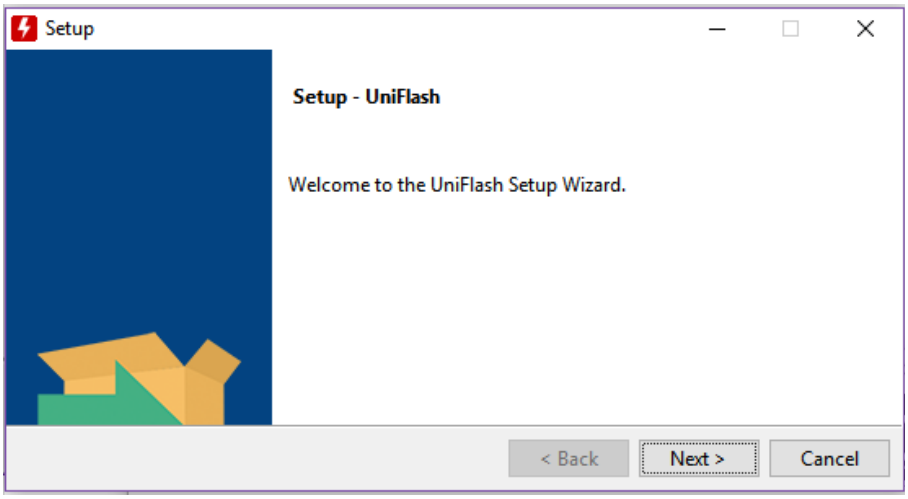


Figure 6-14. Setup Screen 14

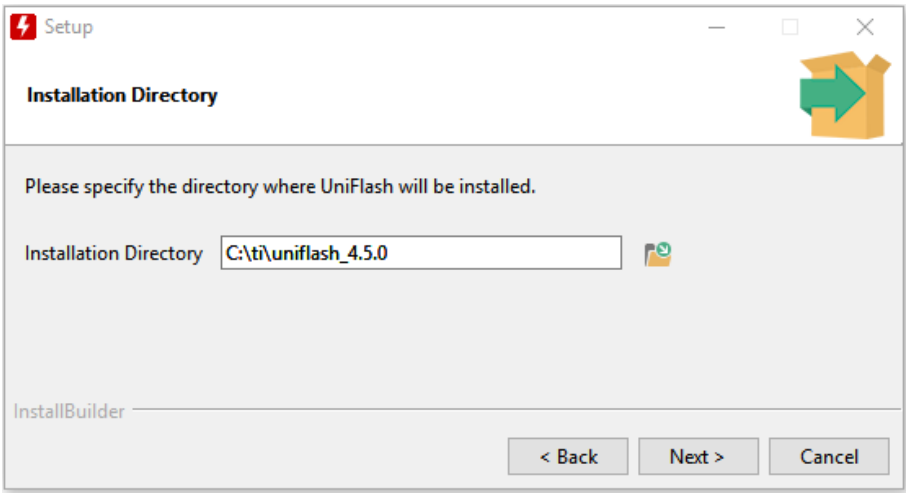


Figure 6-15. Setup Screen 15

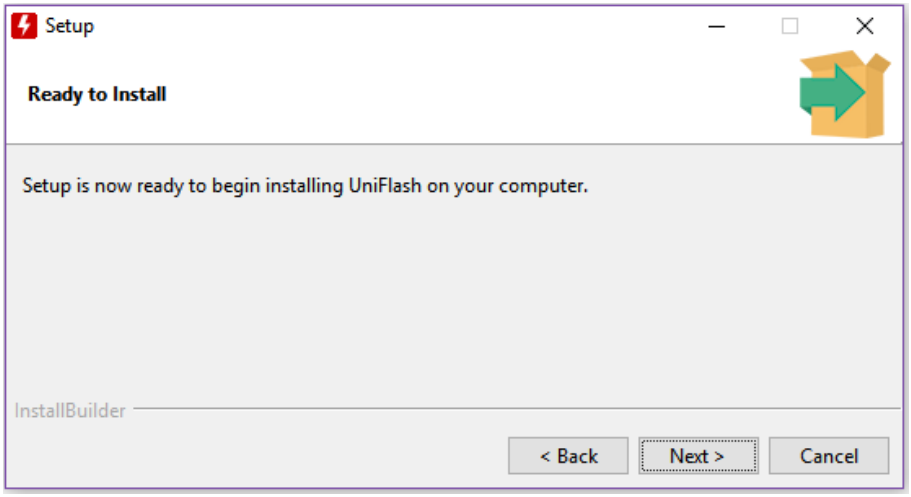


Figure 6-16. Setup Screen 16

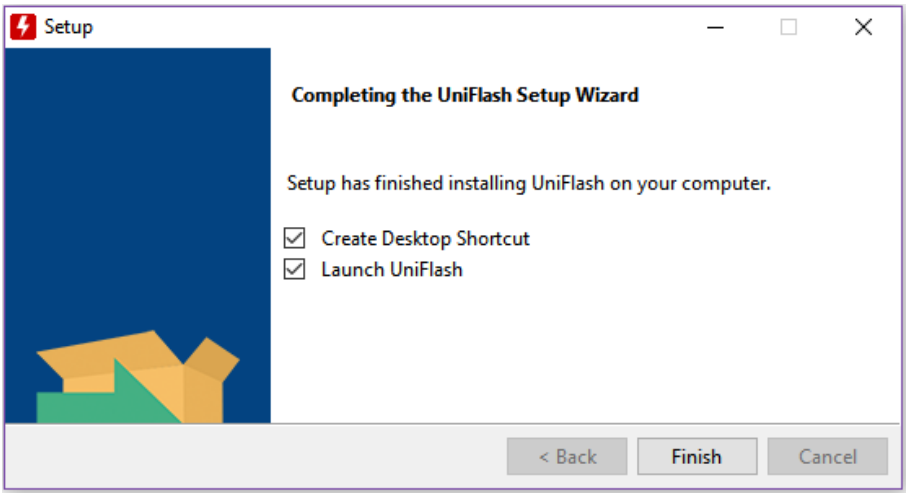


Figure 6-17. Setup Screen 17

When UniFlash installation completes, click **Finish** to launch the UniFlash and program the LaunchPad.

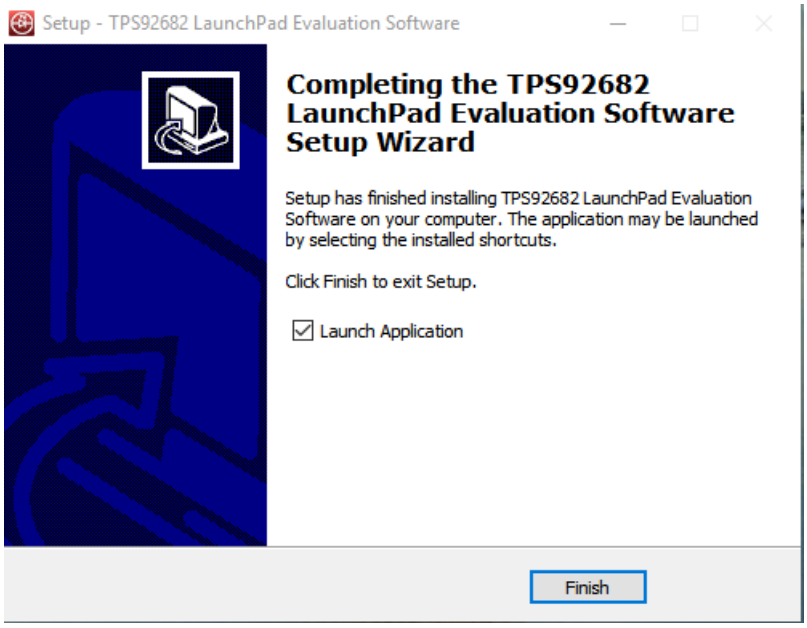


Figure 6-18. Setup Screen 18

Figure 6-18 shows the completion notification of the TPS92682-Q1 Evaluation Software. Deselect the **Launch Application** and click **Finish**.

6.2 Installation Error Recovery

If the screen shown in Figure 6-19 appears, follow the steps below to install an unsigned driver one time.

- Click **Start** and select **Settings**.
- Select **Update and Security**.
- Select **Recovery**.
- Click **Restart Now** under **Advanced Startup**.
- Click **Troubleshoot**.
- Select **Advanced Options**.
- Select **Startup Settings**.
- Click **Restart**.
- On the **Startup Settings** screen, press **F7** during reboot to disable driver signature enforcement. The host computer restarts.

- Repeat the entire reinstallation process.
- A message appears informing that installing .NET failed. Close that window and continue.
- Click **Install unsigned drivers** twice.

After restarting a second time, the host computer resets, which requires all drivers to be digitally signed the next time a default installation executes, unless these steps are repeated.

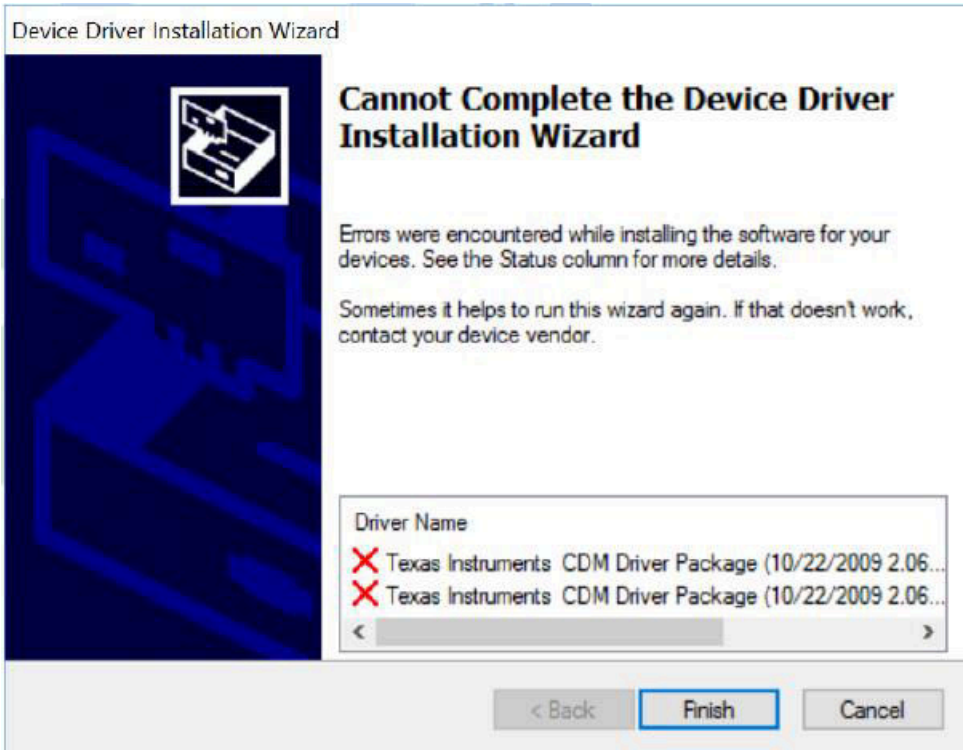


Figure 6-19. Driver Installation Error

6.3 Programming the MSP-EXP432E401Y LaunchPad Board

The LaunchPad Board must be programmed using the UniFlash before running the GUI. Connect the included Micro-USB cable to the USB port of the PC and the LaunchPad as shown in Figure 6-20. Connect a jumper between PINs 3 and 4 of the JP1 as shown in Figure 6-20.

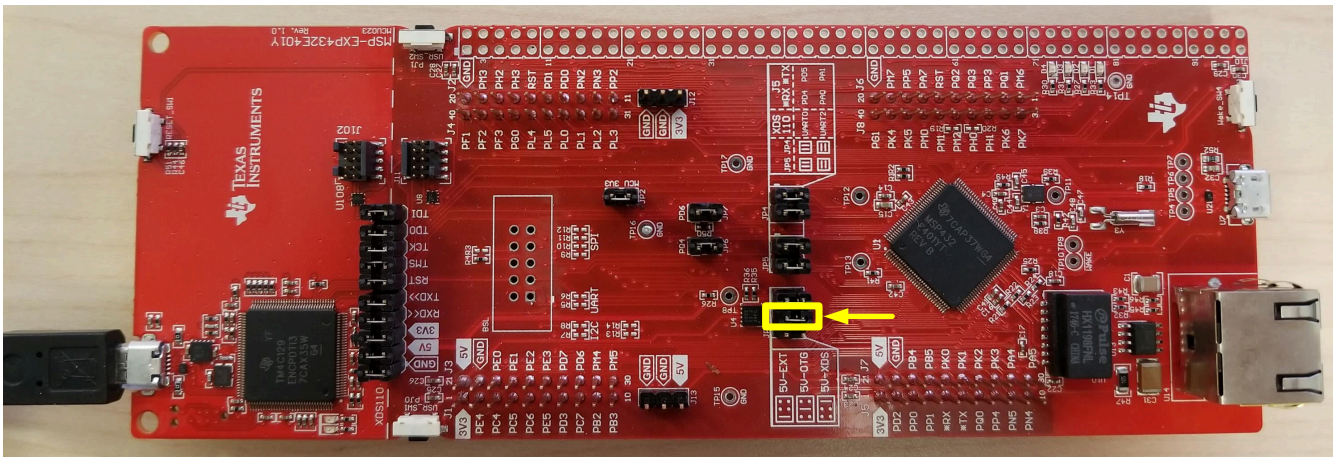


Figure 6-20. LaunchPad Connection for Programming

Typically, the installed UniFlash program opens at the end of the software setup shown in Figure 6-17. If the UniFlash program is not open, launch the program. The window shown in Figure 6-21 appears.

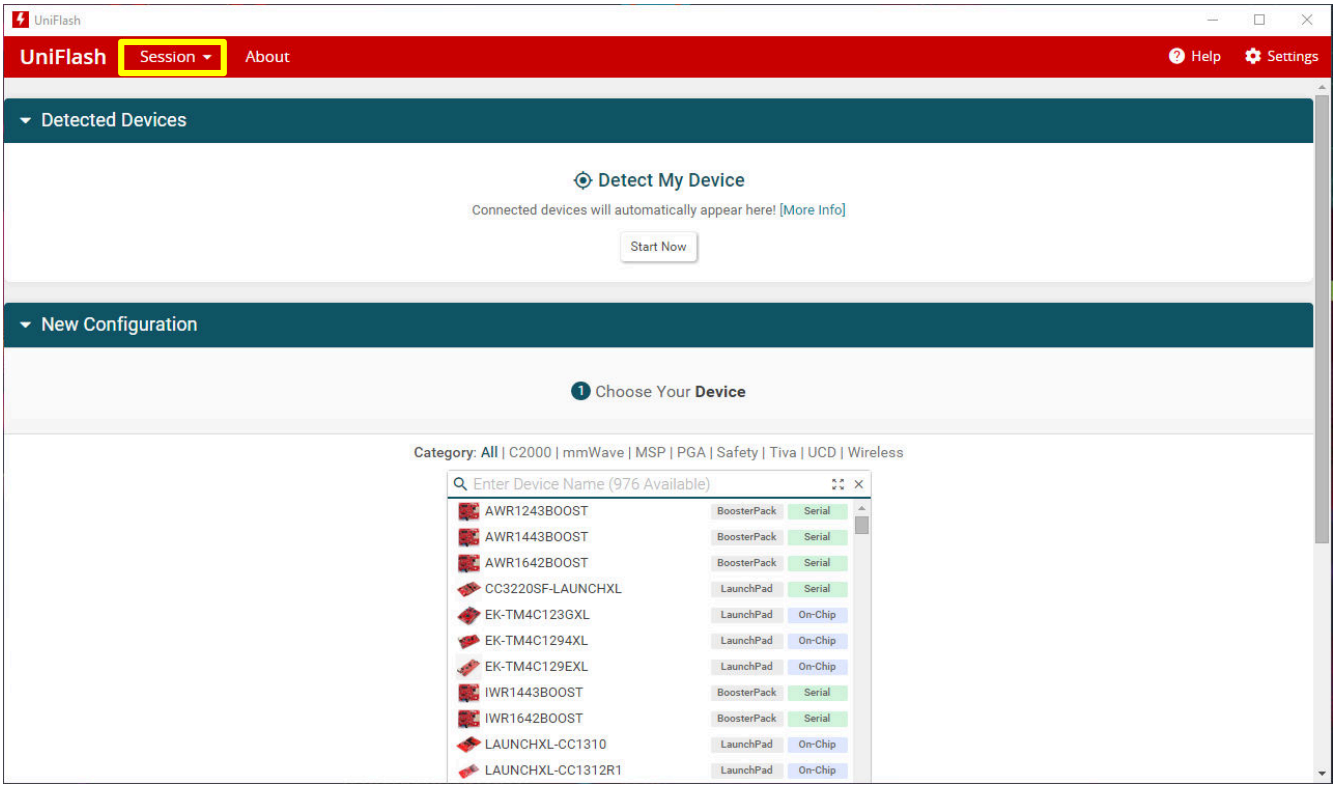


Figure 6-21. UniFlash Programming, Step 1

Click **Session** shown in Figure 6-21 and select **Load Session**.

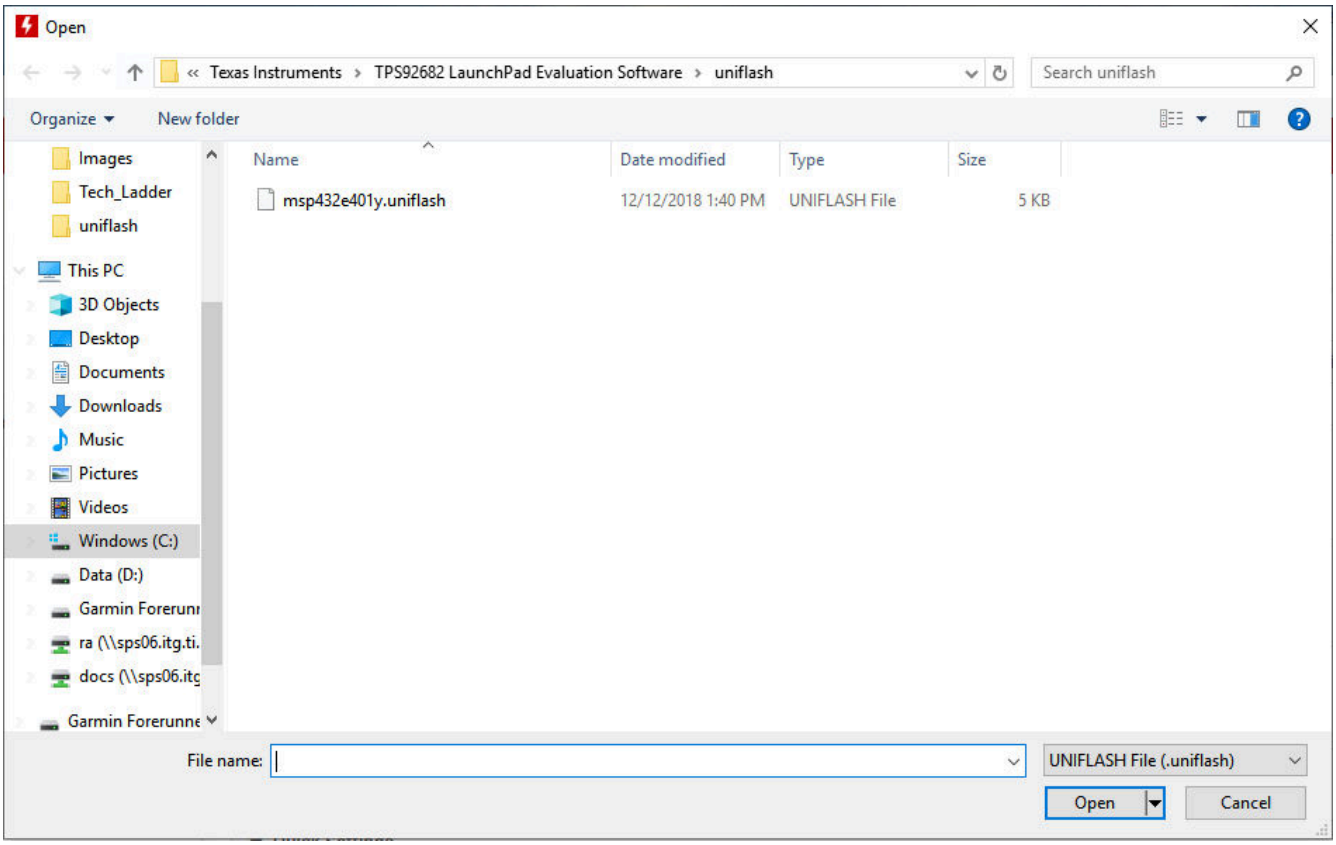


Figure 6-22. UniFlash Programming, Step 2

As shown in Figure 6-22, navigate to the *":\Texas Instruments\TPS92682 LaunchPad Evaluation Software\uniflash"* location and select the **msp432e401y.uniflash** file.

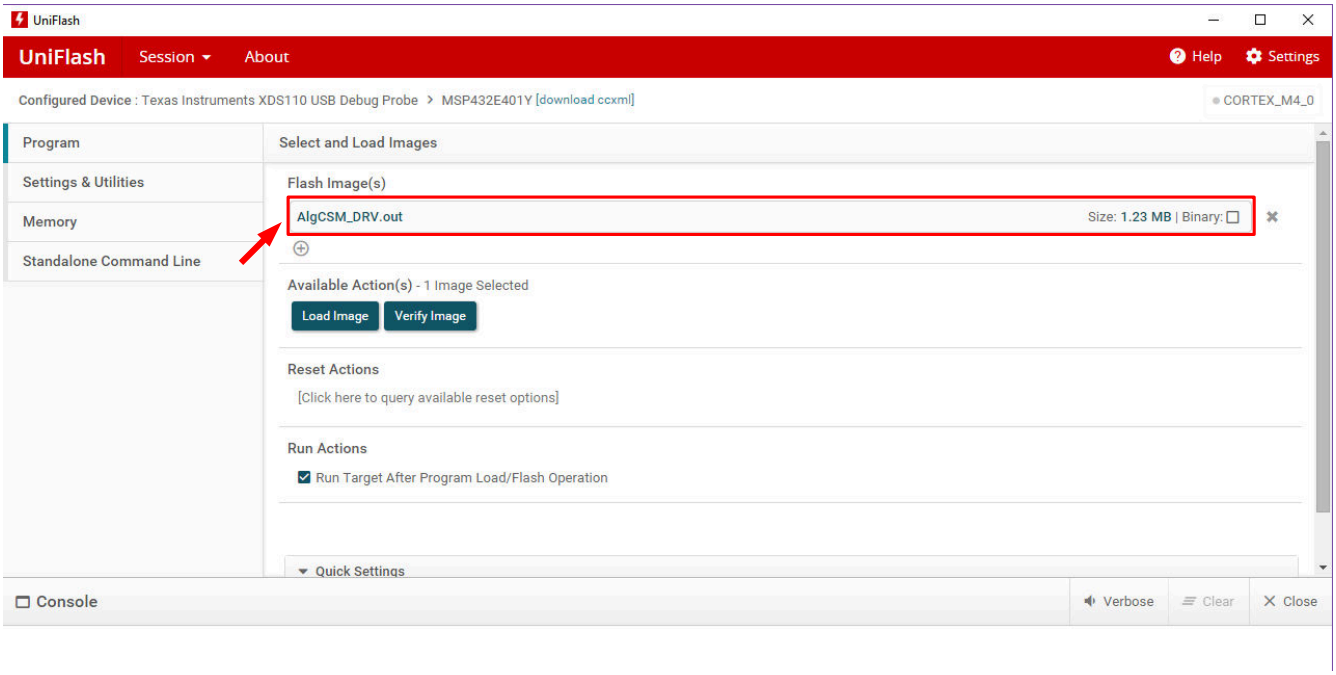


Figure 6-23. UniFlash Programming, Step 3

Click on the flash image file shown in the red box of Figure 6-23. Navigate to the *":\Texas Instruments\TPS92682 LaunchPad Evaluation Software\uniflash"* location and select the **AlgCSM_DRV.out** file as shown in Figure 6-24.

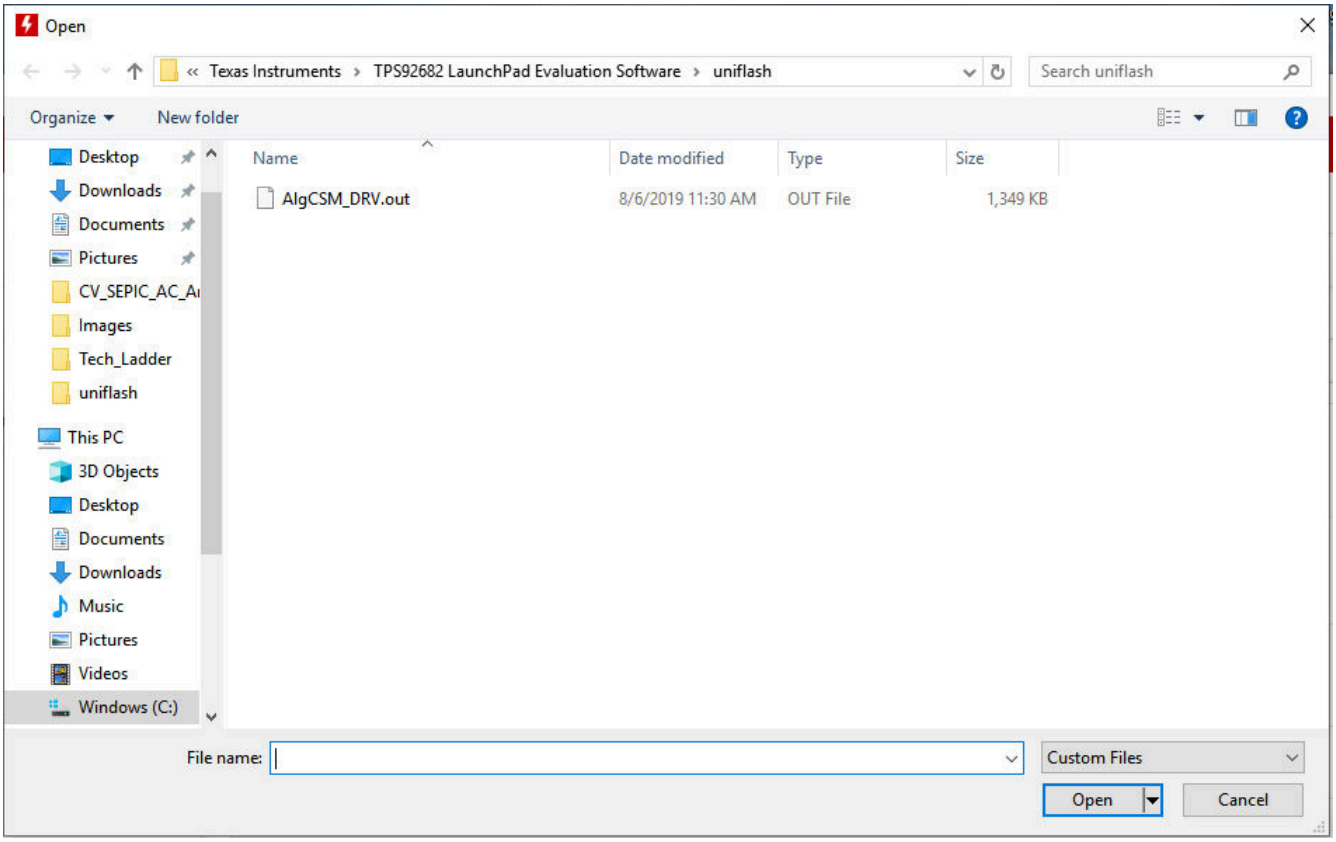


Figure 6-24. UniFlash Programming, Step 4

Click **Load Image**. After the program is loaded into the LaunchPad, a message appears in the console that the *Program Load completed successfully*, as shown in Figure 6-25.

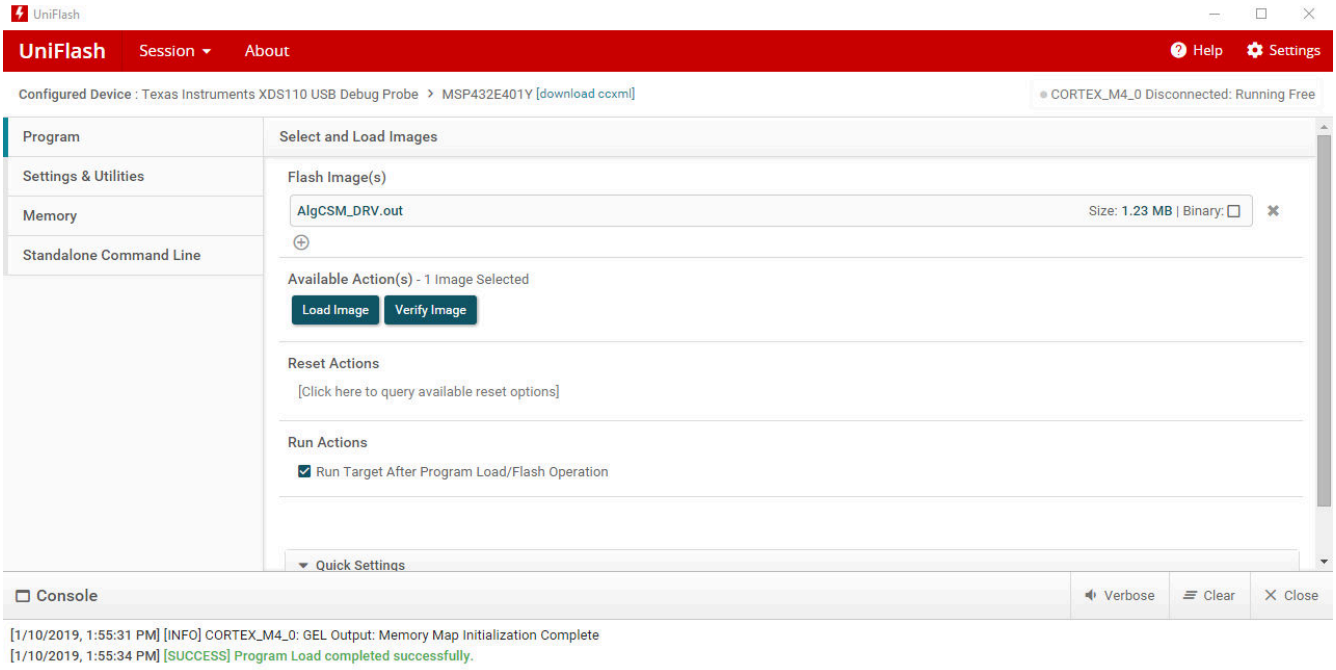


Figure 6-25. UniFlash Programming, Step 5

Close the UniFlash program, disconnect the Micro-USB from the LaunchPad and connect it to the USB port U7 on the other side of the LaunchPad, as shown in Figure 6-26.

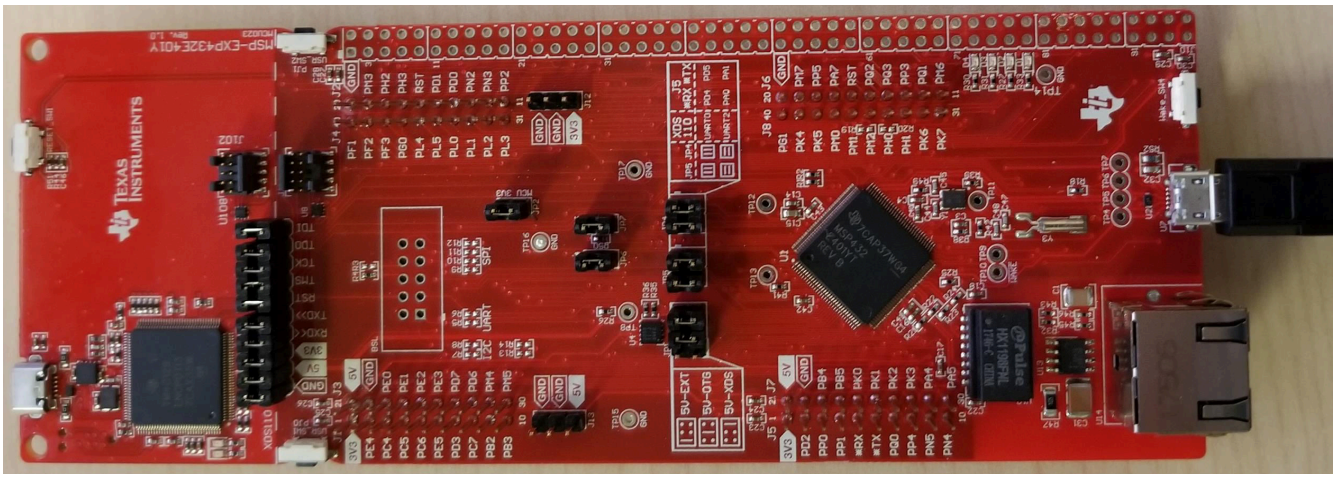


Figure 6-26. LaunchPad Connection for GUI Operation

7 TPS92682EVM-125 Power UP and Operation

To start the EVM operation, connect the header J10 on TPS92682EVM-125 to the header J2/J4 on the LaunchPad, and the header J11 to the header J1/J3, using two included ribbon cables as shown in Figure 7-1.

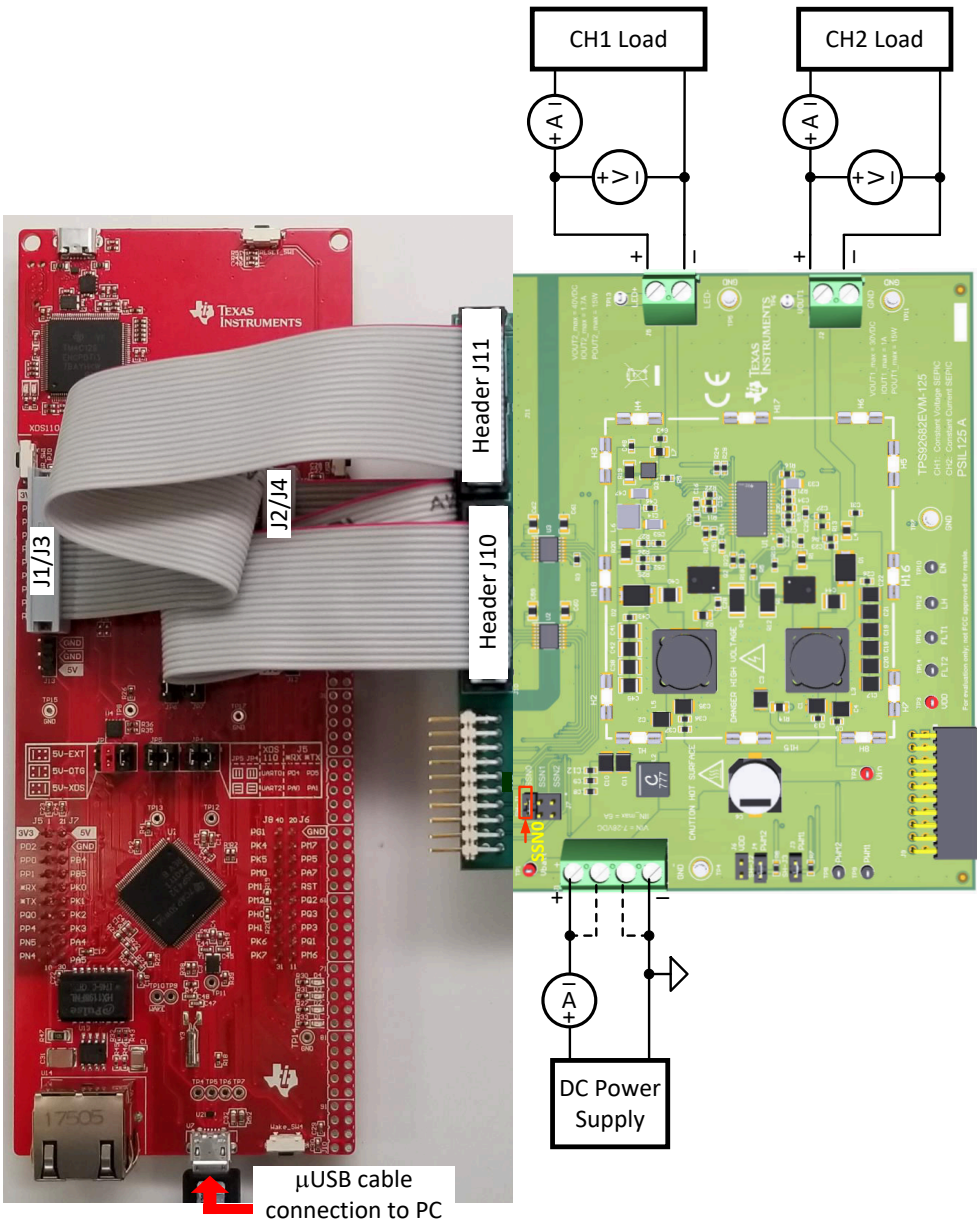


Figure 7-1. LaunchPad Connection to TPS92682EVM-125

Apply power (12 V) to the TPS92682EVM-125 board (terminal J1). Connect a resistive or a an electronic current sink load to the output of channel-1, terminal J2. Connect LED loads to the output of channel-2, terminal J5. Ensure that the loads are such that the maximum input and output current, maximum output power and maximum output voltage indicated on the EVM are not exceeded.

Run the program **LED_Controller_GUI_LP.exe**, located at the *":\Texas Instruments\TPS92682 LaunchPad Evaluation Software"*, to start the GUI. The window shown in Figure 7-2 opens.

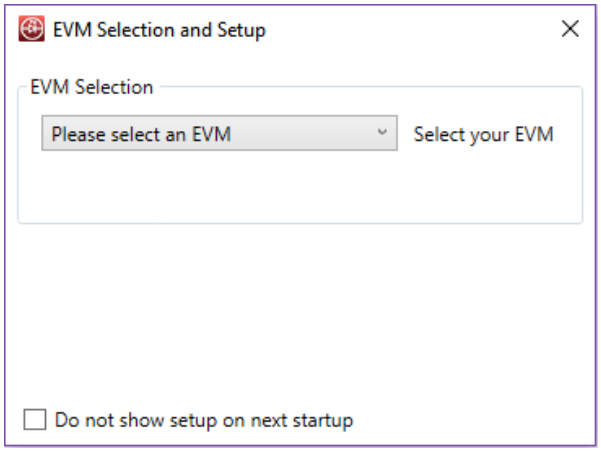


Figure 7-2. GUI Setup Screen 1

Click the EVM selection drop-down menu. Select **TPS92682 CC - PSIL070**.

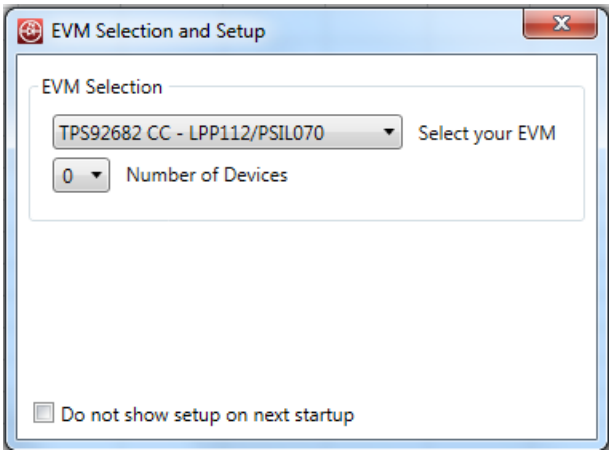


Figure 7-3. GUI Setup Screen 2

On the screen shown in Figure 7-3, select 1 as the number of devices. A new tab appears as shown in Figure 7-4. Select **682** for Device Type. Select **0** for Desired Address. Click **Add Device**.

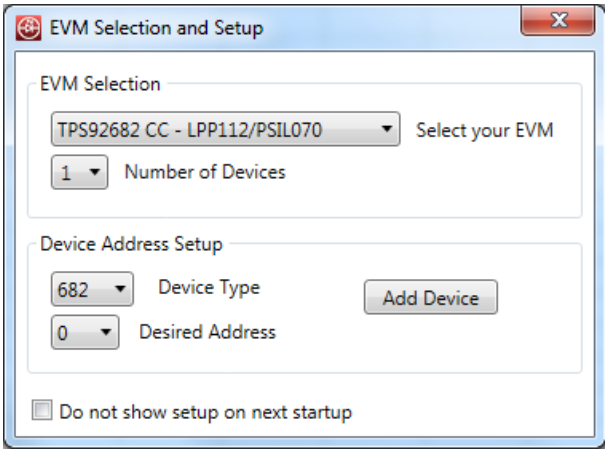


Figure 7-4. GUI Setup Screen 3

The main GUI window appears as shown in Figure 7-5. This window includes three sub-windows:

- MCU Control Box (1): includes controls for external PWM
- SPI Command Box (2): is used to manually read from and write to the registers on the SPI BUS

- Devices Box (3): is the main GUI control window to configure the TPS92682-Q1 device

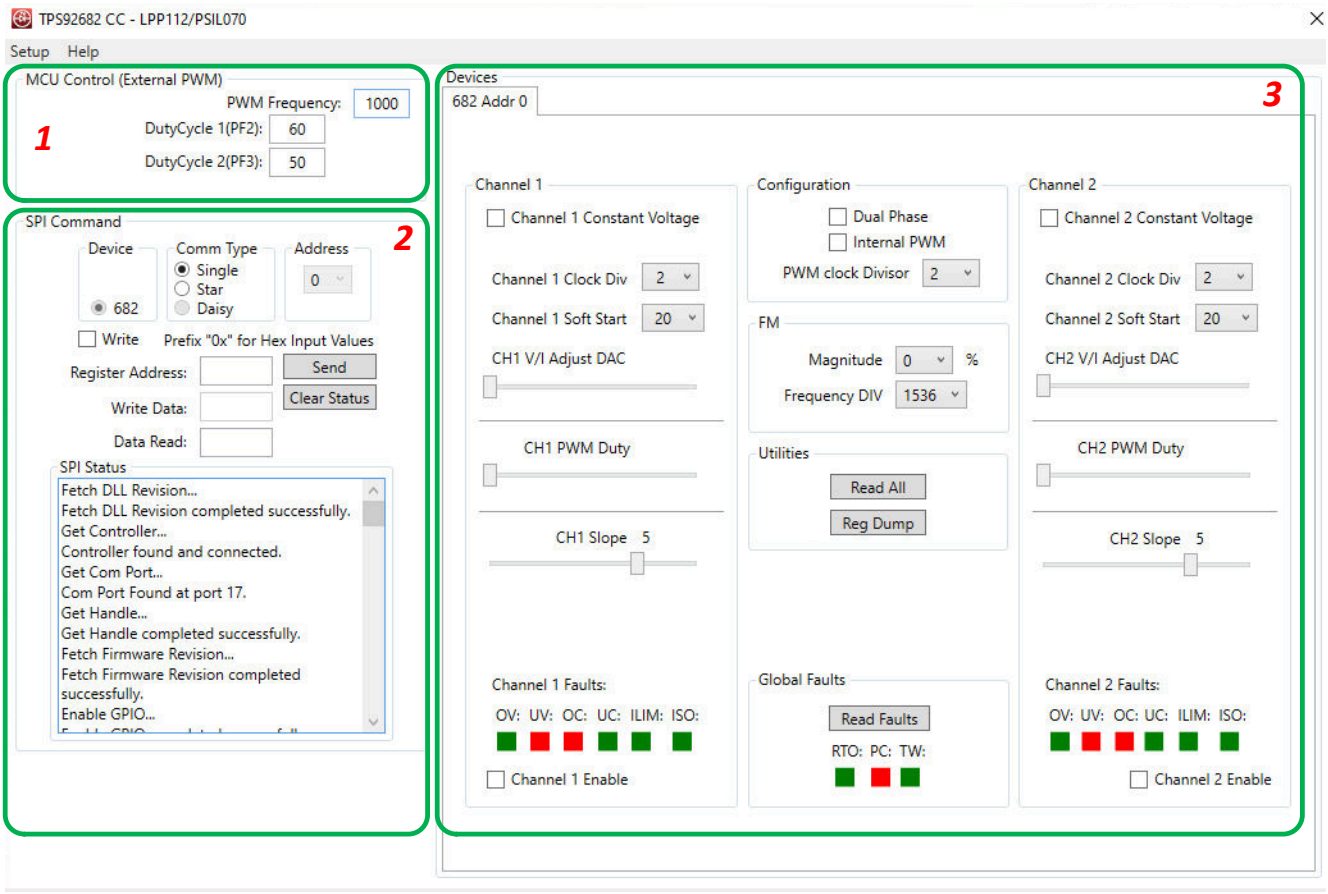


Figure 7-5. GUI, Main Window

7.1 SPI Command

The SPI command box, allow access to the *read from* and *write to* registers. In order to ensure connection to the TPS92682-Q1, perform the following steps as shown in Figure 7-6.

1. Write the register address zero in the *Register Address* box: 0x00.
2. Click **Send** *twice*.

The default value (0x3C) for the register 0 shows in the SPI Status window.

To write to a register, select the **Write** check-box. Write the desired data in the *Write Data* box shown in Figure 7-6. Click **Send** to write the data to the associated register address.

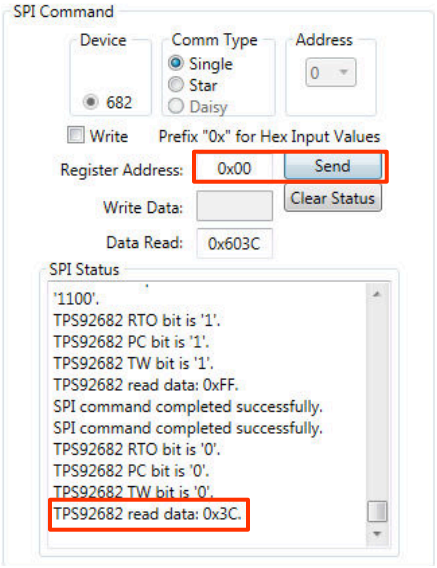


Figure 7-6. SPI Command Window

7.2 GUI Devices Window

In TPS92682EVM-125, channel-1 is configured as a CV mode SEPIC and channel-2 as a CC mode SEPIC converter. The settings shown in red in Figure 7-7 can be used to configure and turn on and regulate the output of the two channels.

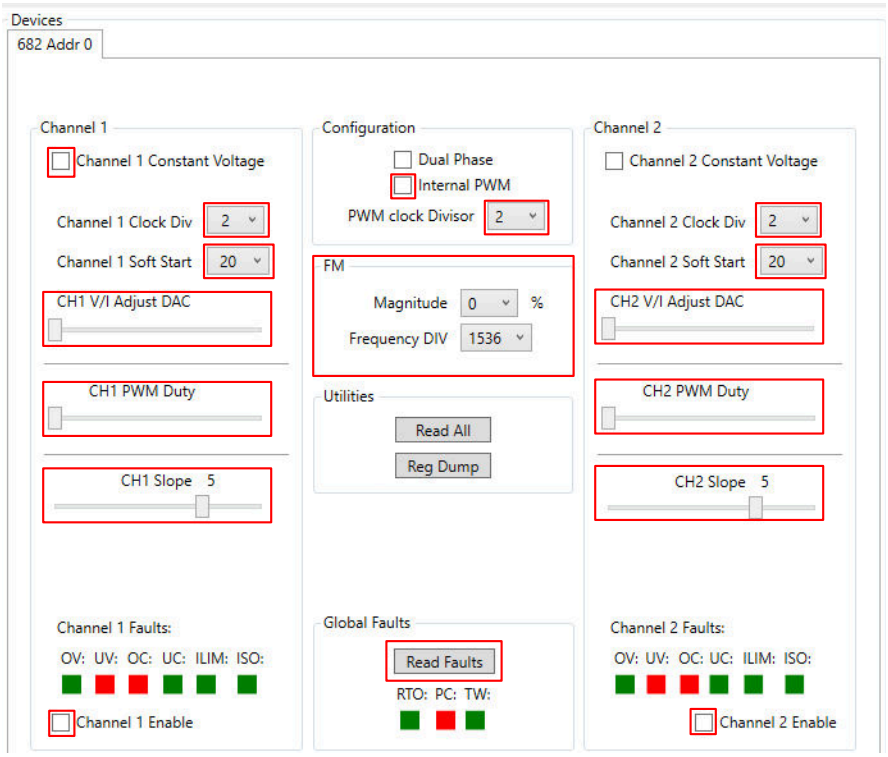


Figure 7-7. Devices Window

Apply the settings shown in Figure 7-8.

1. Select the Internal PWM box to set the PWM dimming to internal.
2. To set the switching frequency, f_{SW} to 400kHz, do not change the Channel Clock Div from the default value of 2.
3. Select the Channel 1 Constant Voltage box to set channel 1 in CV mode.

4. Enter Channel 2 Soft Start value to **100**.
5. Enter the desired value for the CH1 and CH2 V/I Adjust DAC. This DAC controls the output voltage of channel 1 and I_{LED} current of channel 2. For TPS92682EVM-125, the DAC maximum value of 255 corresponds with an output voltage of approximately 30 V for channel 1 and I_{LED} of approximately 1.7 A for channel 2. The relation between I_{LED} and the DAC value is shown in Equation 1.

$$I_{LED} = \frac{VIADJ \times 0.171}{255 \times R_{CS}} \quad (1)$$

   where R_{CS} is the current sense resistor (R20 for channel 2)
6. The EVM generates the internal PWM using a 10-bit DAC counter. Set the PWM duty cycle to 1023 for channel 1 (100% duty cycle for CV channel) and a value between zero and 1023 for PWM dimming for channel 2.
7. By default CHx-Slope is set to code "5", which corresponds to 250 mV of peak slope. For the TPS92682EVM-125, it is recommended to set the slopes for two channels to a code "2" and "1" as shown in Figure 7-8

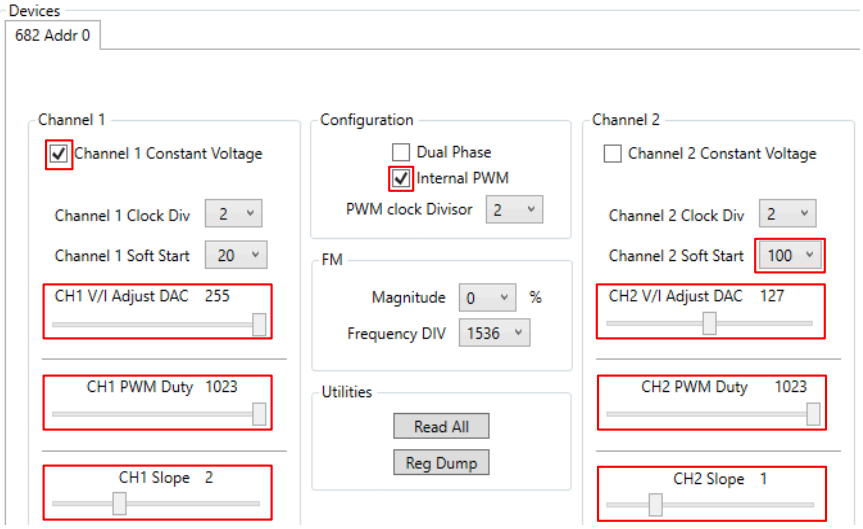


Figure 7-8. Devices Window Setting

After applying these settings, the fault status registers FLT1 (0x11) and FLT2 (0x12) must be checked. Before enabling and turning on the outputs, the fault registers must be read (cleared). The Power Cycle (PC) bit must be cleared in order for the TPS92682-Q1 is enabled. The fault status can be obtained by pushing the **Read Faults** button in Figure 7-9.

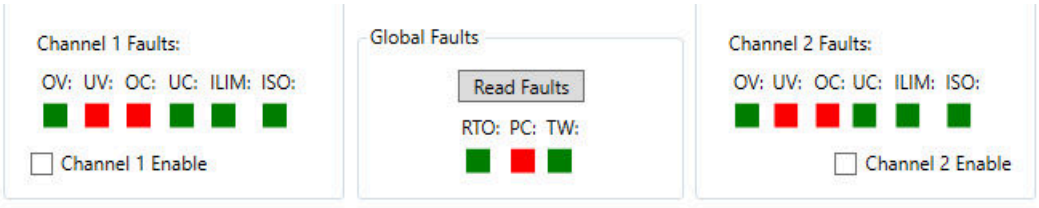


Figure 7-9. Fault Status after Pushing the Read Faults Once

The first time the Read Fault button is pushed, the previous status of the fault registers are shown and the faults are cleared. The second time the Read Faults button is pushed, the cleared faults will change to green as shown in Figure 7-10.

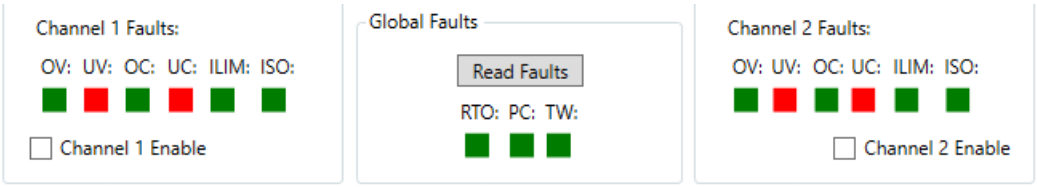


Figure 7-10. Fault Status after Pushing the Read Faults Twice

Some of the faults or diagnostic bits, as undercurrent (UC) and undervoltage (UV) may remain red as the channels are not turned on. For example, the output undervoltage (UV) remains red as the load voltage is initially zero. Therefore, this fault is disabled by default until the soft-start sequence is complete. The output overvoltage (OV), cycle-by-cycle current limit (ILIM), IS Open (ISO), RT Open (RTO), Power Cycle (PC) and Thermal Warning (TW) should be cleared (change status to green) before enabling the channels.

Before enabling the channels, make sure to connect LED loads to the outputs of the TPS92682EVM-125. By setting the Channel 1 and Channel 2 Enable check boxes, the two channels are turned on. At this point after clicking **Read Faults**, for 100% PWM duty cycle, all faults as shown in Figure 7-11 are cleared, except the UC fault for channel 1, which is configured in CV mode. UC fault is ignored in CV mode.

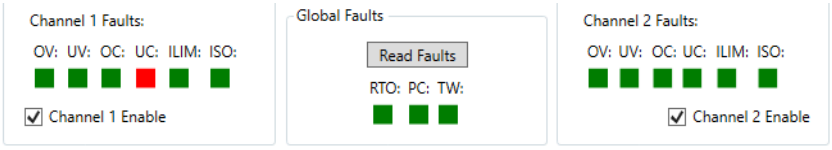


Figure 7-11. Enabling the EVM

To turn off the channels, de-select the Channel 1 and Channel 2 Enable boxes.

If a power cycle occurs, all the registers reset to default values. In this case, it is necessary to repeat all the steps described in Section 7 before re-enabling the converter.

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