Using the UCC23514EVM

User's Guide

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1 Introduction

The UCC23514EVM evaluation module is designed for evaluation of TI's 5-kV_{RMS} isolated single-channel gate drivers with opto-compatible input, and UCC23511. The input is current driven, requiring between 7 mA and 16 mA for device turn-on, and can be reverse biased for turnoff. The UCC23514 is a 4.5-A source and 5.3-A peak sink current for driving Si MOSFETs, IGBTs, and SiC transistors. This user's guide covers the UCC23514EVM, which is used for evaluation of the UCC23514M, UCC23514E, UCC23514S, and UCC23514V, which are similar 8-pin SOIC package devices. In this user guide, the UCC23514M is shown as the primary example.

Developed for high voltage applications where isolation and reliability are required, the UCC23514EVM family of devices deliver reinforced isolation of 5.7 kV_{RMS} and a surge immunity tested up to 8 kV along with a common mode transient immunity (CMTI) greater than 150 V/ns. It offers lower propagation delay, lower-part to-part delay skew, higher CMTI, smaller Pulse Width Distortion, and higher operating temperature, which provides significant performance upgrade over opto isolated gate drivers, while still maintaining pin-to-pin compatibility.

The input current and voltage characteristics of the *e*-diode™ functionally mimics the primary side of an opto-isolator. The output side VCC has a wide recommended operating range from 14-V to 33-V and allows the device to be used in a low-side or high-side configuration along with bipolar supplies for SiC Power FETs. The pin-to-pin compatibility enables designers to use the UCC23514 in existing designs and new designs for motor drives, industrial power supplies, solar inverters, and UPS.

2 Description

The UCC23514EVM evaluation board utilizes a SN74LVC2G17DBVR (dual Schmitt-Trigger buffer) to drive signal current on the primary side of the device. The board is populated with clips, 2-position, and 3-position headers for flexibility in connecting power and signal inputs, along with signal test points and large GND vias to enable installation of ground springs. The PCB layout is optimized with minimal loop area in the input and output paths and showcases design for high voltage between the primary side and secondary side with >8 mm creepage. For detailed device information, refer to the UCC23514 and UCC23511 datasheets and TI's Isolated gate driver solutions.

Table 1. EVM Compatible Devices

Part Number	Description	Package	Feature Description
UCC23514M	4-A source / 5-A sink, output current	Stretched SO-6 package with >8.5-mm creepage and clearance	Miller clamp
UCC23514E	4-A source / 5-A sink, output current	Stretched SO-6 package with >8.5-mm creepage and clearance	Emitter-referenced UVLO
UCC23514S	4-A source / 5-A sink, output current	Stretched SO-6 package with >8.5-mm creepage and clearance	Split Output
UCC23514V	4-A source / 5-A sink, output current	Stretched SO-6 package with >8.5-mm creepage and clearance	Single V_{OUT} pin

(1) *e*-diode is a trademark of Texas Instruments.

2.1 Features

- Evaluation module for the UCC23514 in stretched SO-6 package
- 5-V input buffer, and 14-V to 33-V VCC power supply range
- 4-A and 5-A source/sink current capability (UCC23514)
- 5-kV_{RMS} Isolation for 1 minute per UL 1577
- Buffer disconnect headers for custom input drive solution
- Configurable jumpers allow board to test all UCC23514 variants with miller clamp, negative-supply, and split output

2.2 I/O Description

Table 2. Jumpers Setting

PINS	DESCRIPTION
J1–1	Anode Buffer input
J1–2	GND input
J2–1	Cathode Buffer input
J2–2	GND input
J3–1	Cathode Resistor input
J3–2	GND input
J4–1	Anode Buffer Jumper
J4–2	Anode Buffer Jumper
J5–1	Cathode Buffer Jumper
J5–2	Cathode Buffer Jumper
J6–1	Negative Supply Connection
J6–2	U1 pin 5 (VEE)
J6-3	COM
J7–1	COM
J7–2	U1 pin 6 (CLAMP for UCC23514M)
J7–3	VG
J8–1	R7 to VG Jumper
J8–2	R7 to VG Jumper
J9–1	VG to C9 Jumper
J9–2	VG to C9 Jumper
J10–1	VG to C10 Jumper
J10–2	VG to C10 Jumper
P1-1	VDD
P1-2	GND

2.3 Jumpers (Shunt) Options

Table 3. Jumpers Setting

JACK	Jumper Setting Options		FACTORY SETTING
J1	Option A:	Jumper not installed, IN/PWM signal provided by external signal	Option A
	Option B:	Jumper on J1-1 and J1-2 set Anode Buffer Input low	
J2	Option A:	Jumper on J2-1 and J2-2 set Cathode Buffer Input low	Option A
	Option B:	Jumper not installed, IN/PWM signal provided by external signal	
J3	Option A:	Jumper not installed, Cathode_R left floating from GND	Option A
	Option B:	Jumper on J3-1 and J3-2, ties Cathode_R to GND	
J4	Option A:	Jumper on J4-1 and J4-2, pass signal to Anode Resistor	Option A
	Option B:	Jumper not installed, Anode_R left floating for external drive	
J5	Option A:	Jumper on J5-1 and J5-2, pass signal to Cathode Resistor	Option A
	Option B:	Jumper not installed, Cathode_R left floating for external drive	

Table 3. Jumpers Setting (continued)

JACK	Jumper Setting Options		FACTORY SETTING
J6	Option A:	Jumper installed on J6-2 and J6-3, U1 pin 5 (VEE) tied to GND	Option A
	Option B:	Jumper installed on J6-1 and J6-2, U1 pin 5 (VEE) tied to Negative supply pin	
	Option C:	Jumper not installed, U1 pin 5 (VEE) left floating	
J7	Option A:	Jumper installed on J6-2 and J6-3, U1 pin 6 tied to VG	Option A
	Option B:	Jumper installed on J6-1 and J6-2, U1 pin 6 tied to COM	
	Option C:	Jumper not installed	
J8	Option A:	Jumper not installed, R7 left floating	Option A
	Option B:	Jumper installed, ties R7 to VG	
J9	Option A:	Jumper installed, adds 1uF load to VG	Option A
	Option B:	Jumper not installed, no load added to VG	
J10	Option A:	Jumper not installed, no load added to VG	Option A
	Option B:	Jumper installed, adds 180nF load to VG	

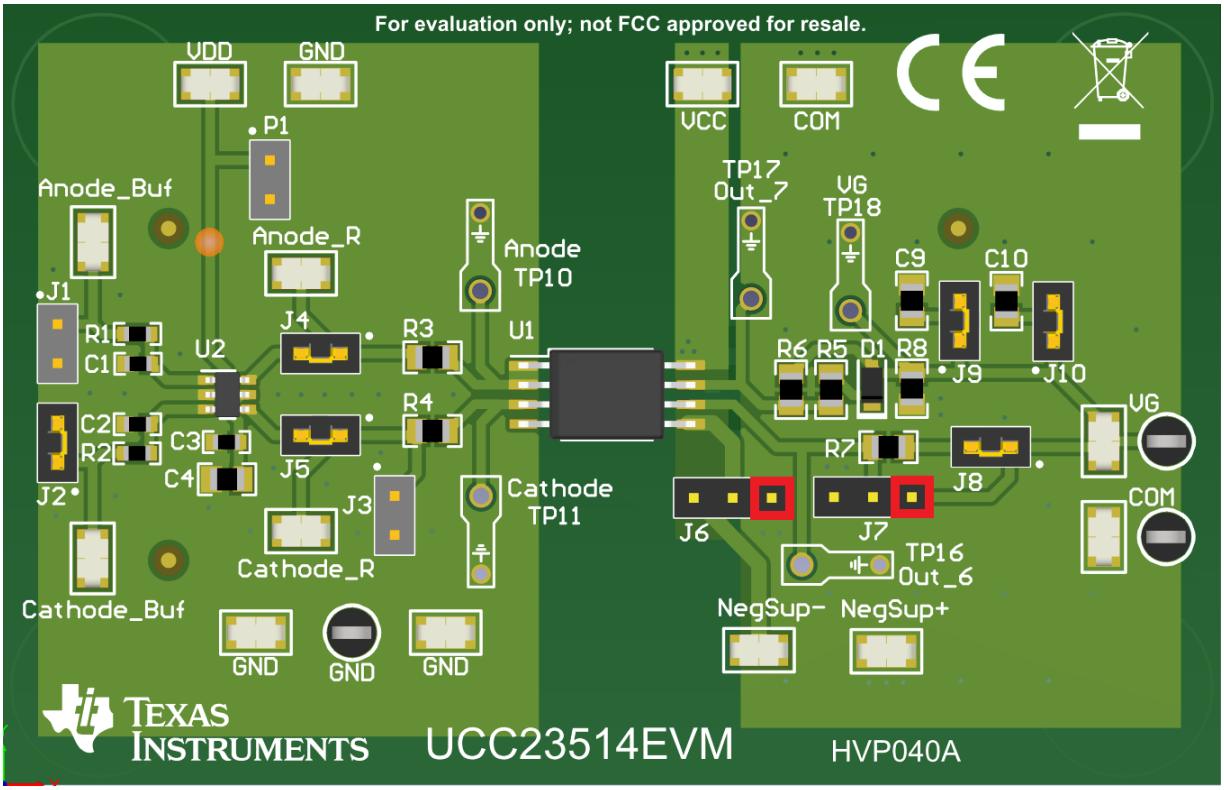

Figure 1. Triple Jumper Pin 1 Locations

2.4 EVM Configurations

Table 4. EVM Configurations

UCC23514EVM Configurations	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
UCC23514M (Default)	A	A	B	A	A	A	A	A	A	A
UCC23514E	A	A	B	A	A	B	B	A	A	A
UCC23514S	A	A	B	A	A	A	C	B	A	A
UCC23514V	A	A	B	A	A	A	C	B	A	A

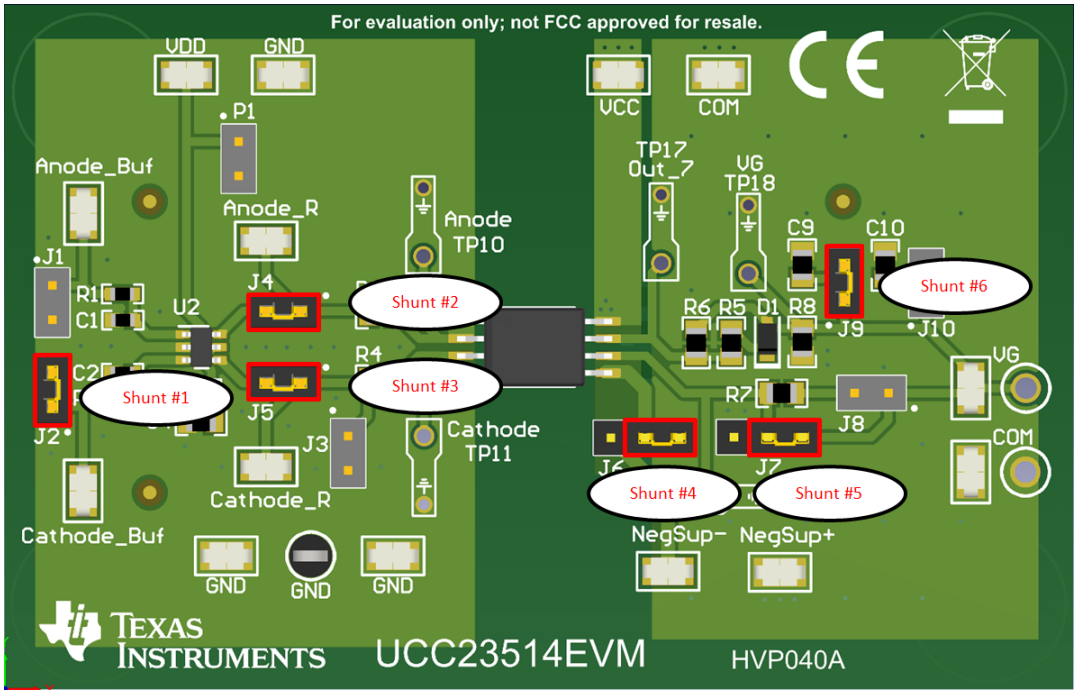

Figure 2. UCC23514M Jumper Configuration (Default)

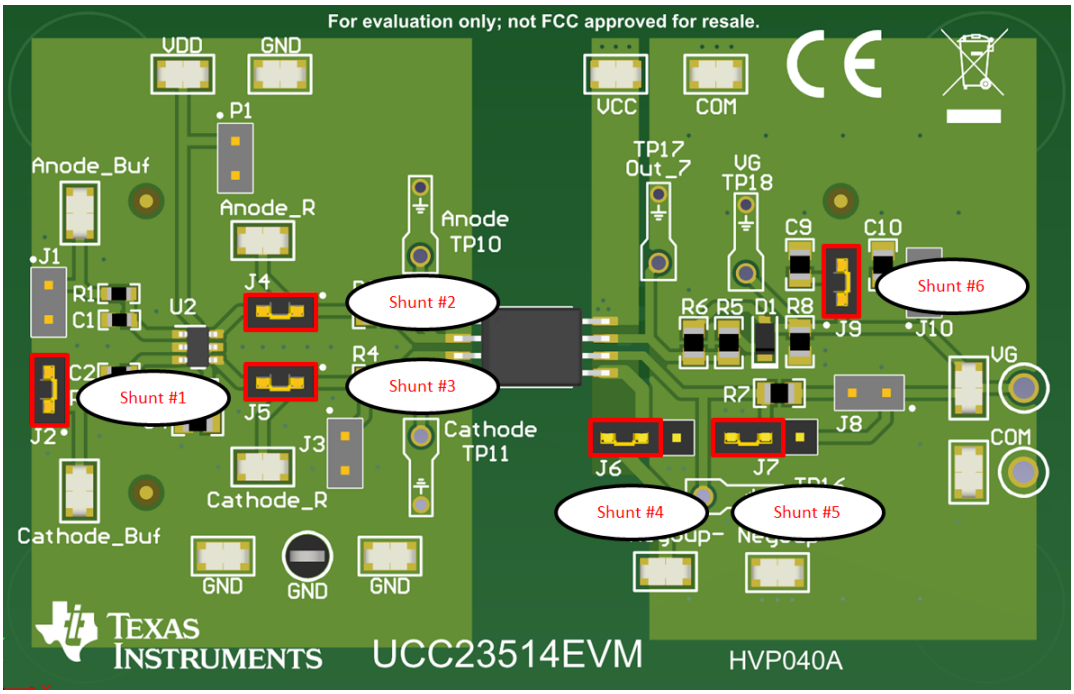

Figure 3. UCC23514E Jumper Configuration

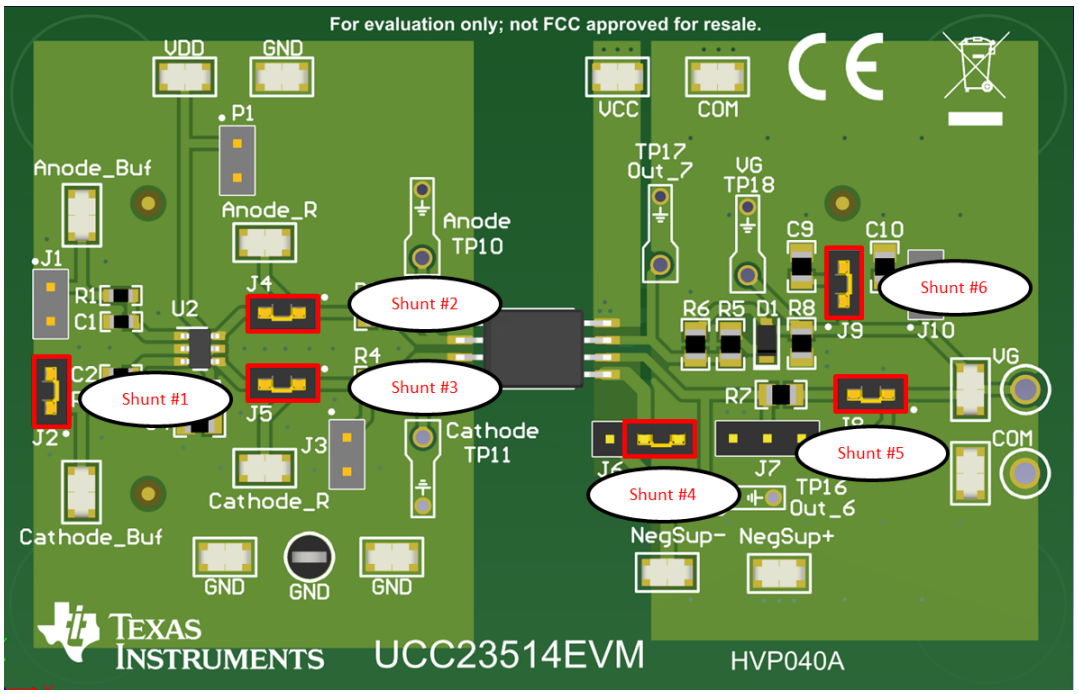

Figure 4. UCC23514S Jumper Configuration

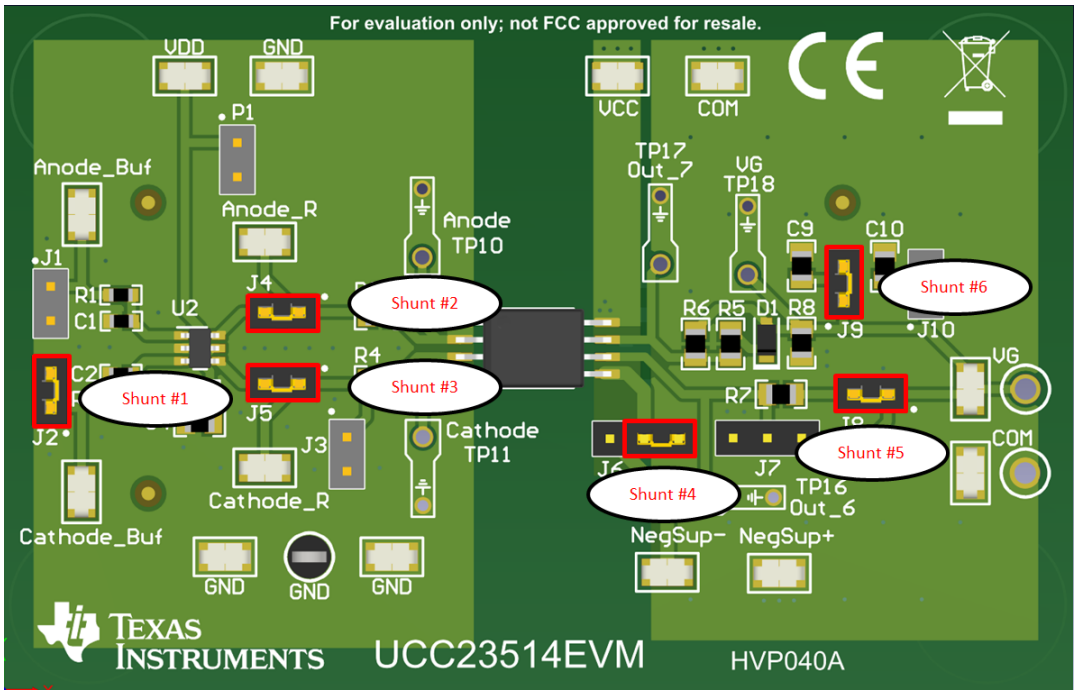

Figure 5. UCC2314V Jumper Configurations

3 Electrical Specifications

Table 5. UCC23514EVM-040 Electrical Specifications

DESCRIPTION		MIN	TYP	MAX	UNIT
V_{DD}	Primary-side power supply	4.5		5.5	V
V_{CC}	Driver output power supply	14		33	V
I_F(ON)	Input Diode Forward Current (Diode "ON")	7		16	mA
T_J	Operating junction temperature range	-40		150	°C

4 Test Summary

In this section, the UCC23514EVM is tested in its default configuration. Different jumper settings, PWM signal input options, and voltage source settings can be found in Section 3 Electrical Specifications.

4.1 Definitions

This procedure details how to configure the UCC23514 evaluation board. Within this test procedure, the following naming conventions are followed. Refer to the UCC23514EVM-040 schematic, Section 7, for details.

V_{XX}: External voltage supply name

$V_{(TPxx)}$: Voltage at test point TPxx. For example, V(TP12) means the voltage at TP12.

$V_{(Jxx)}$: Voltage at jack terminal Jxx

$J_{xx(yy)}$: Terminal or pin yy of jack xx

DMM: Digital multi-meters

UUT: Unit under test

EVM: Evaluation module assembly. In this case, the UUT assembly drawings have location for jumpers, test points, and individual components.

4.2 Equipment

4.2.1 Power Supplies

Two DC power supply with voltage/current above 5-V/0.1-A and 15-V/0.5-A (for example: Agilent E3634A)

4.2.2 Function Generators

One function generator over 1 MHz (for example: Tektronics AFG3252)

4.3 Equipment Setup

4.3.1 DC Power Supply Settings

- DC power supply #1
  - Voltage setting: 5-V
  - Current limit: 0.05-A
- DC power supply #2
  - Voltage setting: 15-V for the UCC23514
  - Current limit: 0.1 A

4.3.2 Digital Multi-Meter Settings

- Digital multi-meter #1

  - DC current measurement, auto-range
- Digital multi-meter #2
  - DC current measurement, auto-range

4.3.3 Function Generator Settings

Table 6. Function Generator Settings

	MODE	FREQUENCY	DUTY	DELAY	HIGH	LOW	OUTPUT IMPEDANCE
Channel Output	Pulse	DC ~ 100 kHz	50%	0 ns	5 V	0 V	High Z

4.3.4 Oscilloscope Setting

Table 7. Oscilloscope Settings

	BANDWIDTH	COUPLING	TERMINATION	SCALE SETTINGS	INVERTING
Channel A	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	OFF
Channel B	500 MHz or above	DC	1 MΩ or automatic	10× or automatic	OFF

4.3.5 Jumper (Shunt) Settings

Default shunt configuration should be adequate for this test.

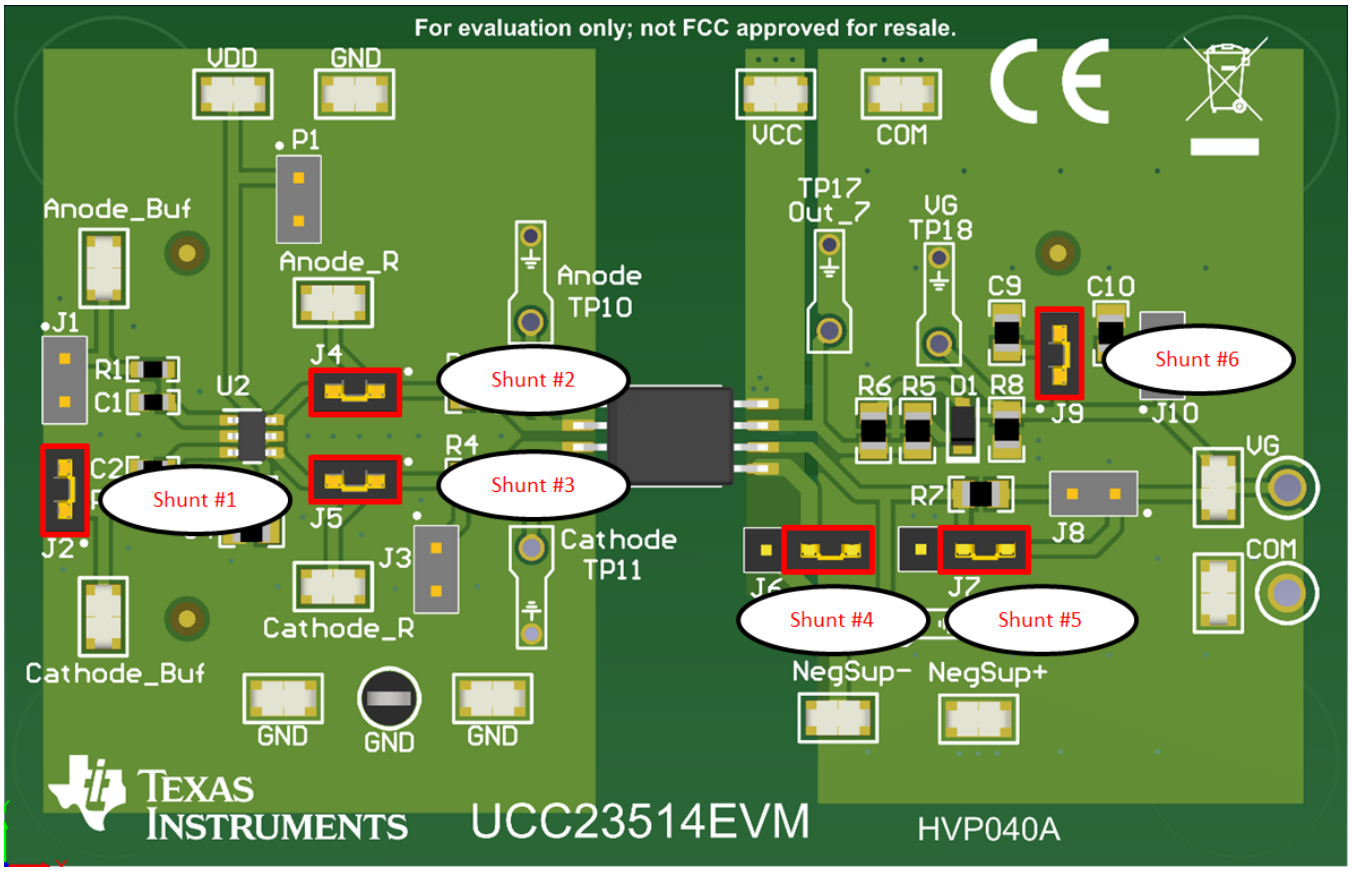

Figure 6. Default Jumper Settings

4.3.6 Bench Setup Diagram

The current bench setup diagram includes the function generator and oscilloscope connections.

Follow the connection procedure below. Figure 7 can be used as a reference.

- Make sure the output of the function generator and voltage sources are disabled before connection.
- Function generator channel applied on Anode_Buf←→Cathode_Buf or J1-1 ←→ J1-2 (see in Figure 7)
- Power supply #1: positive node connected to input of DMM #1 with DMM #1 output connected to P1-1 (or VDD), and negative node applied on P1-2 (or GND).
- Power supply #2: positive node connected to input of DMM #2 with DMM #2 output connected to P2-1 (or VCC), negative node connected directly to P2-2 (or VSS).
- Oscilloscope channel-A probes Anode_R ←→ GND, smaller measurement loop is preferred.
- Oscilloscope channel-B probes VG (or J7-1) ←→ VSS, smaller measurement loop is preferred.

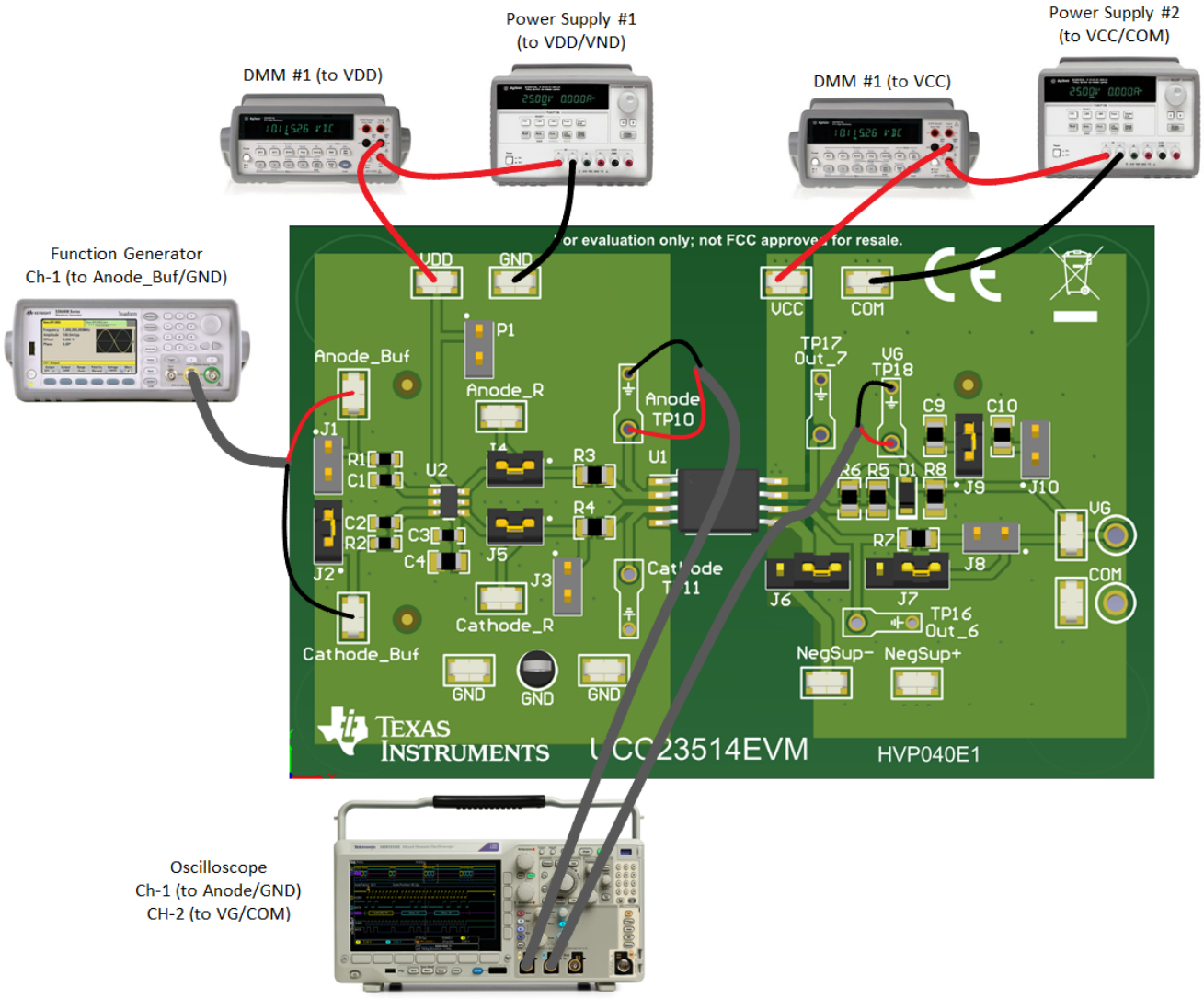

Figure 7. Bench Setup Diagram and Configuration

5 Power Up and Power Down Procedure

5.1 Power Up (C_L = 1000 pF)

1. Before proceeding to the power up procedure, make sure that Section 4.3.6 is implemented for setting up all the equipment. Figure 8 can be used as reference.
2. Enable supply #1.
3. Enable supply #2.The quiescent current on DMM1 and DMM2 ranges in 1 mA to 3 mA if everything is set correctly.
4. Enable function generator output.
5. Afterward, the following occurs:
    1. Stable pulse output on the channel-A and channel-B in the oscilloscope. See Figure 8.
    2. Scope frequency measurement is the same as function generator output.
    3. DMM #1 and #2 should read measurement results around 5 mA–10 mA under no load conditions. For more information about operating current, refer to UCC23514 datasheet.

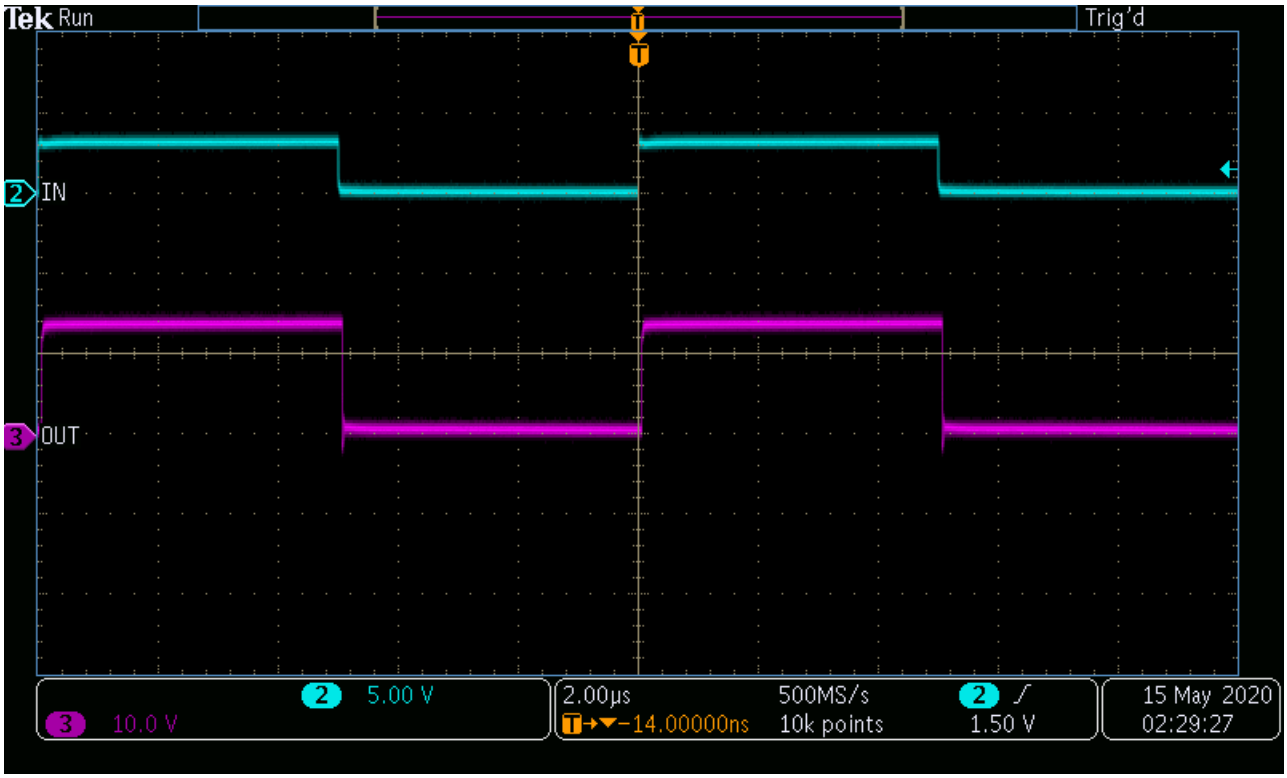

Figure 8. Example Input and Output Waveforms (Ch2 is PWM Input, Ch3 is Output)

5.2 Power Down

1. Disable function generator.
2. Disable power supply #2.
3. Disable power supply #1.
4. Disconnect cables and probes.

6 UCC23511 Test Implementation

Replace the UCC23514 with the UCC23511 from the default configuration on the EVM. Solder the UCC23511 sample and use Table 8 to adjust the value of R_{10} to observe the desired peak current out of the driver.

Table 8. Minimum Gate Resistor (Ω)

Gate driver supply VCC-VEE (V)	Minimum total gate resistance (Ω) = (R_{GON} + R_{G_int}) or (R_{GOFF} + R_{G_int})
15	4
23	7
30	10

7 Schematic

Figure 9 shows only the schematic diagram for the UCC23514EVM.

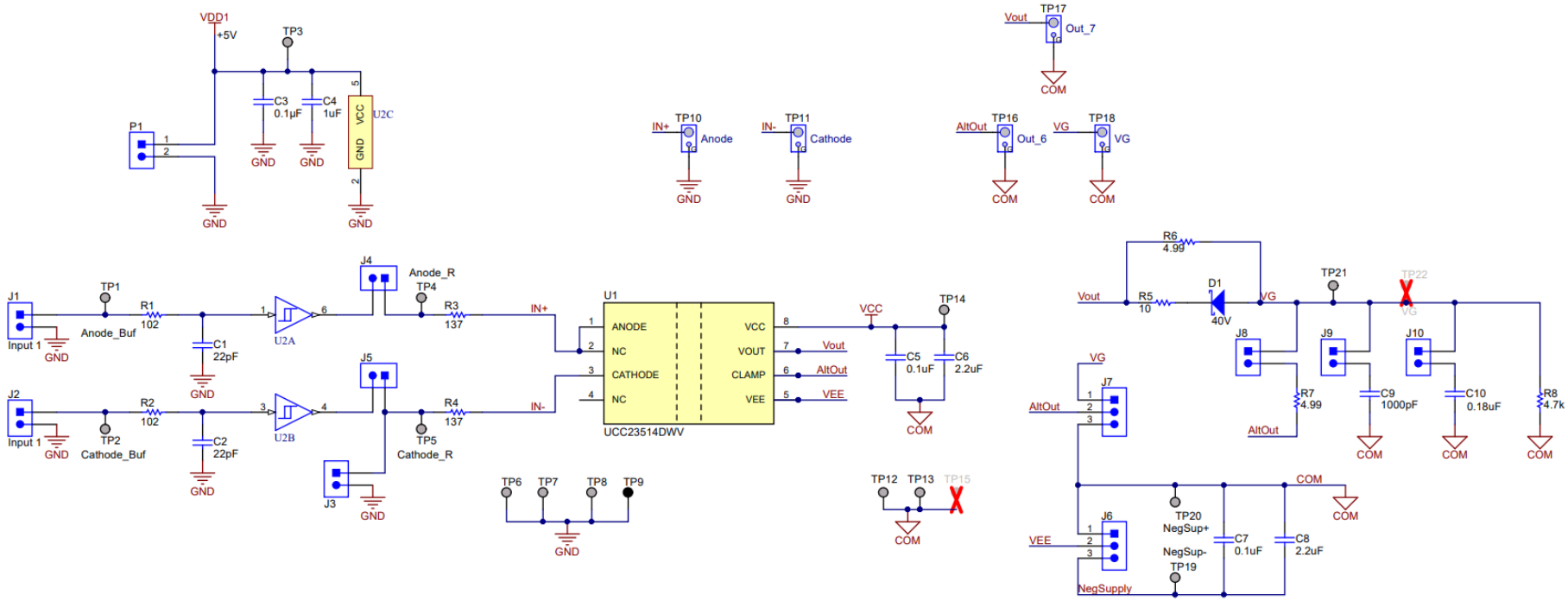

Figure 9. UCC23514EVM Schematic

8 Layout Diagrams

Figure 10, Figure 11, Figure 12, and Figure 13 show the PCB layout information for the UCC23514EVM.

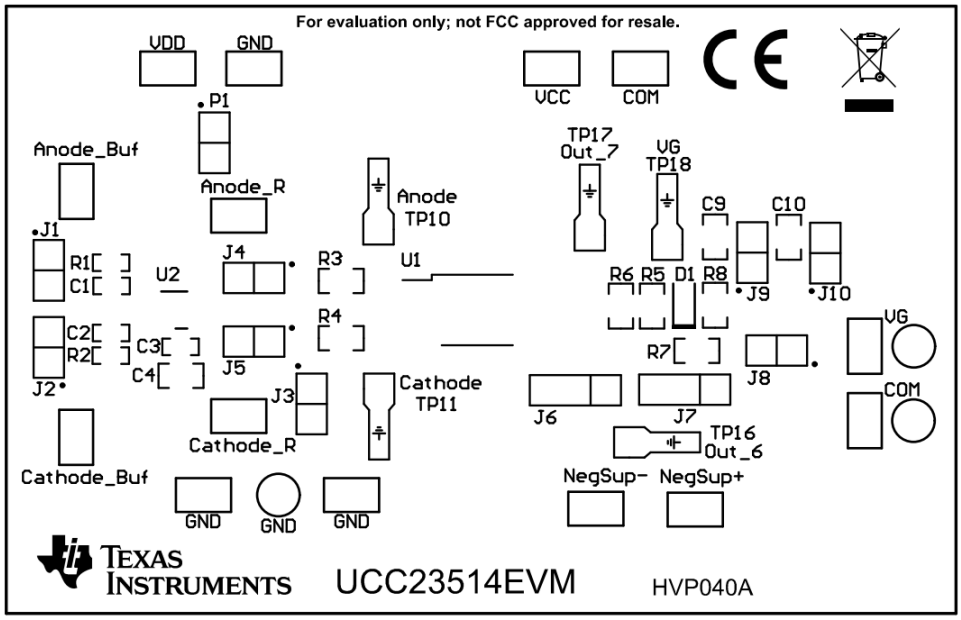

Figure 10. Top Overlay

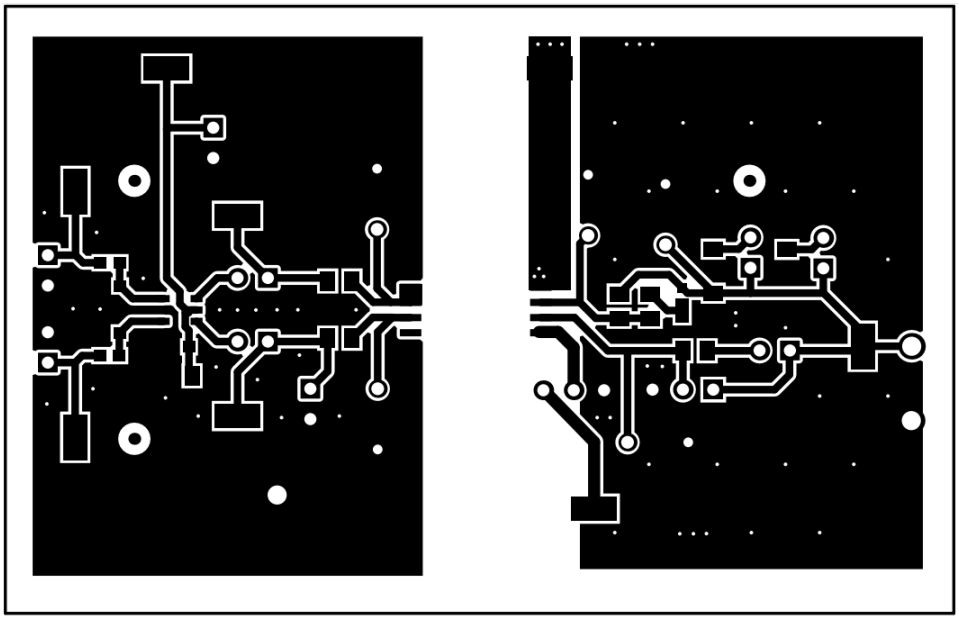

Figure 11. Top Layer

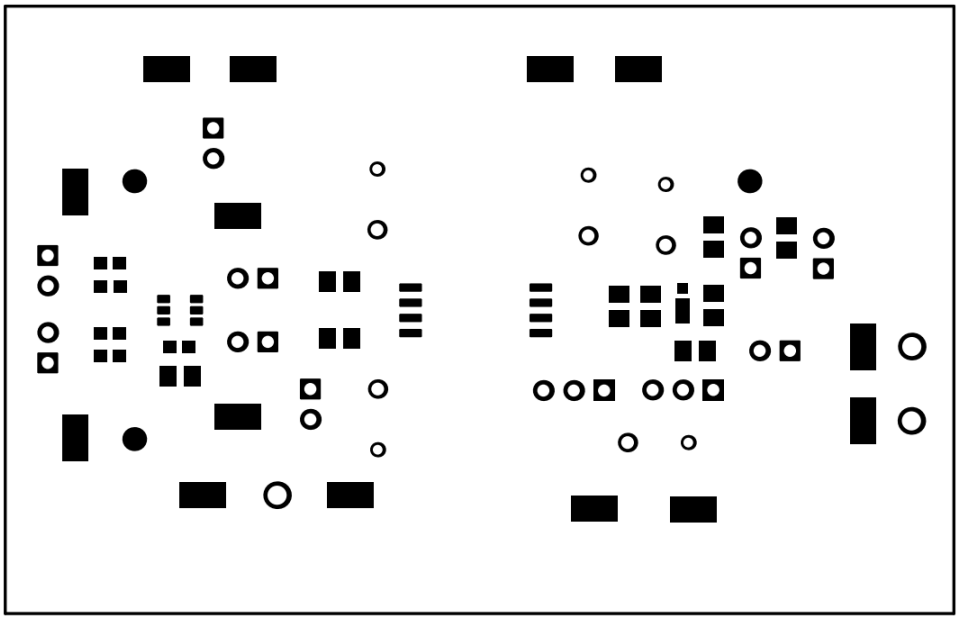

Figure 12. Bottom Overlay

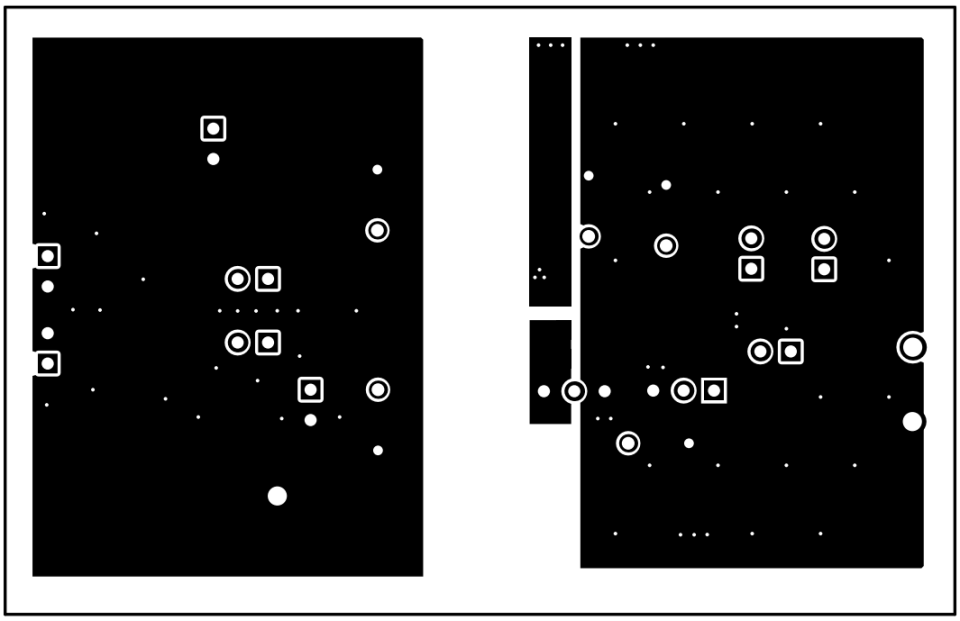

Figure 13. Bottom Layer

9 List of Materials

Table 9. UCC23514EVM List of Materials

Quantity	Designator	Description
2	C1, C2	CAP, CERM, 22 pF, 100 V, +/- 5%, C0G/NP0, 0603
1	C3	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603
1	C4	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805
2	C5, C7	CAP, CERM, 0.1 uF, 50 V, +/- 20%, X7R, 0805
2	C6, C8	CAP, CERM, 0.1 uF, 50 V, +/- 20%, X7R, 0805
1	C9	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0805
1	C10	CAP, CERM, 0.18 uF, 50 V, +/- 10%, X7R, 0805
1	D1	Diode, Schottky, 40 V, 1 A, MicroSMP
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear
9	J1, J2, J3, J4, J5, J8, J9, J10, J11	Header, 100mil, 2x1, Gold, TH
2	J6, J7	Header, 100mil, 3x1, Gold, TH
2	R1, R2	RES, 102, 1%, 0.1 W, 0603
2	R3, R4	RES, 137, 1%, 0.125 W, AEC-Q200 Grade 0, 0805
1	R5	RES, 10.0, 1%, 0.125 W, 0805
2	R6, R7	RES, 4.99, 1%, 0.125 W, 0805
1	R8	RES, 4.7 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805
6	SH-J1, SH-J2, SH-J3, SH-J5, SH-J6, SH-J7	Shunt, 100mil, Gold plated, Black
14	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP12, TP13, TP14, TP19, TP20	Test Point, Miniature, SMT
1	TP9	Test Point, Compact, Black, TH
1	U1	UCC23514M, 4-A/5-A 5KVRMS Opto Compatible Single Channel Isolated Gate Driver in 8-DWV Pkg, DWV0008A (SOIC-8)
1	U2	SN74LVC2G17, Dual Schmitt-Trigger Buffer

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