# *Switching Power Supply Design Review — 60 Watt Flyback Regulator*

by Raoji Patel and Glenn Fritz

Topic 8

# SWITCHING POWER SUPPLY DESIGN REVIEW

## 60 WATT FLYBACK REGULATOR

**By Raoji Patel and Glenn Fritz**

This paper gives a practical example of the design of an off-line switching power supply. Factors governing the choice of a discontinuous flyback topology are discussed. The design uses a pulsed-width modulation (PWM) control scheme implemented with a Unitrode UC3840 IC. This chip's voltage-feed-forward feature is used to achieve improved output regulation. The paper discusses closing the control loop to achieve both stability and adequate dynamic regulation, and provides guidelines for transformer design and component selection.

The circuit developed herein operates from a 117V (±15%), 60 Hz line and meets the following objectives:

1. Output voltages:
   a. +5V, ±5%: 2.5A-5A
      Ripple voltage: 50mV P-P maximum
   b. +12V, ±3%: 1A-2.9A
      Ripple voltage: 100mV P-P maximum
2. Efficiency: 70% minimum
3. Line isolation: 3750V

These objectives are met by using a flyback converter topology with a MOSFET power switch operating at 80kHz. The design features primary side control.

## I. SELECTION OF FLYBACK TOPOLOGY

The flyback, when compared to other switching regulator topologies, has several cost and performance advantages:

**Cost Advantages:**

1. For output power levels less than ~150W, the design of the power transformer (coupled inductor) is relatively simple.
2. Assembly costs for the flyback regulator are low due to a low overall component count. In particular, only one magnetic element (i.e., the transformer) is employed as no inductors are used in the output filters.
3. Output rectifier BV requirements are low, since they do not need to block voltages which in other topologies are developed across the filter inductor.



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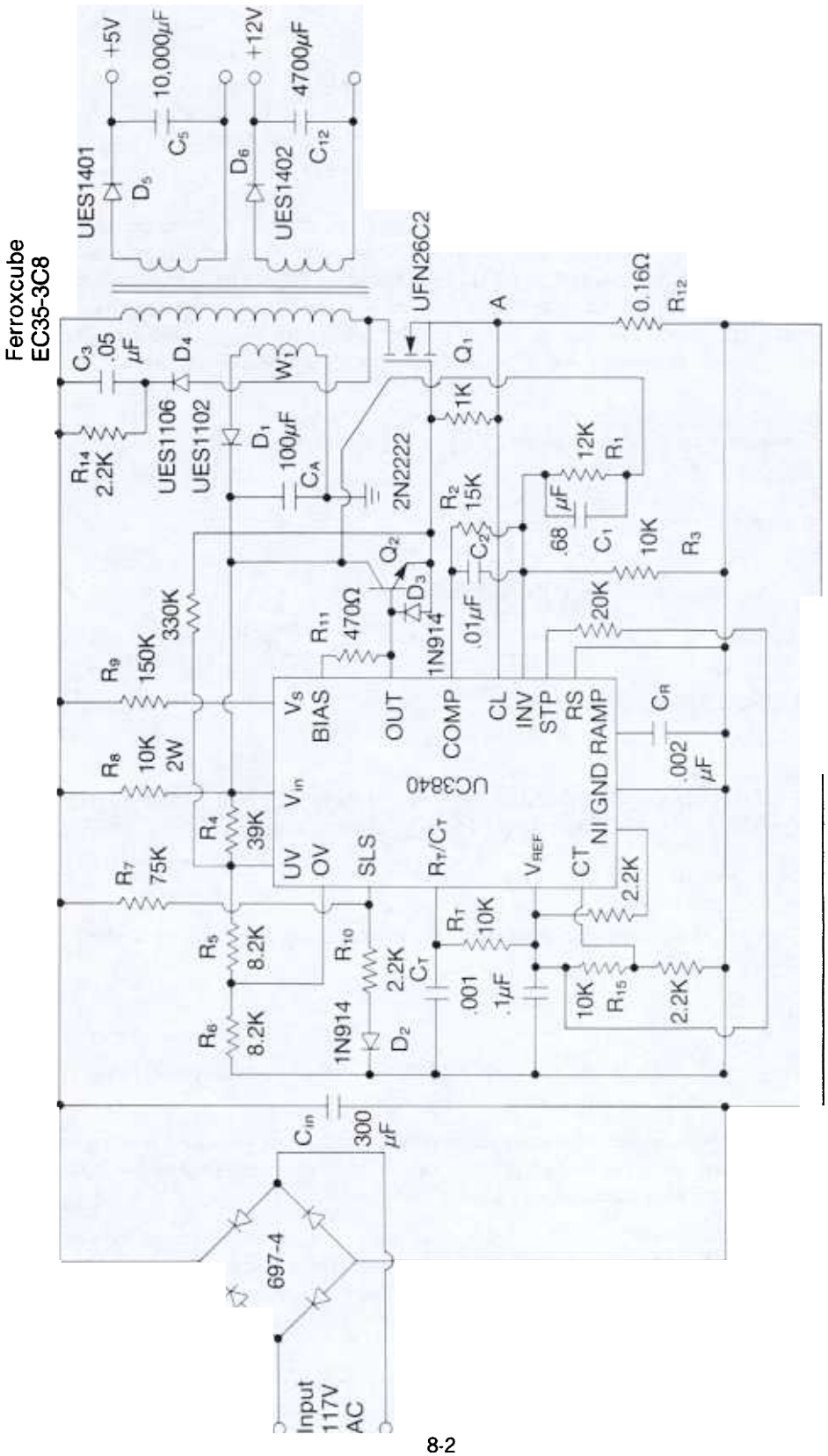



**Figure 1. 60W "Off-Line" Flyback Regulator**

**Performance Advantages:**

1. The flyback topology offers good voltage tracking in multiple output supplies due to the lack of intervening inductances in the secondary circuits.
2. Since there is no need to charge an output inductor each cycle, good transient response is achievable.

For these reasons, the flyback topology was chosen for this 60W, dual-output regulator.

**Discontinuous Current Mode**

Once a converter topology is chosen, the next decision with which the designer is faced is the choice between continuous and discontinuous current modes. Figure 2 compares primary and secondary current and transformer energy storage waveforms for these two cases.

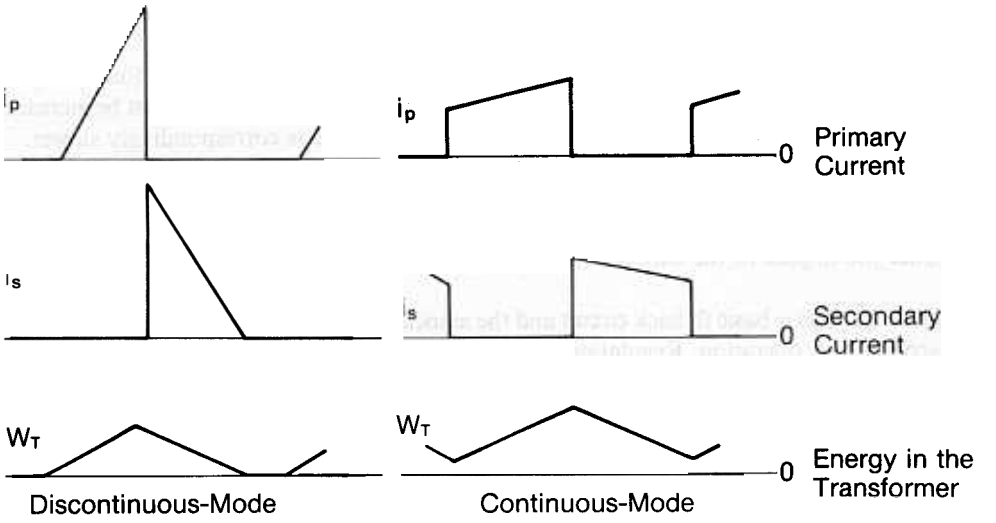



**Figure 2. Discontinuous vs Continuous Flyback Waveforms**

For the present design, a discontinuous current mode was chosen for reasons relating to component performance requirements dictated by these waveforms.

**Advantages of Discontinuous Operation:**

1. A small transformer can be used because the average energy storage ($W_T$ in Figure 2) is low. Use of fewer turns also translates into reduced $I^2R$ losses.
2. Stability is easier to achieve because at frequencies less than one half the switching frequency there is no net inductance reflected to the transformer secondary, and hence no second pole in the input-to-output transfer function. Also, no right half-plane (RHP) zero appears since energy delivered to the output each cycle is directly proportional to the power transistor on-time ($t_{on}$) for the discontinuous case.

3. Output rectifiers are operating at zero current just prior to becoming reverse biased. Therefore, reverse recovery requirements are not critical for these rectifiers.
4. Similarly, the power transistor turns on to a current level which is initially zero, so its turn-on time is not critical.
5. Transistor turn-on to zero current also results in low RFI generation.

Unfortunately, some disadvantages also accrue from the use of a discontinuous current scheme.

**Disadvantages of Discontinuous Operations:**

1. Transistor and diode peak current requirements are approximately twice what they would be in a continuous mode design. Average current requirements remain unchanged.
2. Transformer $d\phi/dt$ and leakage inductance are both high under discontinuous operation, resulting in some loss of cross-regulation.
3. High values of ripple current make output capacitor ESR requirements quite stringent. In most practical discontinuous flyback circuits, capacitance values must be increased in order to achieve adequate ESR. Transient response is correspondingly slower.

In the present design, these few disadvantages were not deemed sufficient to warrant a choice of continuous mode operation. In particular, low output current requirements (5A max.) reduce the impact of the capacitor ESR problem.

Figure 3 shows a basic flyback circuit and the associated voltage and current waveforms for discontinuous operation. Regulation is achieved by varying the duty cycle of power switch $T_1$. During the period when $Q_1$ is on, energy is transferred from input capacitor $C_{in}$ to the primary inductance $L_p$ of the transformer. The magnitude of this stored energy is given by:

$$W = \frac{1}{2} L_p i_{pp}^2 \qquad (1)$$

where $i_{pp}$ = peak primary current

No energy is transferred to the secondary circuit during this period. When $Q_1$ is off, energy stored in the transformer is delivered by way of the secondary winding to the output filter capacitor and load. The average power delivered to the load is given by:

$$P_o = \frac{W}{T} = \frac{L_p i_{pp}^2}{2T} \qquad (2)$$

where T = switching period

The peak primary current ($i_{pp}$) is dependent on the input voltage ($V_{in}$), the primary inductance $L_p$, and the on-time of $Q_1$ ($t_{on}$):

$$i_{pp} \quad \frac{V_{in}\, t_{on}}{L_p}$$

Also, the average power output is related to the output voltage and load resistance:

$$P_o = \frac{V_o^2}{R}$$

Substituting for $P_o$ and $i_{pp}$ in equation 2, one obtains:

$$\frac{V_o^2}{R_L} = \frac{V_{in}^2\, t_{on}^2}{2L_pT}$$

The DC output voltage is therefore:

$$V_o = V_{in}\, t_{on} \sqrt{\frac{R_L}{2L_pT}} = V_{in} D \sqrt{\frac{R_L T}{2L_p}} \qquad (3)$$

where duty cycle $D = \frac{t_{on}}{T}$

Note that for a discontinuous flyback, the output voltage varies directly with both $V_{in}$ and $\sqrt{R_L}$ when a conventional PWM control chip is used.

## II. SELECTION OF A CONTROL CIRCUIT

A PWM control technique is used in this design rather than a variable frequency scheme. Reasons for this decision follow, and are again related to cost and performance.

1. The transformer design can be optimized with PWM control because switching occurs at a fixed frequency.
2. Fixed frequency operation results in a narrow EMI spectrum. EMI is, therefore, filterable.
3. Output ripple under light load conditions is minimized with a PWM technique.
4. Integrated circuits are available for PWM control, while variable frequency techniques require discrete implementation. Modern PWM control ICs, such as the UC3840, also provide various auxiliary functions which further reduce the overall number of components required.
5. Implementation with PWM control allows for the use of a voltage-feed-forward technique to achieve improved output regulation and volumetric efficiency.
6. Power supply switching can be synchronized with external circuits, such as CRT amplifiers, to reduce the display interferences.

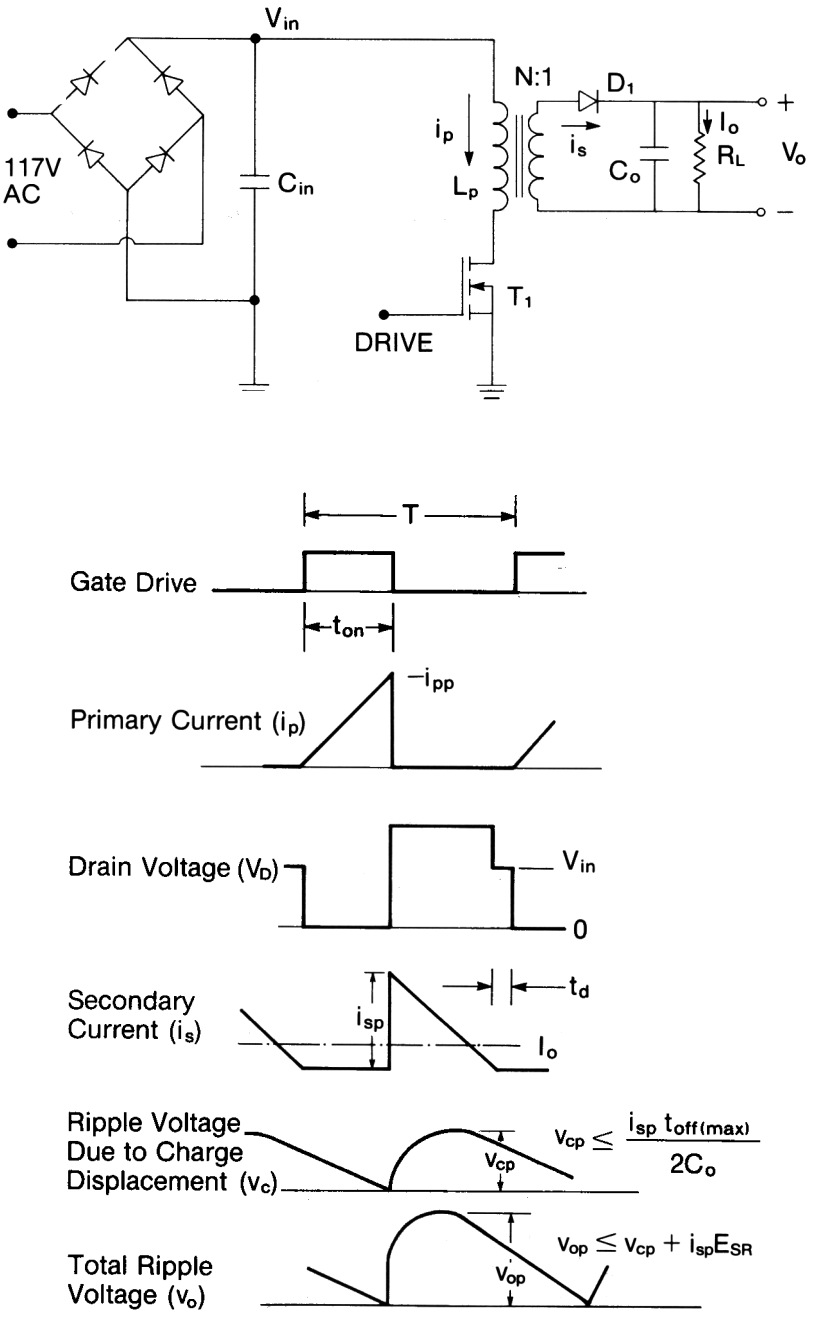



**Figure 3. Voltage and Current Waveforms, Discontinuous-Mode Flyback Regulator**

The voltage-feed-forward technique is illustrated in Figure 4. The rate of increase of the sawtooth waveform (internally generated by the PWM IC) is directly proportional to the input voltage $V_{in}$. As $V_{in}$ increases, the output pulse width (transistor on-time) decreases in such a manner as to provide a constant "volt-second" product (constant energy) to the transformer primary. Therefore, variations in $V_{in}$ do not affect output regulation. The operation of this feed-forward scheme is described by two relations:

$$V_c = \frac{V_{in}}{K}$$

where K = constant
$V_c$ = control voltage
$V_s$ = P-P sawtooth voltage

$$D = \frac{t_{on}}{T} = \frac{V_c}{V_s} = \frac{KV_c}{V_{in}}$$

Application of these relations to equation 3 yields the following as the open-loop response of the voltage-feed-forward discontinuous flyback regulator:

$$V_o = KV_c \sqrt{\frac{R_L T}{2L_p}} \qquad (4)$$

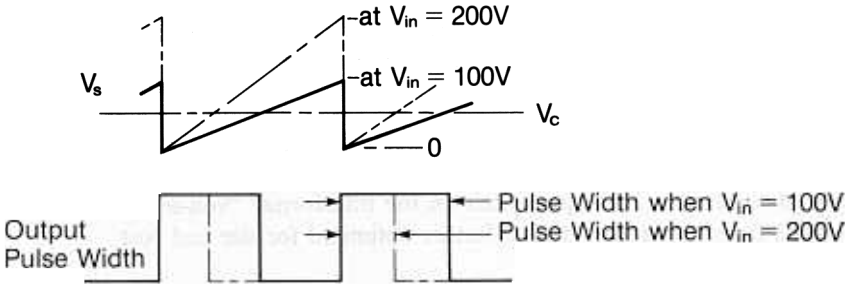



**Figure 4. Voltage-Feed-Forward Technique**

Note that the output voltage is independent of $V_{in}$, but varies directly with $\sqrt{R_L}$. Figure 5 shows the open-loop dependence of $V_o$ on $V_{in}$ and $R_L$ for both conventional PWM and feed-forward controls. The curves show experimental results, and are in good agreement with equations 3 and 4. Deviations from flat response in the feed-forward case are due to variations in the MOSFET turn-off delay time, $t_{d(off)}$.

Freedom of $V_o$ from $V_{in}$ dependence minimizes the error amplifier gain requirement while maintaining adequate output regulation. In addition, the audio susceptibility of the feed-forward implementation is good due to the cycle-by-cycle compensation for input voltage variations.

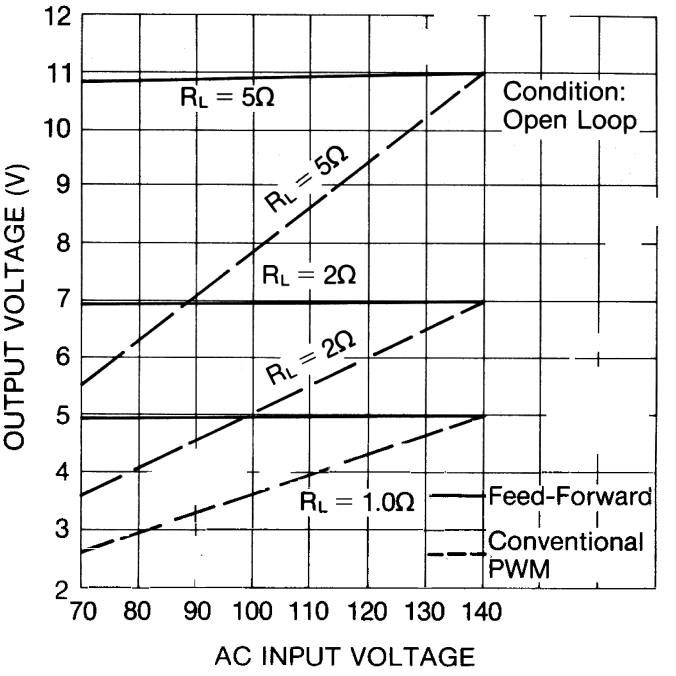


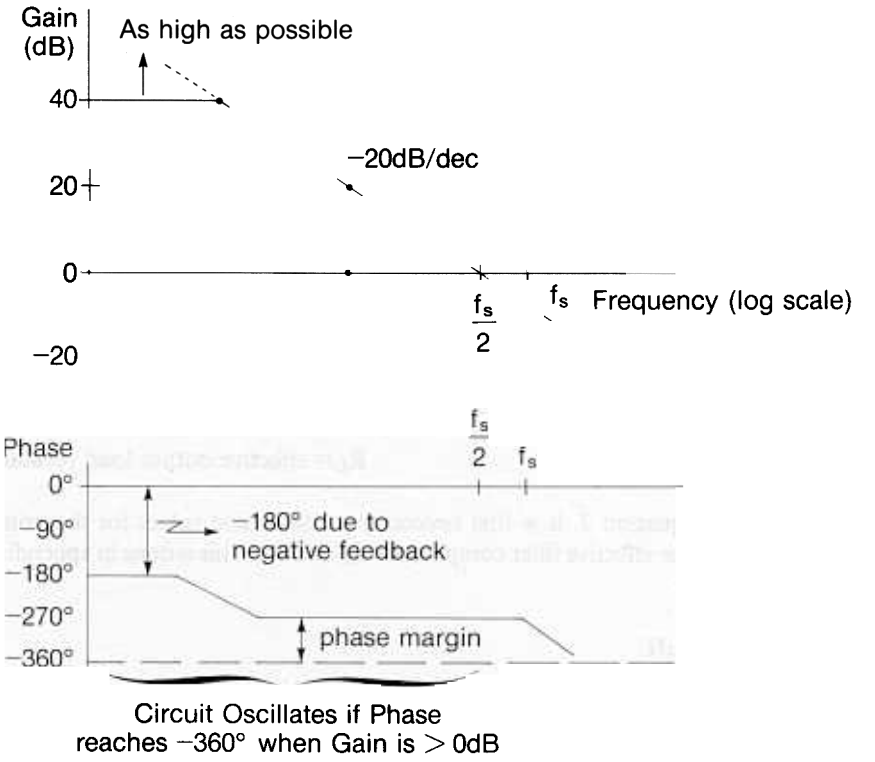

**Figure 5. Comparison between Voltage-Feed-Forward and Conventional PWM Operation (Experimental Results)**

The UC3840 IC provides a terminal which can be used to clamp the control signal internally to any desired level. When used in conjunction with the feed-forward circuitry, this feature allows the designer to set an upper limit on the transformer "volt-second" product. The design of the transformer can then be further optimized for size and cost.

## III. CLOSING THE LOOP

The 60W regulator utilizes a primary side control technique wherein an auxiliary transformer winding on the primary side is used to develop a control voltage which is fed back to the PWM error amplifier. External compensation of this amplifier gives the designer control over the closed-loop frequency response of the entire system. The objectives in designing the error amplifier compensation are to insure circuit stability while achieving adequate dynamic output regulation. Figure 6 illustrates an optimum practical open-loop frequency response for a switching regulator.

Good DC and transient regulation requires high closed loop gain at frequencies below $f_s/2$. Signals at higher frequencies do not contribute to regulation because they are "sampled" at too low a rate by the circuit. Unwanted oscillation results if the closed-loop phase reaches $-360°$ at any frequency for which the gain is greater than 0dB. Conservative designs should maintain a 45° phase margin above $-360°$ at these frequencies. In practice, this criterion is most easily met if the 0dB gain cross-over point is at as low a frequency as possible. To compromise between transient response and stability requirements, the 0dB cross-over is usually designed to occur near $f_s/2$.




## Figure 6. Desired Closed-Loop Response

In order to determine the error amplifier response required to stabilize the 60W regulator, while achieving the desired regulation, the small-signal open-loop response of the PWM modulator and the power output stage is first determined. The DC response, as previously developed, is:

$$V_o = KV_c \sqrt{\frac{TR_L}{2L_p}} \tag{5}$$

For low frequencies, the small signal variation in output voltage is obtained by differentiating equation 5 with respect to $V_c$:

$$\frac{dV_o}{dV_c} = K \sqrt{\frac{TR_L}{2L_p}} \tag{6}$$

The effective output capacitance $C_E$ and load resistance $R_L$ form a low-pass filter which causes additional attenuation above the break frequency of the filter. The overall control-to-output transfer function is:

$$\frac{v_o}{v_c} = K\sqrt{\frac{TR_L}{2L_p}}\left(\frac{1}{(s/\omega_0 + 1)}\right) \tag{7}$$

where $\omega_0 = \dfrac{2}{R_L C_E}$

$$K = \frac{V_{in(min)}}{V_s}$$

$C_E$ = effective output capacitance

$R_L$ = effective output load resistance

In order to evaluate equation 7, it is first neccesary to determine values for the primary inductance $L_p$ and for the effective filter components $C_E$ and $R_L$. This is done in appendices I and II. The results are:

$L_p = 165\mu H$
$C_E = 4500\mu F$
$R_{L(min)} = 2.40\Omega$
$R_{L(max)} = 5.88\Omega.$

For purposes of graphing the control-to-output transfer function, it is only necessary to determine the DC gain and the filter cutoff frequency.

**DC Gain:**

$$\frac{v_o}{v_c} = K\sqrt{\frac{TR_L}{2L_p}} = \frac{V_{in(min)}}{V_s}\sqrt{\frac{TR_L}{2L_p}}$$

$$\left.\frac{v_o}{v_c}\right|_{DC,\ max.\ load} = \frac{100V}{3.5V}\sqrt{\frac{(12.5\mu s)\ (2.40\Omega)}{2\ (165\mu H)}} = 8.6 = 18.7dB$$

$$\left.\frac{v_o}{v_c}\right|_{DC,\ min.\ load} = \frac{100V}{3.5V}\sqrt{\frac{(12.5\mu s)\ (5.88\Omega)}{2\ (165\mu H)}} = 13.4 = 22.5dB$$

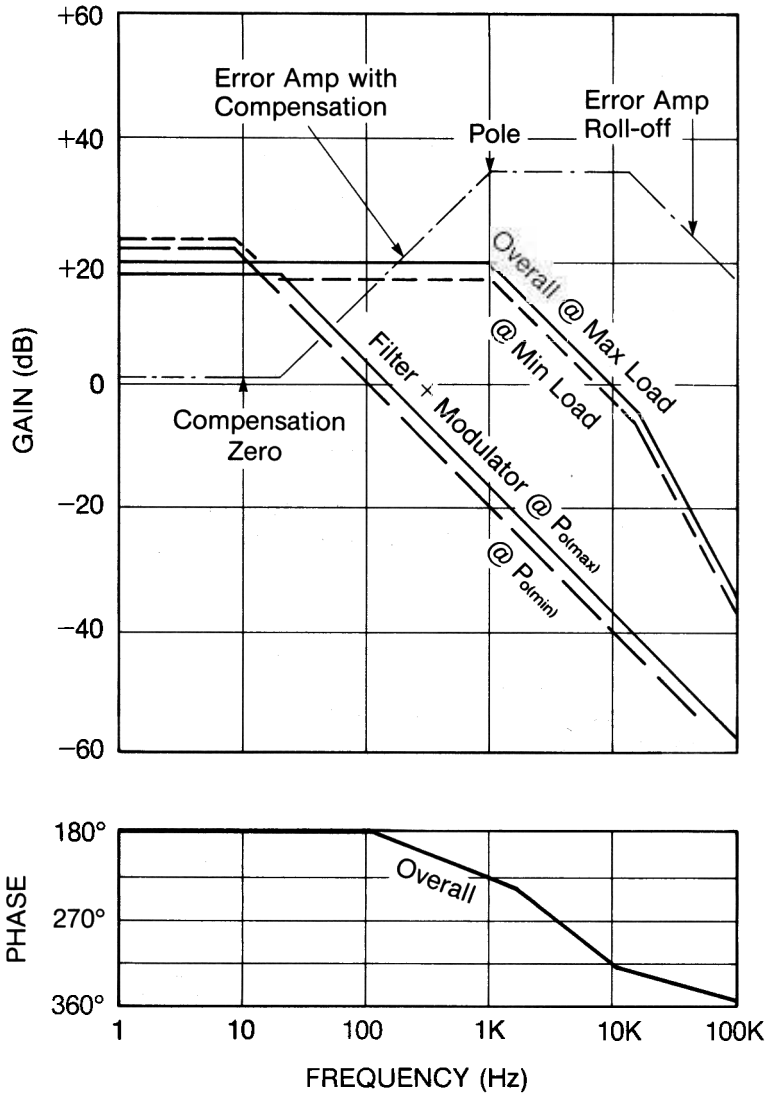
**Cutoff Frequency:**

The transfer function break frequencies for maximum and minimum load conditions are:

$$f_1\ (P_{o(max)}) = \frac{2}{2\pi\ 2.4\Omega\ 4500\mu F} = 29.5\ Hz$$

$$f_1\ (P_{o(min)}) = \frac{2}{2\pi\ 5.8\Omega\ 4500\mu F} = 12.2\ Hz$$

The resulting frequency response is illustrated in Figure 7A.




## Figure 7A. Gain and Phase Plots

Figure 7B shows the open-loop error amplifier response for the UC3840. The gain plot can be thought of as representing an upper limit on the gain response of the error amplifier when compensated. Note that at frequencies above ~15kHz, the closed-loop gain (filter + modulator + error amplifier) would be less than 0dB even if compensation networks did not cause further attenuation. Therefore, a 40kHz gain cross-over is not obtainable with this particular design. We chose 15kHz as a best case practical 0dB point.

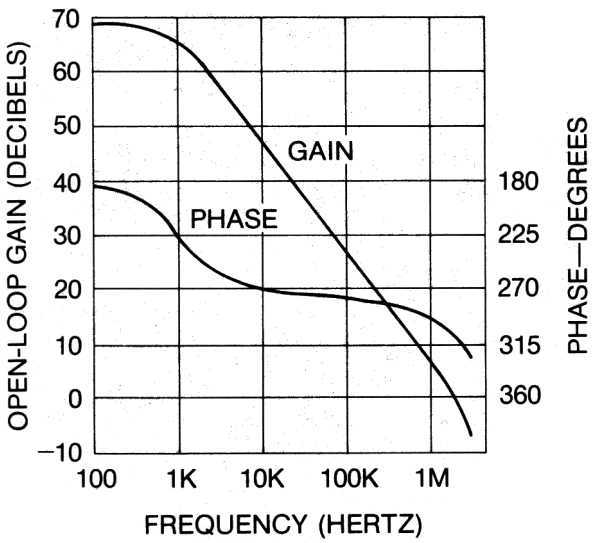



**Figure 7B. Open-Loop Response of UC3840 Error Amplifier**

In order to obtain adequate gain below 15kHz, a zero is needed in the closed-loop response near 20 Hz in order to compensate for the low frequency filter pole. The desired response of the compensated error amplifier is shown in Figure 7A. Also shown is the resulting overall closed-loop response. Figure 8 shows the error amplifier with the compensation elements required to achieve this response.

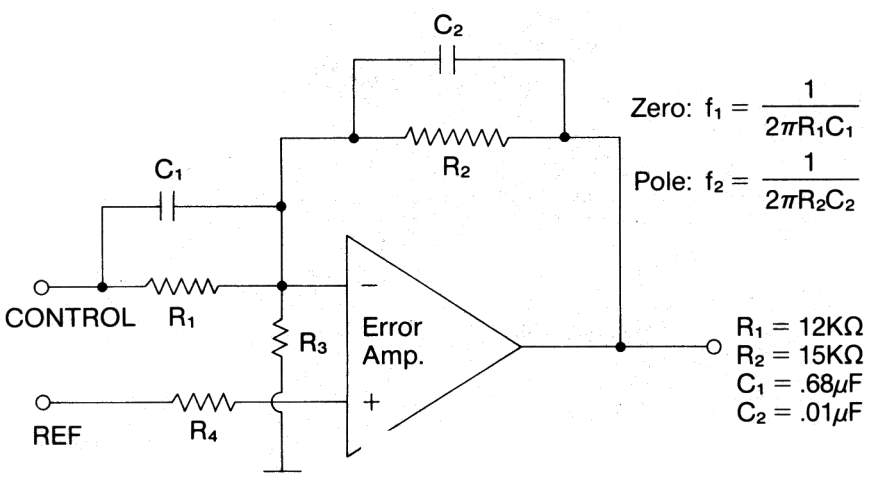



**Figure 8. Error Amplifier with Compensation**

## IV. DESIGN DETAILS AND PERFORMANCE (Refer to Figure 1)

The AC input voltage for this supply is rectified with a full-wave bridge and filtered by input capacitor $C_{in}$. The UC3840 control chip is equipped with under- and over-voltage lockout features. The under-voltage feature initially disables all internal circuits except the (low current) reference voltage circuit. The lockout voltage is set by divider network $R_4$-$R_5$-$R_6$ in Figure 1. This feature allows capacitor $C_A$ to charge through $R_8$ and to store enough energy to power the drive circuitry. The UC3840 under-voltage lockout has built-in hysteresis to prevent hesitant start-up.

After the control IC is enabled, drive energy is provided each cycle from an auxiliary primary side transformer winding $W_1$. In conjunction with $C_A$ and diode $D_1$, this winding forms a regulated 12V drive supply. This supply is also used to provide primary-side control for the 5 and 12V outputs. This voltage is fed to the UC3840 control input through $R_1$. This low-cost control scheme is not optimum in terms of output coupling, but, with a careful transformer design, ±2% regulation is still achievable.

The UC3840 operates at a fixed frequency $f_s = 1/(R_TC_T)$. This frequency is independent of the ramp slope, which varies directly with input voltage $V_{in}$, to provide voltage-feed-forward compensation. This ramp slope variation is accomplished as follows. Control chip input $V_s$ is no more than one forward-biased diode drop above ground. Therefore, the current through $R_9$ is almost directly proportional to $V_{in}$. This current is fed internally to a current mirror which in turn drives ramp-control capacitor $C_R$ at a charging rate proportional to $V_{in}$. Ramp linearity is better than 2%.

In order to optimize the transformer, it is desirable to limit the maximum duty cycle, as previously mentioned. This is accomplished with the UC3840 by clamping the control voltage to a level determined by voltage divider $R_7$-$R_{10}$ and diode $D_2$.

Transistor $Q_2$ and diode $D_3$ provide a low impedance drive for fast switching of power FET $Q_1$. An internal transistor always pulls the UC3840 bias output to a level near supply voltage $V_c$ unless the under-voltage lockout is active. When the open-collector control chip output is high, then drive to $Q_2$ is provided from the bias output through $R_{11}$. In this way the input capacitance of $Q_1$ is quickly charged for fast turn-on. This input capacitance is discharged through $D_3$ at turn-off.

The UC3840 also provides dynamic current limiting to protect costly power components. Primary current flows through $R_{12}$ to develop a current-limit input signal at point A. This signal is compared to a reference signal established by $R_{15}$ and $R_3$. When the current-limit signal exceeds this reference by 400mV, an internal error latch forces the PWM output low but leaves the bias output enabled. Capacitor $C_A$ discharges through $R_{11}$ until the under-voltage feature is activated, turning off the bias transistor. Not until this time does the control chip attempt a restart.

The snubber network $R_{14}$-$C_2$-$D_4$ prevents turn-off voltage spikes from exceeding the FET breakdown voltage. This snubber does not provide load-line shaping.

Power FET $Q_1$ and output rectifiers $D_5$ and $D_6$ are all in TO-220 packages to provide high volumetric efficiency. The rectifiers were chosen for fast forward recovery to minimize

switching losses. The higher-current 5V output utilizes a Schottky rectifier for low forward-biased power dissipation. The power FET provides fast switching when driven with the simple, efficient circuit already described.

Figure 9 shows the output regulation achieved with this design. Note that loading one output effects the regulation of the other output. This results from changes in the energy stored in the transformer leakage inductance. Transient response is shown in Figure 10.

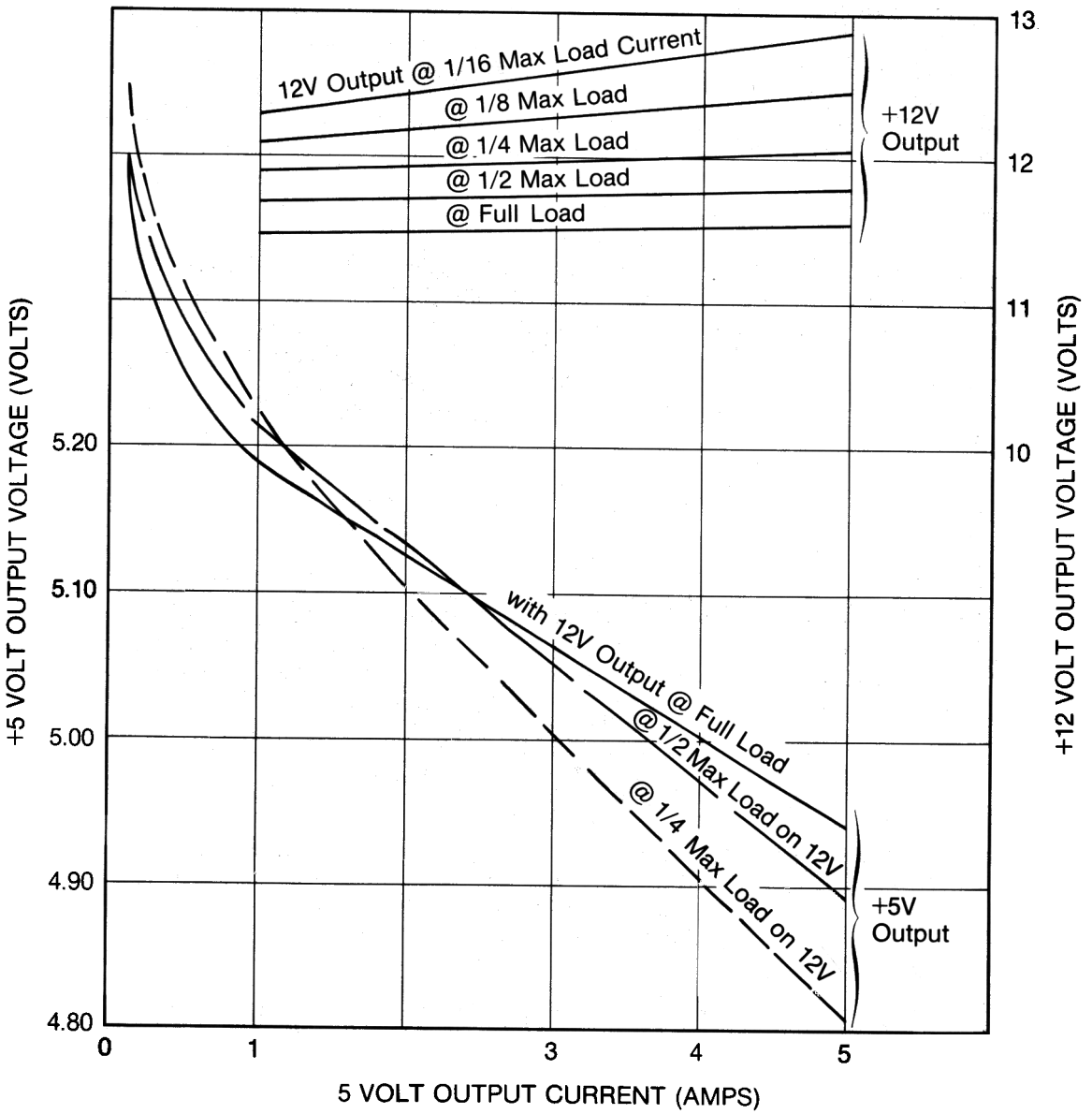



**Figure 9. Output Load Regulation**

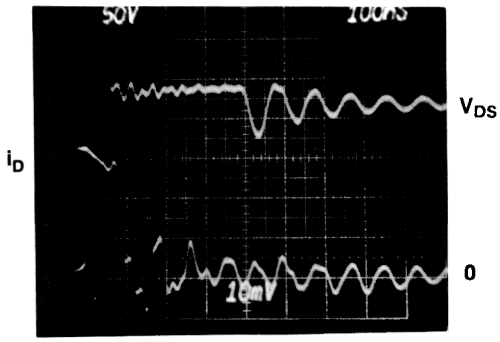



Figure 10A. Drain Voltage and Current Waveform Showing the Effect of the De-Spiking Network

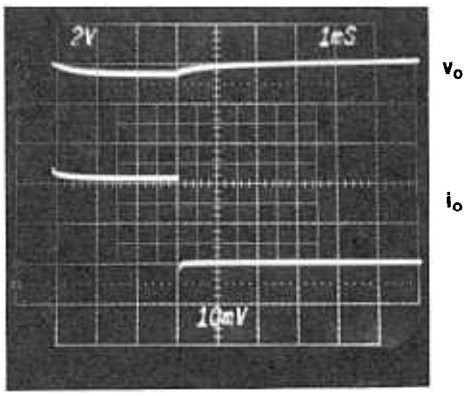



Figure 10B. Transient Response: Step Change of Load Current from 1A to 3A in +12V Output

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