*Application Note*

# *Insulation Resistance Detection Designs in GESS-BMS*

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**ABSTRACT**

This application note summarizes the design requirements in the high voltage 1500V system according to the existing energy storage regulations, analyzes the current mainstream bridge insulation monitoring topology, compares the accuracy, cost and monitoring time in multiple dimensions, summarizes three designs. Simulates the three designs sampling time, and conducts experimental verification for accuracy of the low-cost design.

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## Trademarks

# 1 Introduction

Energy storage power station is a complex industrial system, involving energy storage converters, energy storage batteries and management systems and other electrical equipment, so to avoid system short circuit, Or the leakage current is high, to the user, so the insulation inspection system of the energy storage power station is critical to the safety of the energy storage power station operators. At the same time, insulation monitoring can also avoid insulation failure damage to end equipment, improve the service life of the equipment.

If you can make sure that the insulation is good enough when you touch any two points, then safety can be improved. When the energy storage system is operating, the positive side of Figure 1-1 represents the positive side of the high voltage battery pack, the negative side represents the negative side of the high voltage battery, and the PE represents the enclosure. RisoP is the equivalent resistance between the high voltage negative and the enclosure, RisoN is the high voltage positive and the enclosure equivalent, V1 stands for the voltage between the high voltage negative and the enclosure as monitored by the BMS and V2 stands for the voltage between the high voltage positive and the enclosure as monitored by the BMS; if any one of he resistance values of RisoP or is RisoN is designed for greater than the threshold specified by the national standard, then the human body is safe despite mistakenly touching any two place of the high voltage positive, high voltage negative and enclosure .

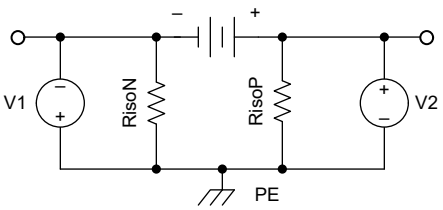


**Figure 1-1. Insulation System in Energy Storage System**

For the system performance of the energy storage system, GB/T34131 gives some indicators on voltage, current, temperature sampling and insulation resistance monitoring:

**Table 1-1. Requirements for Voltage, Current, Temperature, Insulation Resistance Accuracy in GB/T34131**

| | Scope | Error | Period |
|---|---|---|---|
| Battery cell voltage | <5V | ≤0.005V | ≤100ms |
| | 5 approximately 15V | ≤0.2% | |
| Battery cluster voltage | <500V | ≤5V | ≤100ms |
| | ≥500V | ≤1% | |
| Battery cluster current | <200A | ≤2A | ≤50ms |
| | ≥200A | ≤1% | |
| Cell temperature | -20 approximately 65 | ≤1℃ | ≤1s |
| | [-40,-20)U(65,125] | ≤2℃ | |
| Insulation resistor(≥400V) | R≤75kΩ | ≤±15kΩ | |
| | R>75kΩ | ≤±20% | |

Creepage distances and electrical clearances are also important areas of focus in the design of energy storage insulation monitoring. In the European market in the energy storage sector, suppliers mainly refer to IEC62619, in the North American market, the main supplier reference regulation is UL1973, The electrical clearance and creepage distances sections of both regulations are referenced to IEC60664. This paper therefore summarizes electrical clearance and creepage distances for 1000V/1500V/2000V systems in IEC60664.

**Table 1-2. Creepage Distance and Clearance Requirements in 1000V Energy Storage Systems**

| Voltage | Type | Pollution degree | CTI | OVC | Altitude/m | CLR/mm | CRP*/mm |
|---|---|---|---|---|---|---|---|
| 1000V | Basic | II | I | OVC-II(6000) | <2000m | 5.5 | 5.5 |
| | | | | | 4000m | 7.1 | 7.1 |
| | | | | OVC-III(8000) | <2000m | 8 | 8 |
| | | | | | 4000m | 10.4 | 10.4 |
| | Reinforced | | | OVC-II(8000) | <2000m | 8 | 8 |
| | | | | | 4000m | 10.4 | 10.4 |
| | | | | OVC-III(12000) | <2000m | 14 | 14 |
| | | | | | 4000m | 18.1 | 18.1 |

**Table 1-3. Creepage Distance and Clearance Requirements in 1500V Energy Storage Systems**

| Voltage | Type | Pollution degree | CTI | OVC | Altitude/m | CLR/mm | CRP*/mm |
|---|---|---|---|---|---|---|---|
| 1500V | Basic | II | I | OVC-II(8000) | <2000m | 8 | 8 |
| | | | | | 4000m | 10.4 | 10.4 |
| | | | | OVC-III(10000) | <2000m | 11 | 11 |
| | | | | | 4000m | 14.2 | 15.1 |
| | Reinforced | | | OVC-II(12000) | <2000m | 14 | 15.1 |
| | | | | | 4000m | 18.1 | 18.1 |
| | | | | OVC-III(16000) | <2000m | 19.4 | 19.4 |
| | | | | | 4000m | 25.1 | 25.1 |

GB/T 34131 also requires insulation voltage tests and dielectric strength test. Take 1500V BMS as an example, Insulation voltage testing refers to following four places(①②③④) shall withstand 1500V DC voltage Lasts one minute and the insulation resistance value shall not be less than 10MΩ.

- Between the battery-connected acquisition terminal and the ground terminal.
- Between the communication terminal and the earth terminal.
- Between the acquisition terminal and the communication terminal.
- Between the supply terminal and the communication terminal.

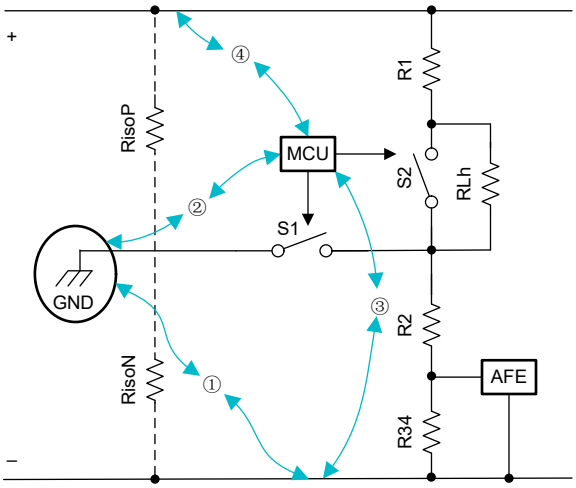


**Figure 1-2. Insulation voltage tests**

Dielectric strength test refers to following five places(①②③④⑤) shall withstand a DC voltage of 4380V for 1 minute, there needs to be no insulation breakdown and flashover and leakage current needs to be less than 10mA.

- Between the battery-connected sampling terminal and the ground terminal.

- Between the communication terminal and the ground terminal.
- Between the sampling terminal and the supply terminal.
- Between the sampling terminal and the communication terminal.
- Between the supply terminal and the communication terminal.

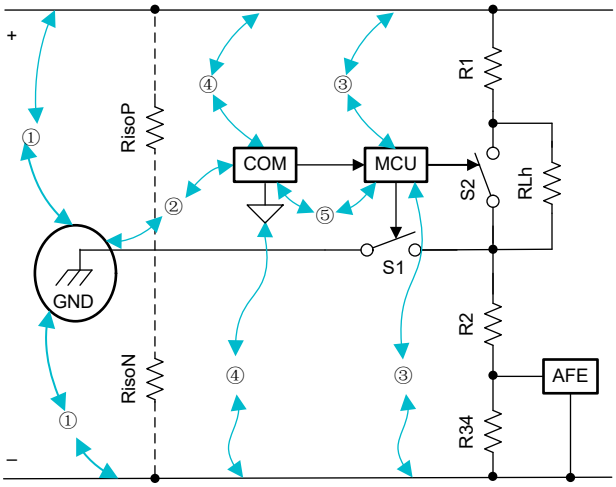


**Figure 1-3. Dielectric strength tests**

Test tips:

1. Non-electrification, disconnect PE, HV and communication;
2. While do ① test, between HV(BAT+/BAT-) and PE, circuit needs to withstand 5880V(4380V+1500V), because battery cluster voltage is included in.

# 2 Topologies for Insulation Monitoring in ESS

Currently, the methods used for insulation monitoring in the energy storage field are mainly external resistance method and AC injection method.

The AC current injection method generates a square wave signal which is then injected into the RC circuit between the HV line and the Protective Earth (PE) through an RC filter or transformer. The impedance is calculated based on the charge and discharge of the capacitor. The main drawbacks of AC injection are that the signal is susceptible to interference, difficult to achieve a reliable and accurate design, and that a large transformer is required to isolate the injection circuit from the HV circuit. The advantage of the AC current method is that it is not affected by the isolation capacitance.

The external resistance method connects a series of resistors between the positive and negative poles, using the set switch on and off in the circuit, the voltage value on the resistance in both states can be obtained by listing the circuit status equation. The two equations are combined to determine the positive and negative battery resistance values to ground and determine the positive and negative battery insulation.

The topology of the external resistance insulation monitoring method is mainly different in how many switches and whether or not to use isolating devices, according to the number of switches divided into single and double switches. Depending on whether the control is put on the high or low side

## 2.1 Single Switch Topology

Use topo1-one switch to detect insulation. Sampling is put in the high voltage side, where S1 can use reed relay, signal relays, etc. which can withstand high voltage. S2 can choose solid state relays or Photo MOS and controlled by UIR.

According to the ESS regulations, the dielectric strength test refined to the withstand voltage or isolation requirements of the device as follows:

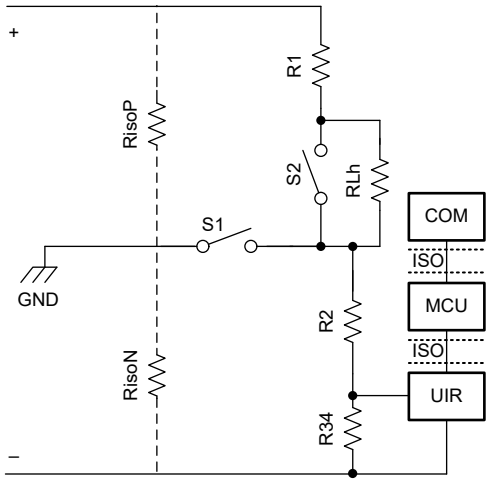


**Figure 2-1. Single Switch Topo(topo1)**

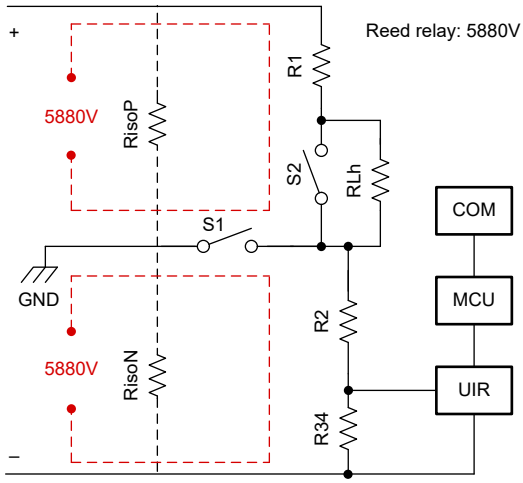


**Figure 2-2. Topo1-HV(BAT+/BAT-) and PE①5880V**

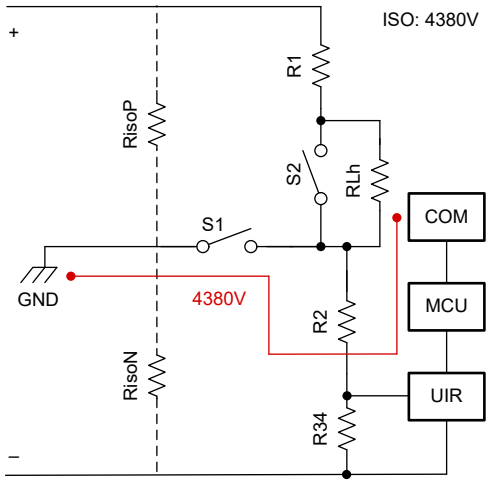


**Figure 2-3. Topo1-Communication and PE②4380V**

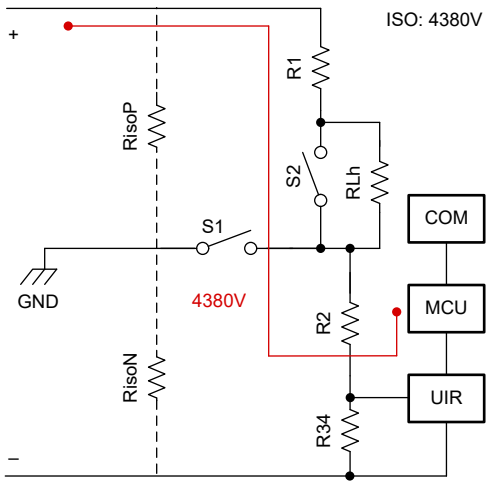


**Figure 2-4. Topo1-HV and LV(MCU)③4380V**

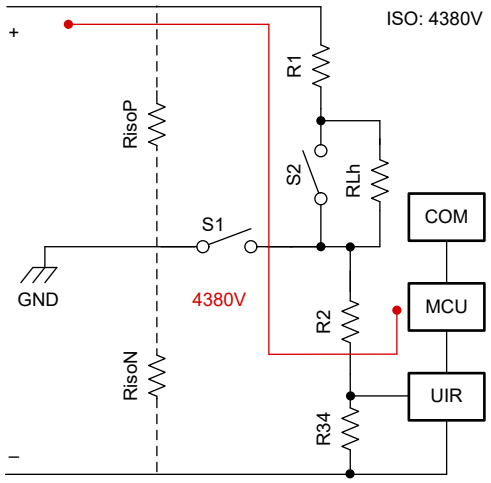


**Figure 2-5. Topo1-HV and Communication④4380V**

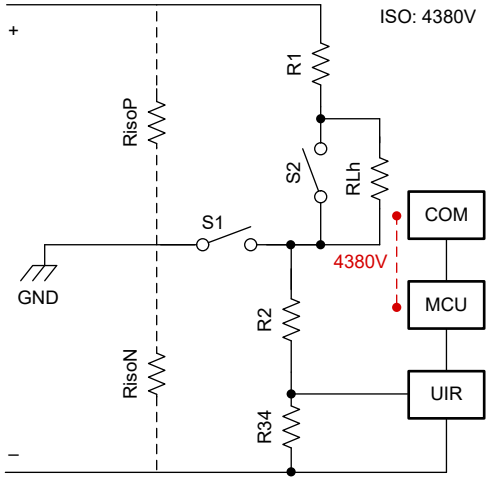


**Figure 2-6. Topo1-LV and Communication⑤4380V**

**Table 2-1. Maximum Device Spec**

| Device Spec | Withstand voltage(V) |
|---|---|
| Reed relay | 5880V |
| Isolator | 4380V |

### *2.1.1 Test Steps*

1. Close S1, S2 and wait voltage at ADC to settles (500us), get *VN* **1**, $V_{DC}$=2*VN* $_1$.
2. Open SW1 and close SW2、SW3 (400us delay) , wait until voltage at ADC settles (500us), get *VN* $_{off}$.
3. Close SW1 , wait until voltage at ADC settles (500us), get *VN* $_{on}$.
4. Calculate *Riso*P and *Riso*N (use following formula).

$$\mathrm{RisoP} = \frac{\mathrm{VDC}(\mathrm{VNon} - \mathrm{VNoff})}{(\mathrm{VDC} - \mathrm{VNon}) \times \frac{\mathrm{VNoff}}{\mathrm{R1}} - (\mathrm{VDC} - \mathrm{VNoff}) \times \frac{\mathrm{VNon}}{\mathrm{R1} + \mathrm{RL}}} \quad (1)$$

$$\mathrm{RisoN} = \frac{VNon}{(VDC - VNon)\left(\frac{1}{R1} + \frac{1}{RisoP}\right) - VNon\left(\frac{1}{R34 + R2}\right)} \quad (2)$$

The error of the injection resistance, the error of the sampling resistance, and the error of the high voltage detection are taken into account in the calculation formula, the worst accuracy is obtained:

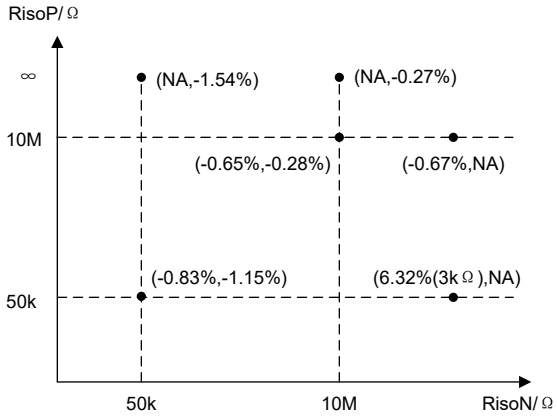


**Figure 2-7. Worst Case for Topo 1**

## 2.2 Dual Switch Floating Sampling Topology

Use topo2-dual switch, sampling ADC located on the low voltage side with isolated operational amplifier for high-voltage sampling and insulation monitoring. Withstand voltage or isolation requirements of the device as follows:

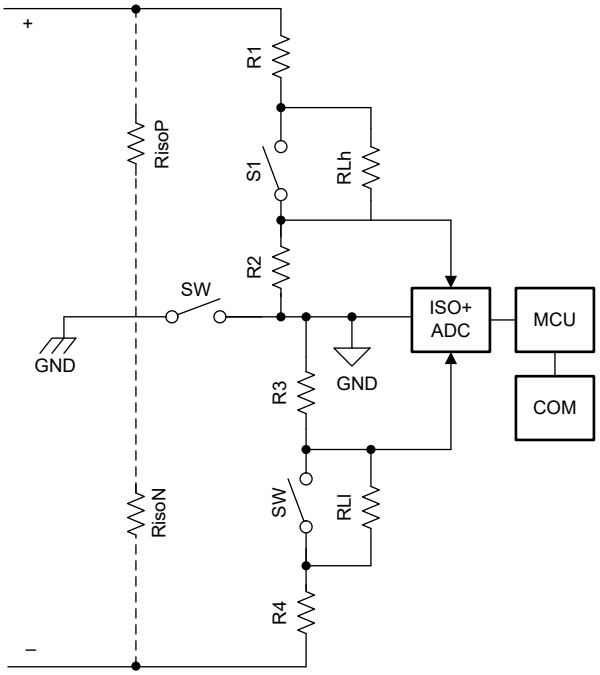


**Figure 2-8. Dual Switch topo, Sampling GND Float(topo2)**

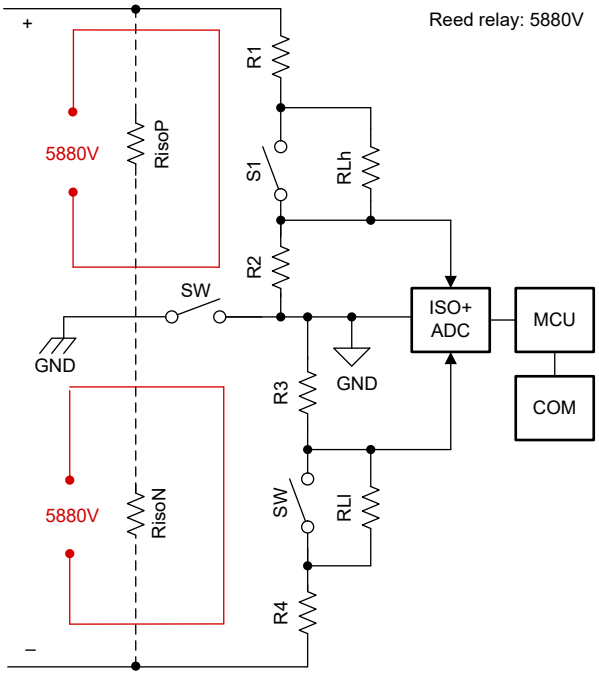


**Figure 2-9. Topo2-HV(BAT+/BAT-) and PE①5880V**

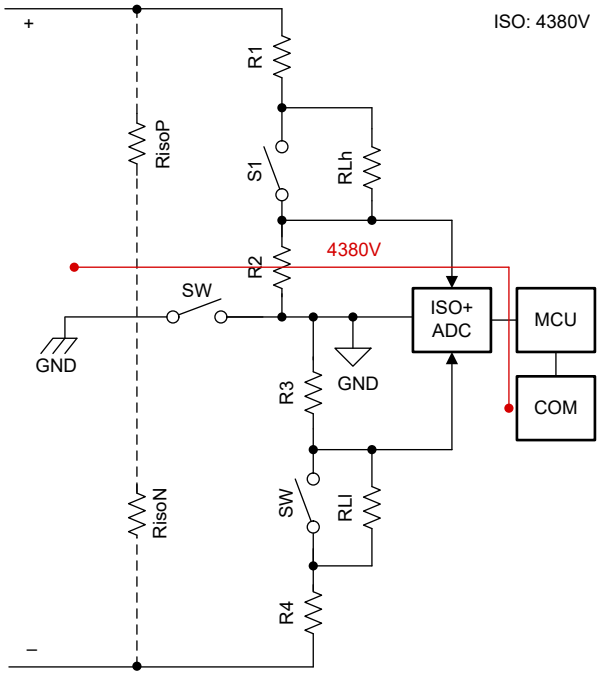


Figure 2-10. Topo2-Communication and PE②4380V

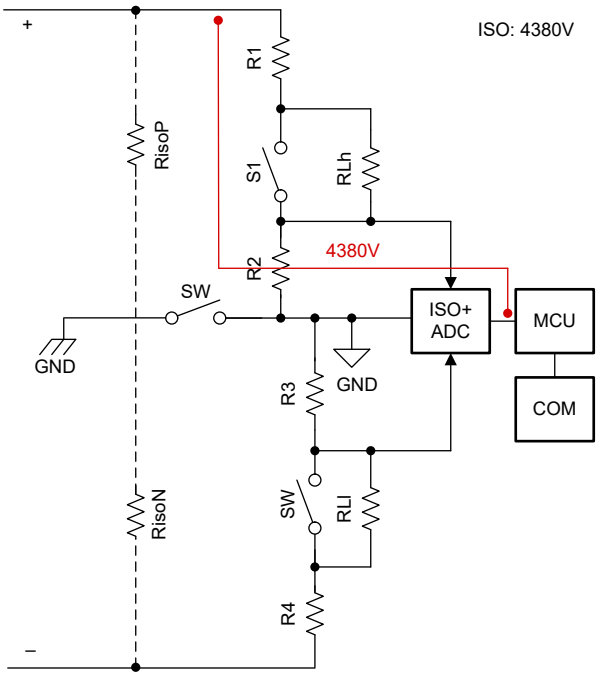


Figure 2-11. Topo2-HV and LV(MCU)③4380V

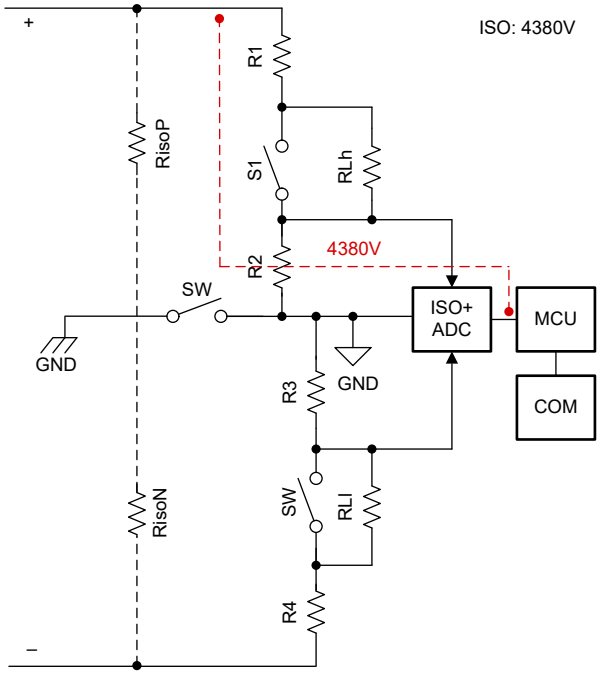


Figure 2-12. Topo2-HV and communication④4380V

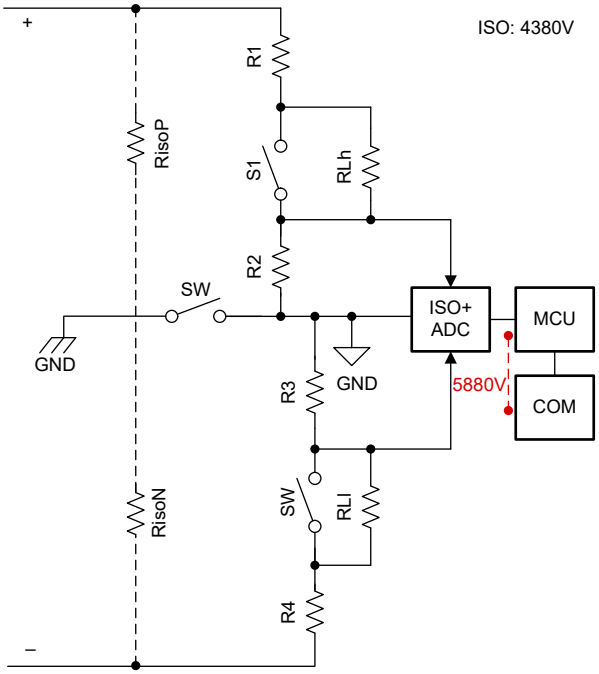


Figure 2-13. Topo2-LV and Communication⑤4380V

### *2.2.1 Test Steps*

1. Close SW1 and SW3, open SW2, get V+.
2. Close SW2 open SW1, get V-.
3. Put V+ and V- into Risop and RisoN calculate formula.

Based on the operating mode of the two circuits, the formula for calculating RisoP and RisoN is as follows:

$$Rp = \frac{VDC + VBn1 - \frac{VBn1 \times VBp}{VBp - VDC}}{\frac{VBn1}{R3 + R4 + RL1} + \frac{VBp \times VBn1}{(R1 + R2) \times (VBp - VDC)} - \frac{VDC + VBn1}{R1 + R2 + RLh} - \frac{VBn1}{R3 + R4}} \quad (3)$$

$$Rn = \frac{-1}{\frac{1}{R3 + R4 + RL1} + \frac{VBp}{(R1 + R2) \times (VBp - VDC)} + \frac{VBp}{Rp \times (VBp - VDC)}} \quad (4)$$

The error of the injection resistance, the error of the sampling resistance, and the error of the high voltage detection are taken into account in the calculation formula, the worst accuracy is obtained:

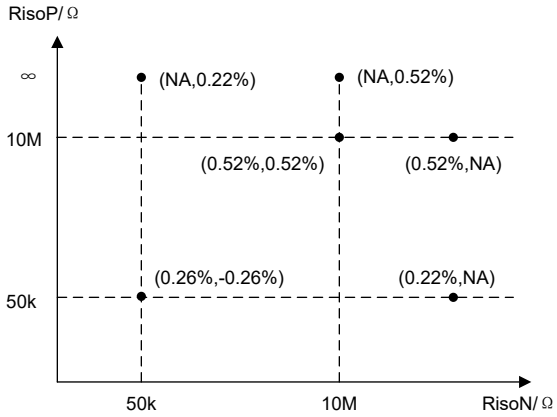


**Figure 2-14. Worst Case for Topo 2**

## 2.3 Dual Switch Sampling in High Voltage Side Topology

Use topo3-dual switch, sampling ADC and control signal put on the high voltage side with isolated operational amplifier for high-voltage sampling and insulation monitoring. Topo and device requirement based on dielectric strength as following:

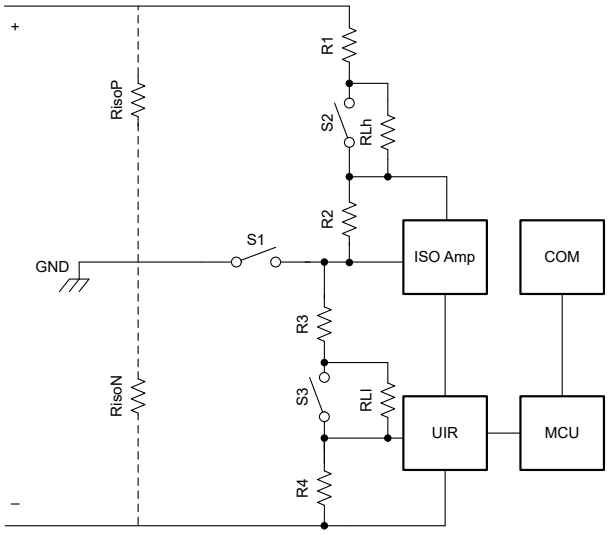


**Figure 2-15. Dual Switch, Sample GND Connected to HV(topo3)**

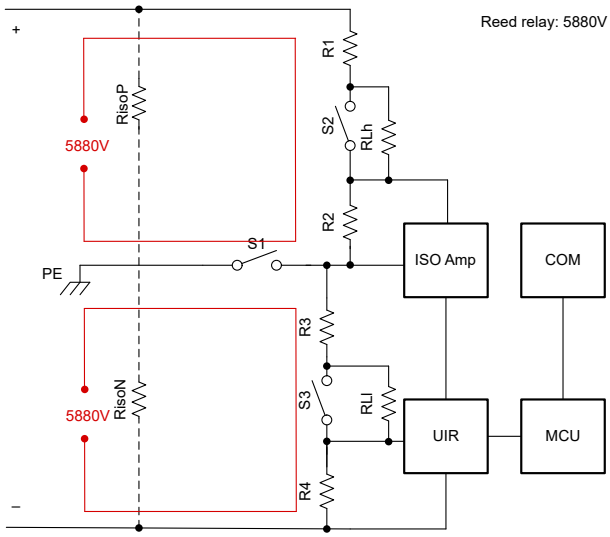


**Figure 2-16. Topo3-HV(BAT+ or BAT-) and PE①5880V**

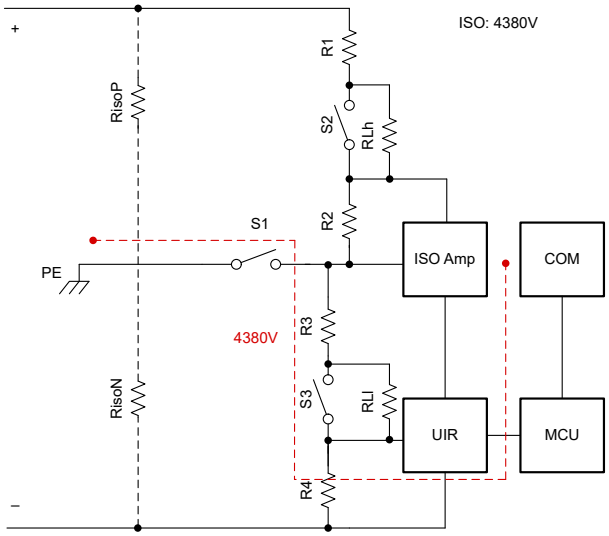


**Figure 2-17. Topo3-Communication and PE②4380V**

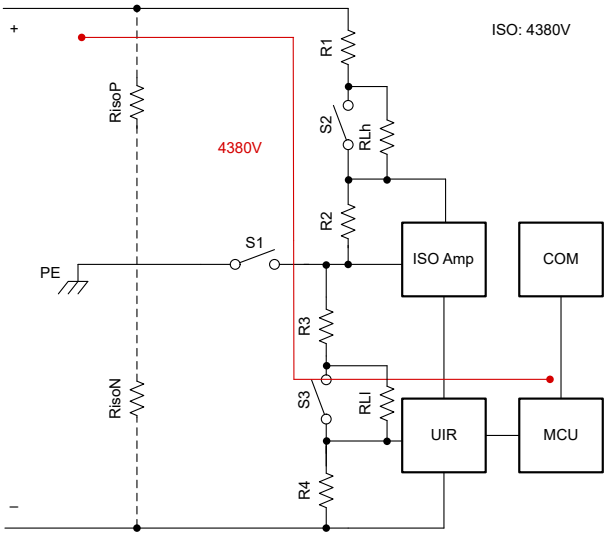


**Figure 2-18. Topo3-HV and LV(MCU)③4380V**

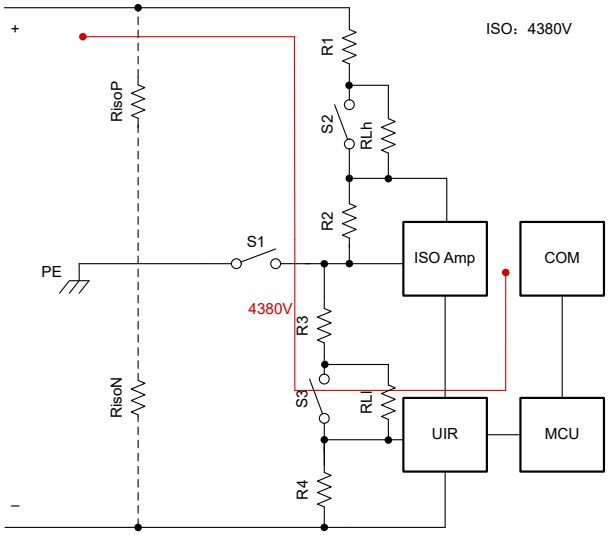


**Figure 2-19. Topo3-HV and Communication④ 4380V**

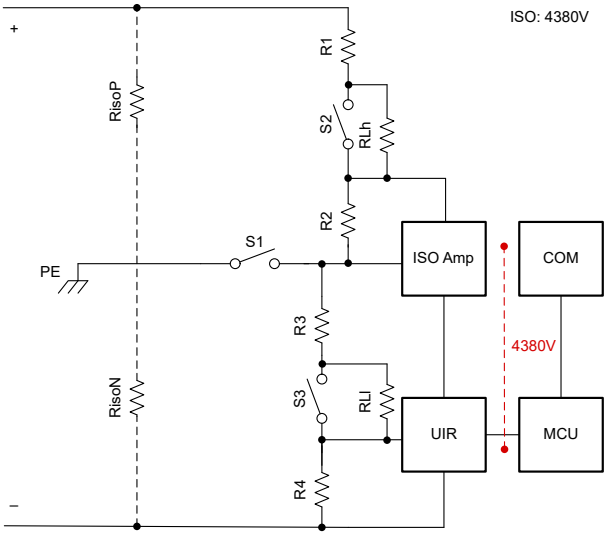


**Figure 2-20. Topo3-LV and Communication⑤4380V**

Test steps:

1. Close SW1&SW3, open SW2, get V+.
2. Close SW2 open SW1, get V-.
3. Put V+ and V- into Risop and RisoN calculate formula.

Calculate formula and worst case are the same as the Topo2 because the difference is only sampling point position and does not influence the formula.

## 2.4 AC Injection Topology

In AC injection method, the insulation resistance of the system is obtained by injecting a low voltage AC signal between the positive and negative terminals of the power battery at a certain frequency. The disadvantage is that the test signal creates ripple interference in the system, which affects the normal operation of the system. AC Injection need high accuracy AD/DA, injection capacitor, current sense. RMS detection, low pass, band pass, analyze detected signal… this can be done in dozens milliseconds. Due to the uncertainty about the accuracy, it does not need to be analyzed in this article.

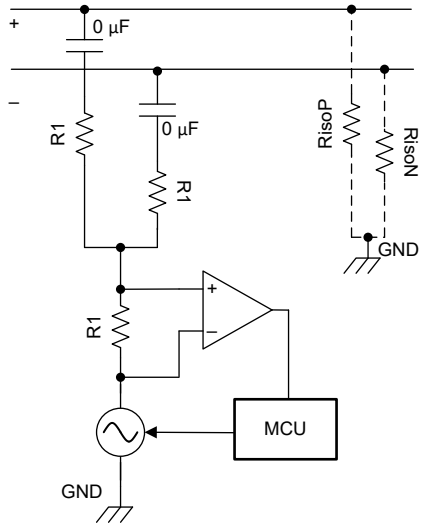


**Figure 2-21. AC Injection Insulation Test Topology**

# 3 Comparison of Designs

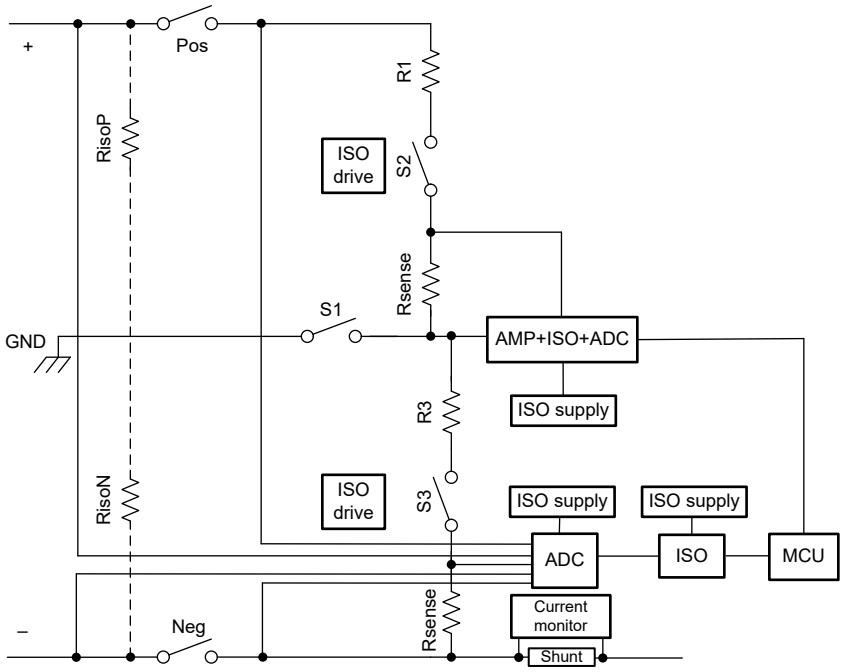


**Figure 3-1. Control Block Diagram**

The control block diagram for the topology of the dual switch, according to the requirements of the BMS for insulation detection and high voltage detection in the stored energy, is shown in the diagram above and requires both ends of the voltage drop before the sampling relay and after the relay is closed, if a differential ADC is used. Two voltage samples are required, and three voltage sampling channels are required if a single-ended ADC is used and the high-voltage negative side is considered a sampling site. Insulation monitoring and current monitoring of the shunt are also required.

This is why the system requires the use of transport, isolation, and ADCs for insulation voltage sampling, where isolation also requires additional power supply, and three ADCs for high-voltage sampling. Additional isolation and power supply are also required, as well as a single current sample.

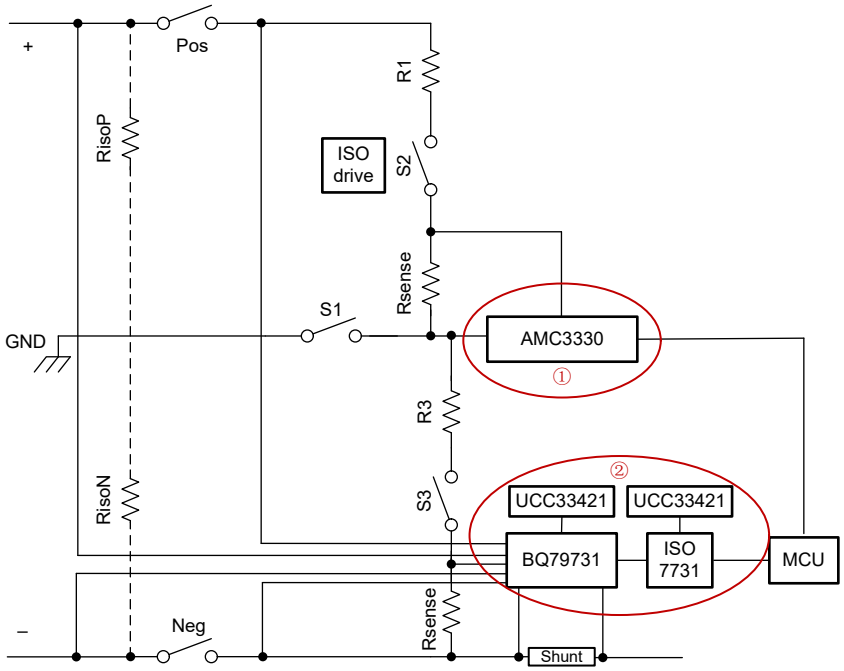


**Figure 3-2. Design1 Based on Topo 2**

Depending on the sample point arrangement, there are three options to choose from, first is the integrated AMC3330 to take on the isolation and handling functions. Sampling using the MCU's ADC, high-voltage sampling and current sampling is done by BQ79731. If the two SSRs are controlled with the ADC on the high side, the control of the SSR and the high side do not need to withstand a medium strength test voltage of 4380V from a medium strength test point of view, so no additional isolation device is required to control the SSR.

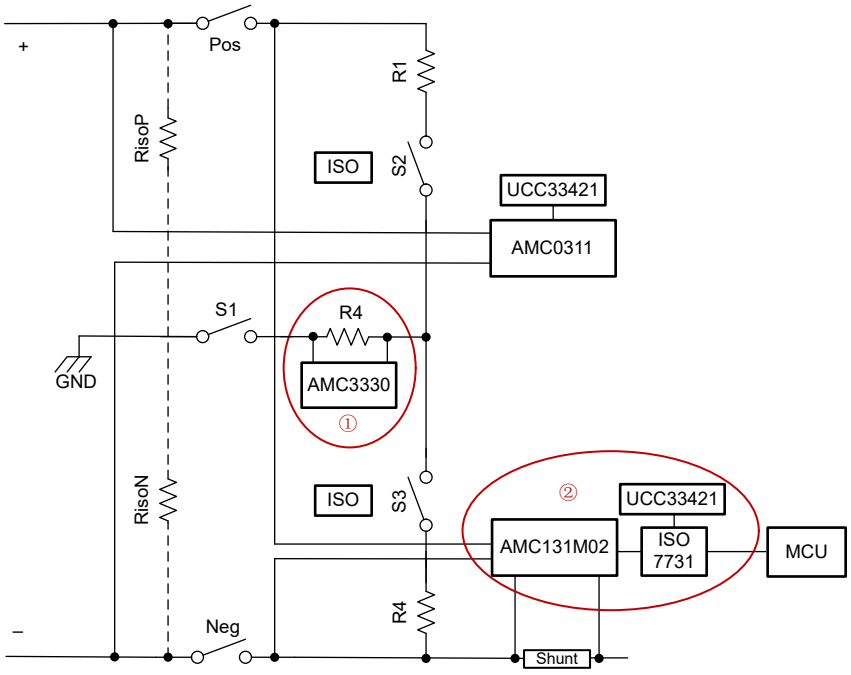


**Figure 3-3. Design2 Based on Topo 3**

Second design is to use the AMC131M03 with two isolated ADCs and one current sampling, which is less expensive but less accurate for voltage and current sampling than BQ79731, while insulation sampling requires a dual channel AMC131M02. And the control signal of the SSR needs to be isolated to meet the requirements of the media strength test.

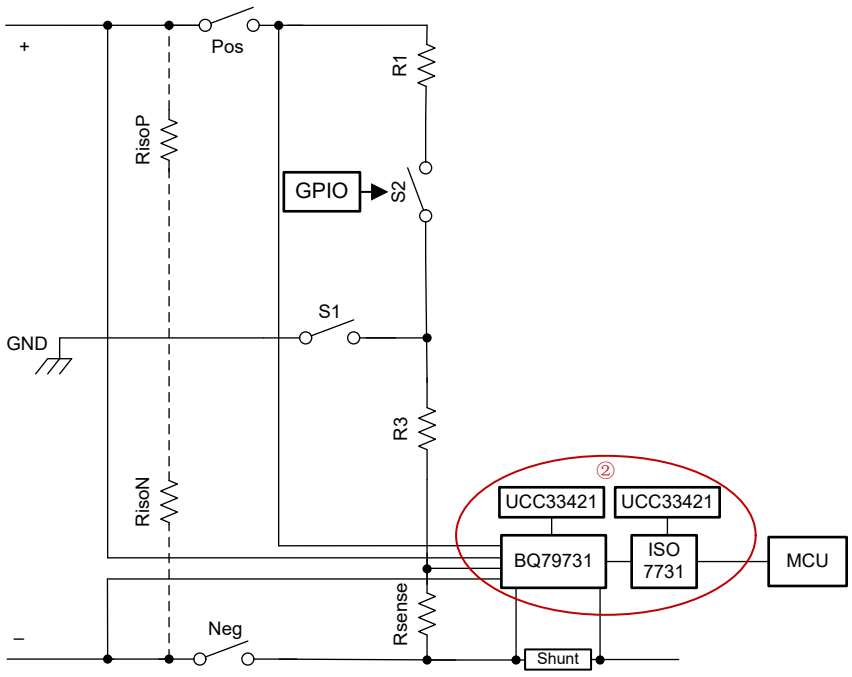


**Figure 3-4. Design3 Based on Topo 1**

The third design is a cost down design based on the topology of a single switch and a single sampling point, which uses BQ79731 to sample three voltages and the shunt current, and it can use GPIO in BQ79731 to control the switch without isolation, but it can be 5.3% lower in accuracy than the topology of the dual switch, but still meets the 20% requirements stipulated by the regulations.

## 3.1 Injection Resistance Influence on Accuracy

For the topologies of the bridge method, we change different injection resistors to calculate the final accuracy, and find that the insulation detection accuracy is proportional to the injection resistance accuracy.

**Table 3-1. Influence of Injection Resistance to Insulation Detection Accuracy**

| | Injection resistance value | | |
|---|---|---|---|
| | **4.5M** | **5.5M** | **6.5M** |
| **Injection resistance accuracy** | **Insulation resistance detection accuracy** | | |
| 0.1% | 0.31% | 0.29% | 0.30% |
| 0.2% | 0.63% | 0.58% | 0.54% |
| 0.5% | 1.59% | 1.45% | 1.36% |
| 1.0% | 3.22% | 2.93% | 2.74% |

# 4 Capacitor Influence on Sampling Time

The Y capacitance in insulation testing has a great influence on the speed of insulation testing. The mechanism of the Y capacitance affecting insulation detection is, for example, in the bridge method, that it delays the time of steady state establishment, if the unconverged voltage value is used to calculate, The resulting insulation resistance value is also inaccurate.

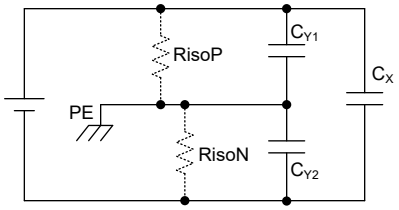


**Figure 4-1. Y Capacitor in Insulation Circuit**

## 4.1 How to Choose Y Capacitor

Although the input filtering of the high-voltage component, the theoretical value of the Y capacitance of HV+ and HV- to PE is the same, due to the tolerance of the Y capacitor itself and the difference of parasitic capacitance in parallel with it, CY1 and CY2 are often unequal, but because the bridge method is that the upper bridge arm and the lower warp arm are not opened and collected at the same time, and the larger the Y capacitance, the greater the impact on the insulation resistance measurement, so we generally calculate the external CY1 and CY2 in the static test in the following way:

Note: The total capacity between the live parts of the B-class voltage and the electric platform does not exceed 0.2J at the maximum working voltage, and the energy stored in the maximum working voltage is not more than 0.2J (GB 18384-2020 in Auto), and the maximum stored power (Q=0.5 × C × U^2) of the positive side capacitance Cy+ or negative side capacitance of the B-class voltage circuit is 0.2J.

**Note**

The coefficient of 1.27 is the proportional parameter brought about by the influence of temperature on the capacitance value.

For a 1500V energy storage system, the Y capacitor needs to be less than 230nF, and can choose 200nF in this article's evaluation.

## 4.2 Sampling Time

Suppose that the power supply Vu charges the capacitor C through the resistor R, V0 is the initial voltage value on the capacitor, Vu is the voltage value of the capacitor after it is fully charged, and Vt is the voltage value on the capacitor at any time t, then the following calculation formula can be obtained:

If the initial voltage on the capacitor is 0, the formula can be simplified to:

From the above formula, it can be seen that because the exponential value can only be infinitely close to 0, but never equal to 0, it takes an infinite amount of time for the capacitor to be fully charged.

While t = RC，Vt = 0.63Vu；while t = 2RC，Vt = 0.86Vu；while t = 3RC，Vt = 0.95Vu；

While t = 4RC，Vt = 0.98Vu；while t = 5RC，Vt = 0.99Vu；

It can be seen that when it reaches 5t, it is basically close to the final value.

Therefore, for the 1500V insulation detection system, the Y capacitor can be selected as 200nF, so it takes 4.5s to detect a voltage of 0.995u.

Based on analysis before, concluded in Table 4-1.

**Table 4-1. Comparison of Three Designs**

| Designs | Design 1 | Design 2 | Design 3 |
|---|---|---|---|
| | Device | Device | Device |
| Switch | Reed relay × 1 | Reed relay × 1 | Reed relay × 1 |
| | SSR × 2 | SSR× 2 | SSR × 1 |
| Insulation monitoring | UIR BQ79731-Q1× 1 | AMC131M02 × 1 | UIR BQ79731-Q1 |
| HV sense | - | AMC0311 × 1 | - |
| Insulation sampling | AMC3330 × 1 | AMC3330 × 1 | AMC3330 × 1 |
| ISO | ISO7731 × 1 | ISO7731 × 1 | |
| Supply | UCC33421 × 2 | UCC33421 × 2 | UCC33421 × 1 |
| **Cost summary** | US$10.21 | US$9.72 | US$7.8 |
| **Shunt** | Yes | Yes | Yes |
| **Accuracy (worst case)** | 0.82% | 0.82% | 5.9% |
| **HV supply** | Need | Need | Need |
| **Sampling time** | $=R \times 2C_Y$ | $=R \times 2C_Y$ | $=RC_Y$ |

1. The cost is almost entirely from TI devices and >1ku quantity.

Considering cost and accuracy, using double arms and putting control in high voltage can be the better choice for insulation monitoring in energy storage system.

# 5 Key Devices

## 5.1 BQ79731-Q1

The BQ79731-Q1 can be used to measure divided down high voltage nodes in a battery system. It can measure voltage across Fuse, Contactors and check isolation voltage in a battery junction box (BJB) system. The device has two integrated current sense (BQ79731-Q1) paths supporting low-side shunt resistor. Coulomb counting (BQ79731-Q1) function is available for accurate SOC calculation. There are 15 GPIOs or auxiliary inputs that can be used for HV measurements, thermistor measurements, and driving relays. There are four SW outputs that can be used to drive MOSFET switches in the measurement path. The device can function as a SPI HUB and interface with up to eight separate SPI devices or groups. Over current protection response can be achieved autonomously using HW pins for fast protection in dangerous over current events. The isolated bi-directional daisy chain ports support both capacitor and transformer based isolation. The device can also communicate with MCU over SPI and UART.

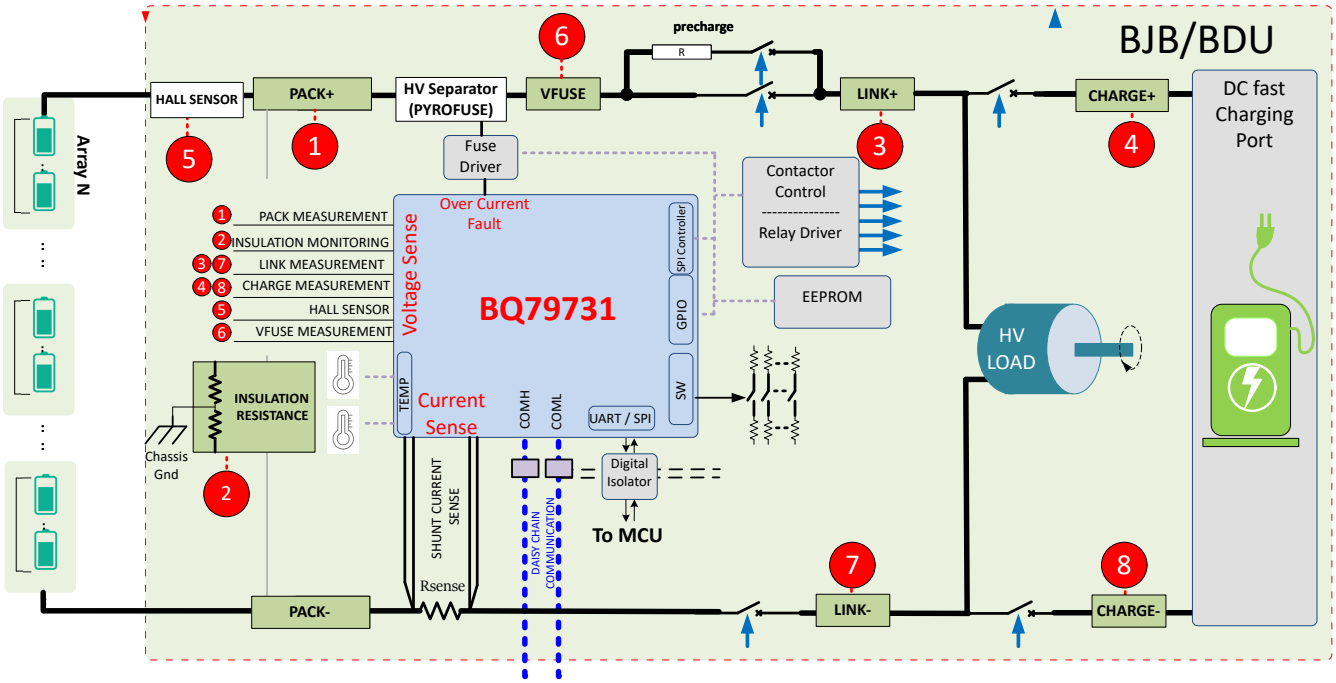


**Figure 5-1. BQ79731-Q1 Functional Block Diagram**

## 5.2 UCC33421-Q1

UCC33421-Q1 is an automotive qualified DC/DC power module with integrated transformer technology designed to provide 1.5W of isolated output power. It can support an input voltage operation range of 4.5V to 5.5V and regulate 5.0V output voltage with a selectable headroom of 5.5V. UCC33421-Q1 features a proprietary transformer architecture that achieves a 5kVRMS isolation rating, while simultaneously supporting low EMI and excellent load regulation. The UCC33421-Q1 integrates protection features for increased system robustness such as enable pin with fault reporting mechanism, short circuit protection and thermal shutdown. The UCC33421-Q1 comes in a miniaturized, low profile design SOIC (5.85mm × 7.50mm) package with 2.65mm height and > 8.2mm creepage and clearance.

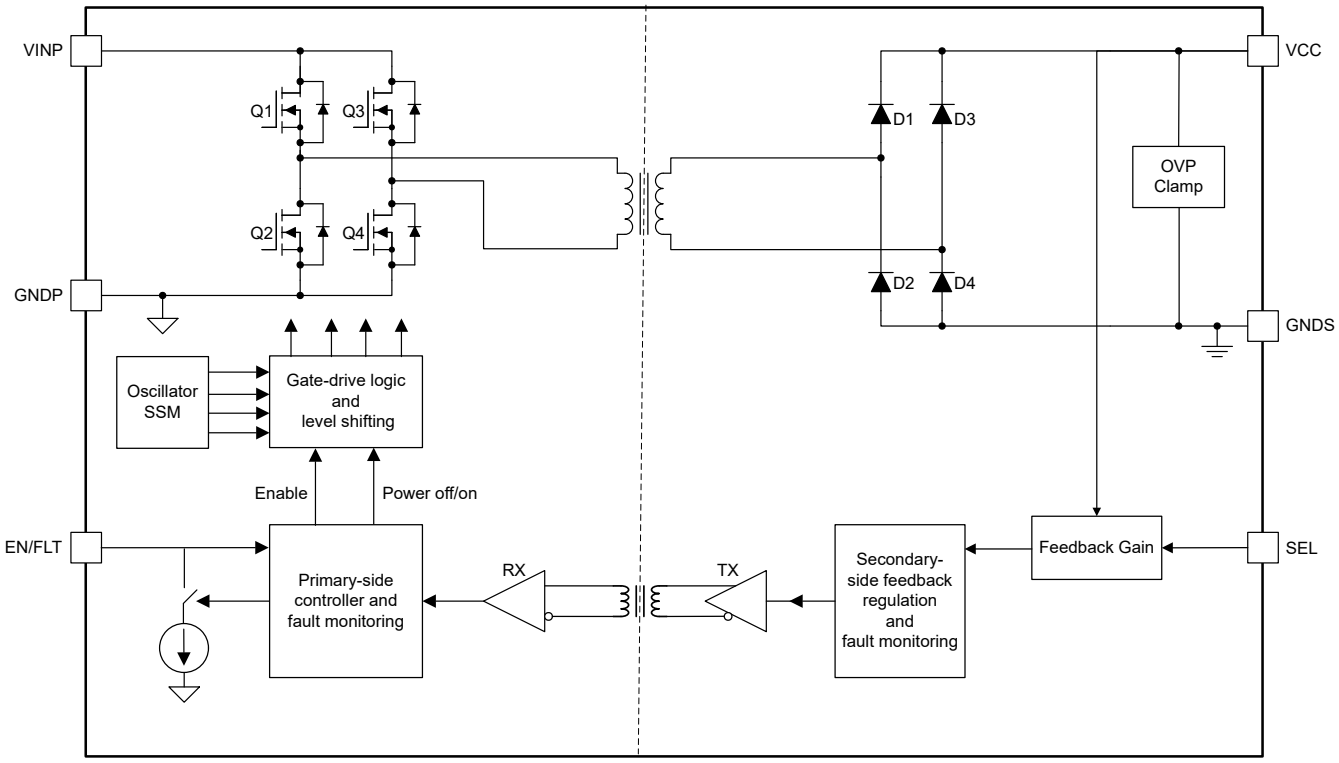


**Figure 5-2. UCC33421-Q1 Functional Block Diagram**

## 5.3 AMC131M02

The AMC131M02 is a precision, two-channel, data and power-isolated, simultaneous-sampling, 24bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC). The AMC131M02 offers wide dynamic range, low power, and energy-measurement-specific features designed for energy metering and power metrology applications. The ADC inputs can be directly interfaced to a resistor-divider network or a shunt current sensor because of the device high input impedance. The AMC131M02 features a fully integrated isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE 0884-17 and UL1577. This isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects lower voltage parts from damage, making the AMC131M02 an excellent choice for poly phase energy metering applications using shunt current sensors.

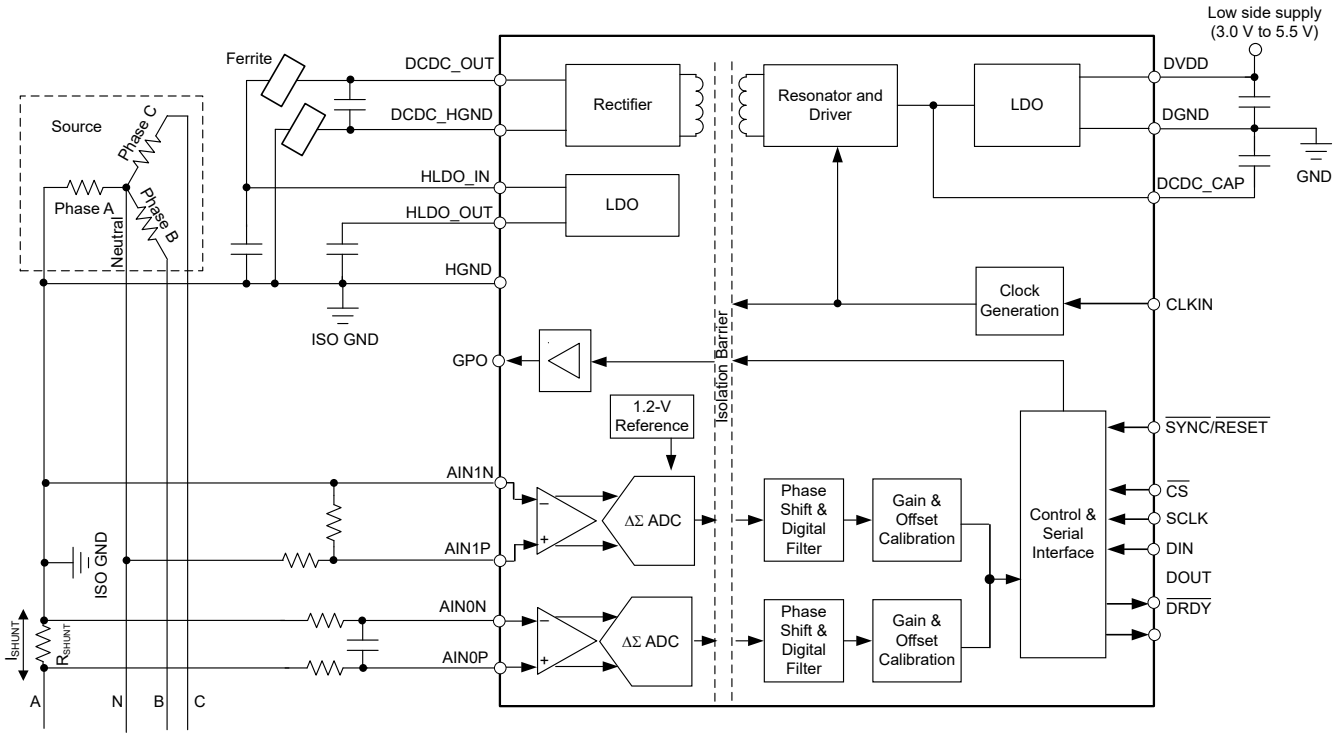


**Figure 5-3. AMC131M02 Functional Block Diagram**

## 5.4 AMC3330

The AMC3330 is a fully-differential precision isolated amplifier with high-input impedance, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3V or 5V voltage supply source from the low voltage side. The input stage of the device drives a 2nd-order, delta-sigma (ΔΣ) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bit stream. The drivers (termed TX in the Functional Block Diagram) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bit stream and clock are synchronized and processed by a 4th-order analog filter on the low-side and presented as a differential analog output.

The 1.2GΩ differential input impedance of the analog input stage supports low gain-error signal-sensing in high-voltage applications using high-impedance resistor dividers. The signal path is isolated by a double capacitive silicon-dioxide ($SiO_2$) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

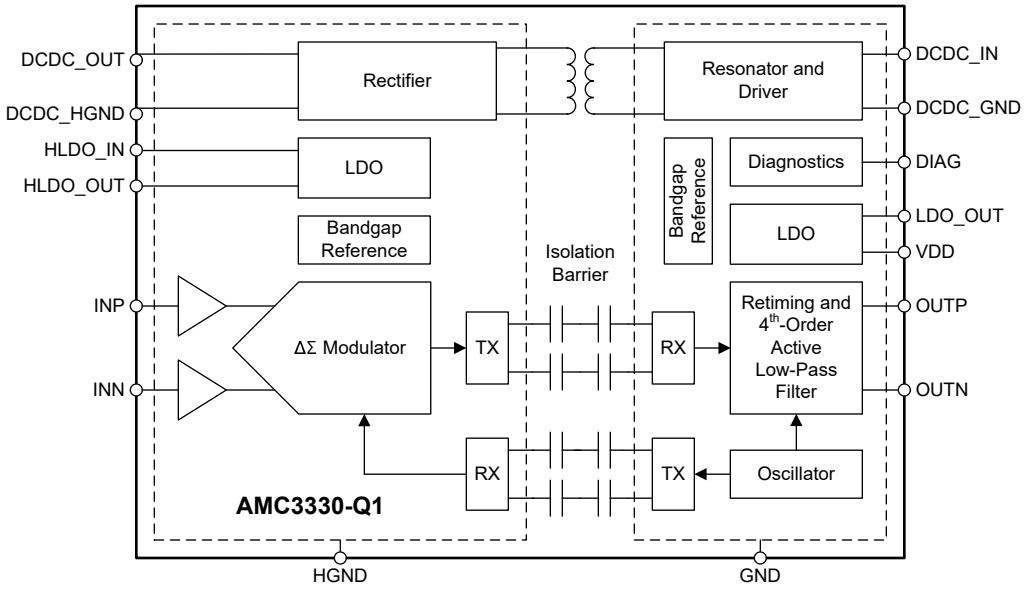


**Figure 5-4. AMC3330 Functional Block Diagram**

## 5.5 ISO773x

The ISO773x devices are high-performance, triple channel digital isolators with 5000VRMS (DW package) and 3000VRMS (DBQ package) isolation ratings per UL 1577.

This family includes devices with reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO7731B device is designed for applications that require basic insulation ratings only.

The ISO773x family of devices provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide ($SiO_2$) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption.

The ISO7730 device has all three channels in the same direction and the ISO7731 device has two forward and one reverse-direction channel. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F. See the Device Functional Modes section for further details.

Used in conjunction with isolated power supplies, this family of devices helps prevent noise currents on data buses, such as RS-485, RS-232, and CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO773x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO773x family of devices is available in 16-pin wide-SOIC and QSOP packages.

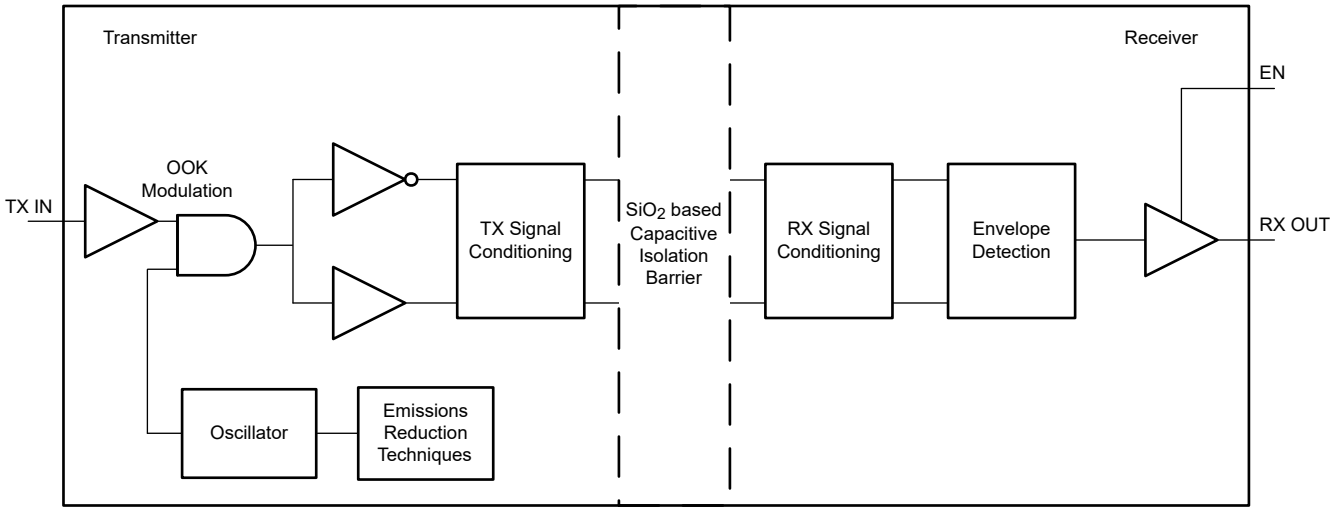


**Figure 5-5. Digital Capacitive Isolator Conceptual Block Diagram**

# 6 Topos Simulation Result and Conclusion

Build simulation models for three designs like following:

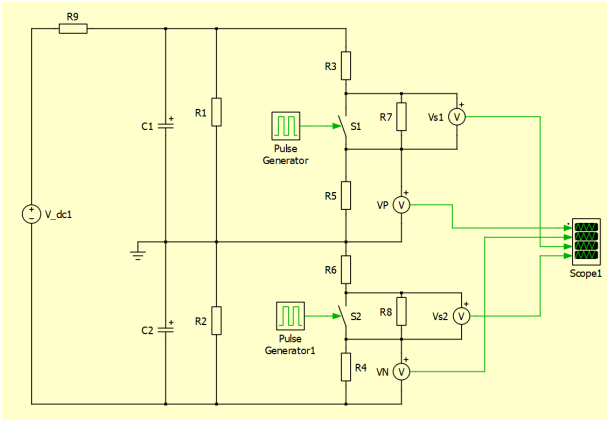


**Figure 6-1. Design 1 Simulation Model**

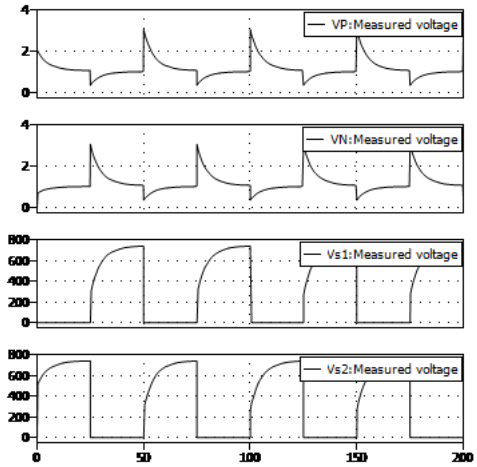


**Figure 6-2. Design 1 Result**

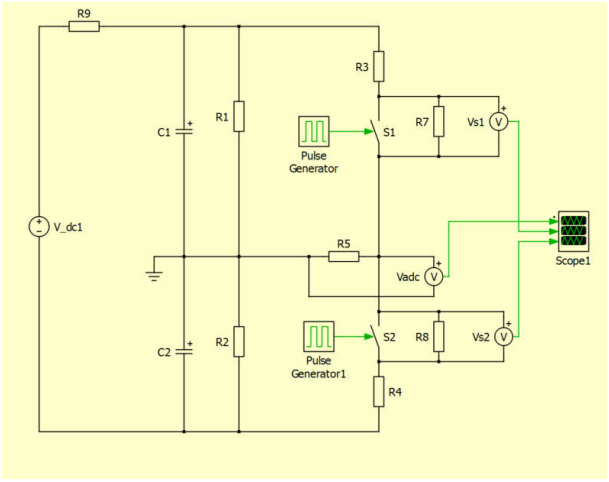


**Figure 6-3. Design 2 Simulation Model**

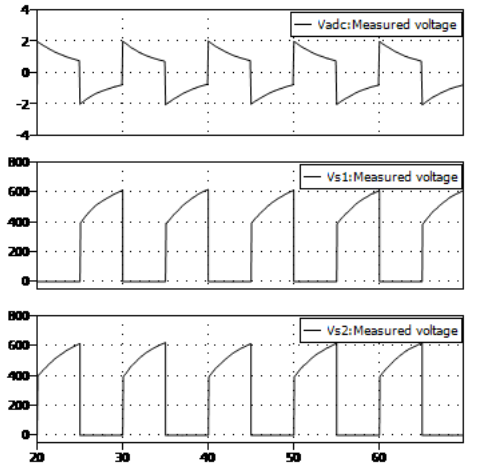


**Figure 6-4. Design 2 Result**

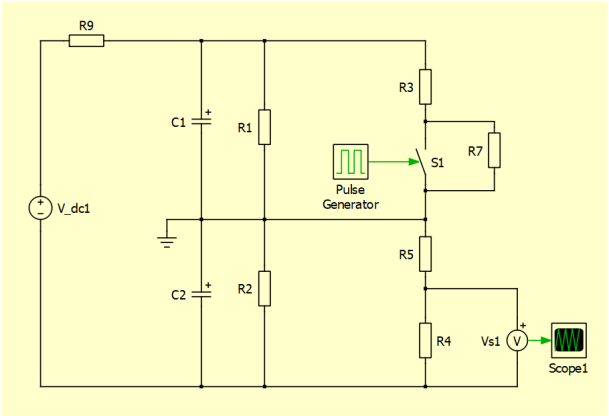


**Figure 6-5. Design 3 Simulation Model**

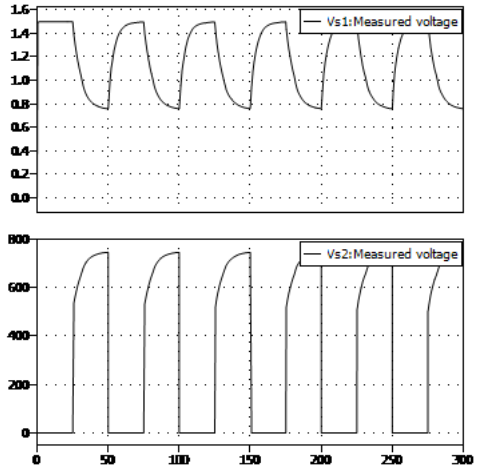


**Figure 6-6. Design 3 Result**

Take design 3 as an example, As simulation result shows, while sampling time > 5.175s, sampling voltage can be 0.995u.

**Table 6-1. Design 3 Test Result**

| RisoP | RisoN | RisoP' | RisoN' | ErrorP | ErrorN |
|---|---|---|---|---|---|
| 10000.0000 | 10000.0000 | 10065.1708 | 10028.0692 | -0.6517% | -0.2807% |
| NC | 10000.0000 | | 10027.3703 | | -0.2737% |
| 10000.0000 | NC | 10067.1862 | | -0.6719% | |
| 50.0000 | 50.0000 | 50.4129 | 50.5771 | -0.8258% | -1.1543% |
| 50.0000 | NC | 46.8382 | | 6.3236% | |
| NC | 50.0000 | | 50.7680 | | -1.5359% |

As shown in the table, worst accuracy 6.3236% happened in RisoP=50kohm, the actual test results are in agreement with the theory.

## 7 Summary

In conclusion, three designs that are mentioned in this article for insulation test are adapted to different application scenes. And the cost down design is also verified by experiment. You can consider the designs when doing insulation monitoring.

## 8 References


- Texas Instruments, *AFE for Insulation Monitoring in High-Voltage EV Charging and Solar Energy Reference Design*, design guide.
- Texas Instruments, *BQ79731-Q1 Pack Voltage Current and Isolation Resistance Monitor for HV Automotive BMS Application*, data sheet.
- Texas Instruments, *UCC33421-Q1 Ultra-Small, 1.5W , 5.0V , 5kVRMS Isolation, Automotive DC/DC Module*, data sheet.
- Texas Instruments, *AMC131M02 2-Channel, 64-kSPS, Simultaneous-Sampling, 24-Bit, Reinforced Isolated Delta-Sigma ADC With Integrated DC/DC Converter*, data sheet.
- Texas Instruments, AMC3330 Precision, ±1V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter, data sheet.
- Texas Instruments, *ISO773x High-Speed, Robust-EMC Reinforced and Basic Triple-Channel Digital Isolators*, data sheet.

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