Application Note

BQ769x2 Frequently Asked Questions

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Abstract

The BQ769x2 devices are highly accurate battery monitors and protectors which supports multi-cell battery packs in the 3- to 16- series cells for Li-ion, Li-polymer, and $LiFePO_4$. The devices integrates protection, monitoring, coulomb counter, cell balancing, regulators, and high side drivers. This document compiles the most frequently asked questions and answers about the BQ769x2 functional operation.

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1 General Operation FAQs

1.1 What are the differences between the devices in the BQ769x2 family?

Device	Cell Count	Communication Interface	CRC Enabled	REG1 LDO Default	VCell Measurement Accuracy
BQ76972	3-16	I²C	N	Disabled	+/- 3mV
BQ7697202	3-16	I²C	Y	Enabled, 3.3V	+/- 3mV
BQ7697204	3-16	SPI	Y	Enabled, 3.3V	+/- 3mV
BQ76952	3-16	I²C	N	Disabled	+/- 5mV
BQ7695201	3-16	SPI	Y	Disabled	+/- 5mV
BQ7695202	3-16	I²C	Y	Enabled, 3.3V	+/- 5mV
BQ7695203	3-16	SPI	Y	Enabled, 5V	+/- 5mV
BQ7695204	3-16	SPI	Y	Enabled, 3.3V	+/- 5mV
BQ76942	3-10	I²C	N	Disabled	+/- 5mV
BQ7694201	3-10	SPI	Y	Disabled	+/- 5mV
BQ7694202	3-10	I²C	Y	Enabled, 3.3V	+/- 5mV
BQ7694203	3-10	SPI	Y	Enabled, 5V	+/- 5mV
BQ7694204	3-10	SPI	Y	Enabled, 3.3V	+/- 5mV
BQ769142	3-14	I²C	Y	Disabled	+/- 5mV

1.2 What are the differences between the BQ769x0 and BQ769x2 device families?

The BQ769x0 (BQ76920, BQ76930, BQ76940) and BQ769x2 (BQ76942, BQ76952, BQ76972) are both highly integrated battery monitors, where the BQ769x0 is the older generation and the BQ769x2 is the newer device. Table showcases the key differences between both families.

Feature	BQ769x0	BQ769x2
Cell Count	3-15	3-16
Cell Voltage Accuracy	+/-10mV	+/- 3mV (BQ76972) +/-5mV (others)
Synced V/I for Impedance Calculations	No	Yes
Refresh Rate	250ms	63ms (Normal Mode) 31.5ms (FastADC mode)
Independent Protection	Yes	Yes
Independent Recovery	No, needs a microcontroller	Yes, can operate autonomously
High Side Driver	No, low-side driver	Yes
LDO	1 LDO, 3.3V at 20mA	Two Programmable LDOs, LDO1 and LDO2. Each can supply 45mA at 5V, 3.3V, 3V, 2.5V or 1.8V
Internal Cell Balancing	Yes, 50mA (920) 5mA (930/940)	Yes, 50mA
LDO in Low Power Mode	No	Yes, an MCU can still be powered when in SLEEP mode
Communication Protocols	I²C	SPI, I²C, HDQ
Programmable Non-Volatile Memory	No	Yes, features OTP memory

1.3 Do I need a microcontroller to control the device or can the device run autonomously?

The BQ769x2 can operate autonomously, without the need of a microcontroller. The device supports three main operating modes:

1. **Fully Autonomous:** In this mode, the device detects protection faults and autonomously disables the FETs if there is an error. After, the device monitors for the proper recovery condition and re-enables the FETs

without the need for an external processor. The device includes an OTP memory that allows the user to control the preset configurations to best meet the needs on power-up of the device.

2. **Partially Autonomous:** The device autonomously detects faults and disables the FETs. This triggers an interrupt to the host device and allow the host to keep the FETs disabled by sending commands like *0x0093 DSG_PDSG_OFF()*, *0x0094 CHG_PCHG_OFF()* or *0x0095 ALL_FETS_OFF()*. After the host decides resuming operation is safe, the host can issue the *0x0096 ALL_FETS_ON()* command to reenable all the FETs.
3. **Manual Control:** The device detects protection faults and provides an interrupt to the host processor via the ALERT pin. This information is read by the host and allows to decide whether or not to disable the FETs. To speed up the turn-off period, the CFETOFF and DFETOFF pins can be driven high by the host. Afterwards, the host processor decides when is safe to resume operation and can reenable the FETs.

1.4 What is the minimum number of cells required to operate the device and how to connect them?

The BQ769x2 device family requires at least 3 cells at all times to operate. These cells must be placed in ascending order so that so that there are cells between VC0-VC1, VC1-VC2, and VC15-VC16. The lowest cell, cell 1, must be connected at between VC0 and VC1, the next higher voltage, cell two between VC1 and VC2. This continues so that the next higher voltage is placed between the next two lowest used pins and so forth. Due to the high voltage tolerance on each of the VCx pins, the time at which each cell is connected to the device does not matter. Therefore, the device allows random cell connections on all VCx pins.

When reducing the cell count below the maximum for the device, is necessary to update the software configuration on the chip to prevent the device from reading the bypassed cells as an undervoltage fault. The user must modify the *Settings:Configuration:Vcell Mode* register to accurately reflect which cells are in use to prevent these faults.

1.5 Can the device perform gauging to calculate State of Health (SOH) and State of Charge (SOC)?

While the device does not integrate a gauging feature, does provides accurate data on voltage, current, accumulated charge, and temperature measurements which are all necessary to generate accurate SOC and SOH measurements. The data measured by the BQ769x2 is passed to a microcontroller unit (MCU) which can perform the calculations if desired. An algorithm can be implemented to perform gauging without the need for any additional devices.

A gauging algorithm with a high level of accuracy is quite complex and often requires a large amount of software development. Therefore, a stack-level gauge like the BQ34Z100-G1 can be used in unison to provide SOC and SOH. This reference design shows how the BQ347Z100-G1 can be interfaced with battery monitors.

1.6 How does unused pins needs to be connected?

Table 1-1. How Unused Pins Need to be Connected

Pin Name	Connection	Additional Actions
VC0-VC16	Unused VC0-VC16 pins must be shorted together	The device must be updated in *Settings: Configuration:Vcellmode* to reflect which pins are not used.
RST_SHUT, REGIN, SRP and SRN	Tied to pin 17, VSS	If REGIN is unused, make sure to disable the LDOs on the device.
TS1, TS3, ALERT, HDQ, CFETOFF, DFETOFF, DCHG, DDSG, REG1, REG2, and FUSE	Left floating or tied to VSS	Is necessary to go to Setting:Configuration: [pin[1:0]] and set equal to 0x0.
PDSG, PCHG, DSG, and CHG	Left floating	-
TS2	Left floating or tied to VSS	Only tie the device to VSS when the device is not entering SHUTDOWN
BREG	1. If REGIN is used, connect to REGIN 2. If REGIN is not used, tie to VSS	-

Table 1-1. How Unused Pins Need to be Connected (continued)

Pin Name	Connection	Additional Actions
LD	1. If DSG is not used, connect to PACK+ through a series resistor 2. LD can be connected to VSS	-
CP1	Connect to the BAT pin	Make sure to disable the charge pump when CP1 is unused as the device consumes an additional 200uA if left operating.

1.7 What does support random cell attachment means?

What random cell attachment means is that when assembling the battery pack and connecting cells to the chip, CELL10 can be connected to VC10 and VC9 first, then CELL4 to VC4 and VC3. The timing sequence in which cells are attached to the device can be in any order desired. This is only possible due to the high voltage tolerance on pins VC1-VC16.

Random cell attachment does not mean that CELL1 can be connected at VC0-VC1 and CELL6 can be connected at VC1-VC2. Cells must be attached sequentially and in ascending order.

1.8 How do I RESET the BQ769x2 device?

The BQ76952 has two different types of RESET: full and partial.

- Full RESETs resets all the digital logic as well as clear all registers not programmed using OTP. These can be achieved by either using either the *0x0012 RESET()* subcommand or exiting shutdown.
- Partial RESETs resets most digital logic including communications, but all register information is preserved. A partial RESET occurs when the RST_SHUT pin is held high for less than one second before going back low. If the pin is held high longer than one second, the device then enters shut down.

1.9 How does the BQ769x2 recover from a fault?

The device can recover from a fault in two ways.

1. **Autonomously:** This is enabled by setting the *Settings:Manufacturing:Mfg Status Init[FET_EN]* configuration bit. Once enabled, the device turned FETs off once a fault is triggered. The device routinely monitor the flags until the flag no longer triggered. After, the FETs are reenabled.
2. **Manually:** When a fault occurs, the ALERT pin is configured to go high, providing an interrupt to the host MCU. To shut off the FETs, the MCU can use commands like *0x0095 ALL_FETS_OFF()*. However, if speed is necessary, the chip has CFETOFF and DFETOFF pins that act as an analog input to disable the FETs. Simply asserting the signal is enough to disable the FETs. When the MCU decides is safe to resume operation, The device can then either send an *0x0096 ALL_FETS_ON()* command or dessert CFETOFF/ DFETOFF depending on which method was used to disable the FETs.

1.10 Does the BQ769x2 support open wire detection?

The device supports detection of broken connections between the chip and the battery. An open-wire event can occur by a physically broken connection between cells, a contaminated contact, wrong resistor values, or solder defect. In case of an open-wire event, the device can provide incorrect voltage measurements for that cell. During open-wire detection, a small amount of current flows from each cell to ground. If a cell is disconnected, the voltage at the measurement node then quickly drop triggering an undervoltage fault. Open-wire detection can be enabled in the *Settings:Cell Open-Wire:Check Time* register and set periodically so that the average current drawn is between 0.65nA to 165nA.

2 Control FETs FAQs

2.1 What are the tradeoffs of High side vs Low side gate driving?

Low side gate driving is often easier to implement than high side driving. Since the source of the FET is connected to GND, all that is needed to turn the FET on is about 10V if the FET is an N-channel. However, since the source is connected to GND, when the FET is turned off, the battery becomes an isolated GND so the reference for communication is lost. While this can be overcome with isolating communication, this is often expensive and consumes a large amount of energy.

High side driving, while harder to implement, maintains that the GND reference so that the same is never lost between the battery and the system and allows easy communication and therefore better performance. High side gate driving is simple with a P-channel FET since the gate needs to be lowered below the pack voltage to turn on. However, P-type FETs have a naturally higher $R_{ds,on}$ than N-type FETs, so P-type FETs are not often used for these applications. N-type FETs do offer a lower $R_{ds,on}$ for high side driving. The catch is that the gate voltage must be brought higher than the battery pack voltage. This requires a power supply higher than the pack voltage as well as level shifters for control. Implementing this often requires additional circuitry which raises costs. However, the BQ769x2 family features a built-in charge pump and high side driver which allows high side driving with no additional cost or complexity to the user.

2.2 Can the BQ769x2 be used for low-side FET driving?

Since the BQ769x2 is designed with an integrated high-side driver, an external driver is needed to be used to implement low-side. The drivers can be controlled by the DCHG and DDSG pins. More information on implementing this is included in the Application Note, *Using Low-Side FETs with the BQ769x2 battery Monitor Family*.

2.3 Is the CP1 capacitor necessary for low-side switching?

No, a capacitor at CP1 is not needed when using low-side switching. The charge pump (CP1) pin is used to boost voltage higher than BAT, but if the higher voltage is not necessary due to using low side switching, the pin does not need a capacitor.

2.4 How long does the BQ769x2 take to turn on the FETs on power up?

The device takes up to 250ms for the device to initialize from SHUTDOWN. Afterwards, the MOSFETs are able to be turned on. In order to turn on manually, users must send a command like *ALL_FETS_ON()* or deassert CFETOFF and DFETOFF. These updates are evaluated every 250ms to determine if one has occurred. If so, the FETs then are enabled.

To determine the state of the FETs, the devicve provides two alternatives: An MCU can poll the device to figure out if the device is initialized by I^2C or SPI or the user can set an interrupt with the ALERT pin which notify the MCU that the device is up and running.

2.5 What are the typical voltages for the Charge (CHG) and Discharge (DSG) pins?

For high side applications, the CHG and DSG pins voltages are the voltage of the attached battery pack plus the voltage provided by the charge pump. The charge pump can either provide 5.5V or 11V to drive the gates of the CHG and DSG pins. The desired voltage can be set by modifying the configuration bit at *Settings:FET:Chg Pump Control[LVEN]*. The 5.5V setting allows a lower power dissipation while driven, but the 11V reduces the on-resistance of the FET while operating.

2.6 What are the voltage ranges of the Precharge (PCHG) and Predischarge (PDSG) pins?

There are two scenarios for the voltage ranges, depending on whether LD or BAT are greater than 8.4V.

1. **LD or BAT >= 8.4V:** When either PCHG or PDSG are enabled, PCHG or PDSG pull to a voltage 8.4V below the higher voltage of BAT and LD. If the BAT pin was 38.4V and the LD pin was 28V, the PCHG pin is held to 30V.
2. **LD and BAT < 8.4V:** Neither PCHG nor PDSG can be pulled below VSS, therefore the resulting voltage between VPACK and VPCHG ranges from VPACK to VPACK-0.5V. Referenced to ground, this means that the voltage on the PCHG pin is between 0 and 0.5V. The same applies to PDSG.

2.7 How can I achieve faster gate turn-offs for DSG?

There are two general methods for reducing gate turn-off times.

The first is shown in Figure 2-1 and offers a low cost design to speed up the turn-off by using a diode (D4) to provide a lower resistance path for the gate of the FET to discharge the stored charge compared to the turn on path. By varying the resistance, the time to turn-off can be increased or decreased as desired.

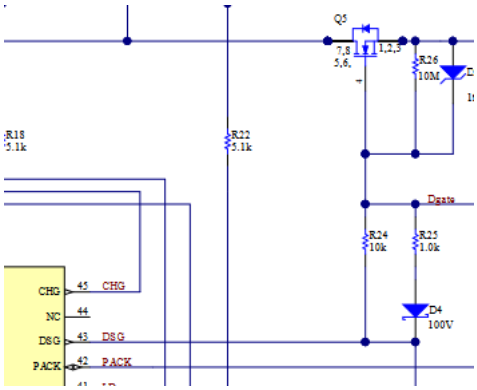

Figure 2-1. First Speed Up Configuration Utilizing a Single Diode (D4)

The second is shown in Figure 2-2. This circuit uses the ability to drive the PMOS low quicker to provide an alternate path for the charge of the FETs to drain from the gate and into PACK+. This configuration, while more expensive, is an excellent choice for situations where multiple FETs are in parallel due to the ability to get a lower resistance. If the user is using only one or two FETs, option one is more cost efficient.

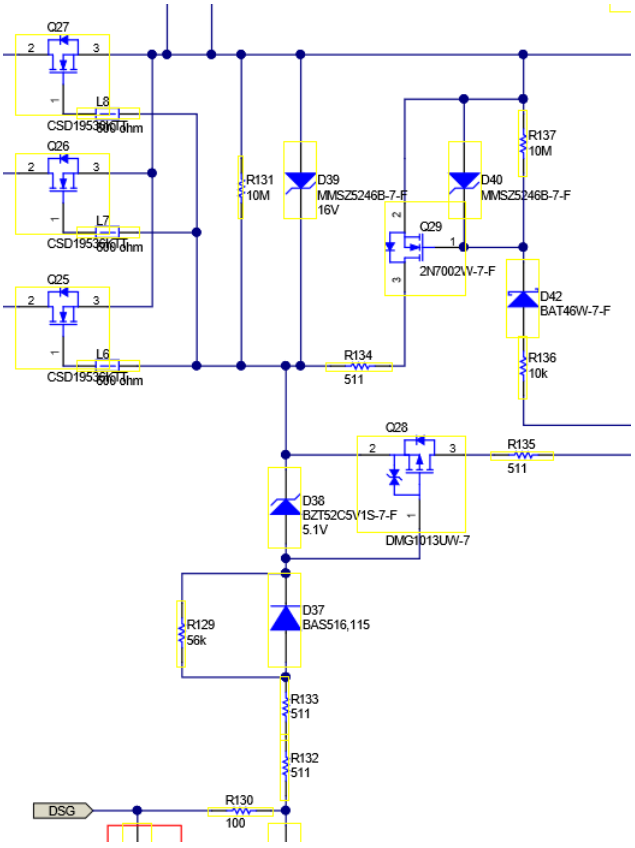

Figure 2-2. The Second Configuration For Multi-FET Applications using a PMOS and Diode (D37 and Q28)

2.8 Why are the FETs turning OFF while data memory registers are being configured in CONFIG_UPDATE mode?

For safety reasons, the BQ769x2 does not support modifications to the configuration registers while the FETs are enabled. Entering CONFIG_ACCESS mode turns off the FETs to protect the device.

2.9 Is there a way to manually control PCHG and PDSG?

While operating with protections enabled, is not possible to manually control PCHG and PDSG. This is done autonomously by the chip. The only possible way to do this is by using TEST_MODE (FET_EN = 0), but this disables all automatic protections in the device so is therefore not recommended for systems in operation. By writing to registers, the PCHG and PDSG can be configured to turn off after a set amount of time or stay on until set voltage is reached while still having protections enabled. For discharge, the registers are *Settings:FET:Predischarge Timeout* and *Settings:FET:Predischarge Stop Delta*. For PCHG, the register is *Settings:FET:Precharge Stop Voltage*.

2.10 Can I use an NFET with the PDSG pin?

No, the PDSG driver operates by pulling the pin voltage slightly lower to enable the PFET. If a N-type FET is used, the PDSG FET is unable to turn-on.

2.11 What states are PDSG and PCHG when disabled?

PREDISCHARGE (PDSG) and PRECHARGE (PCHG) use tri-state drivers for the output so when PDSG and PCHG are disabled, these are in a high impedance state to minimize leakage current.

2.12 How do I disable the Discharge FET (DFET) and Charge FET (CFET)?

There are three ways to turn off the DFET and CFET. These can be turned off using the subcommands *0x0095 ALL_FETS_OFF()* and *0x0093 DSG_PDSG_OFF/0x0094 CHG_PCHG_OFF*. The former shutoff both the DFET and CFET while the latter only disable the respective DFET and CFET. The final way is to configure a multipurpose pin to the DFETOFF/CFETOFF mode. When that pin is asserted from an external source, the corresponding gate is then disabled. Whether the pin is active-high or active-low can be configured in the device settings under *Settings:Configuration:DFETOFF Pin Config[OPT5]*.

2.13 Can the BQ769x2 idle with PDSG ON during SLEEP mode?

Yes, this can be achieved by setting your device to PREDISCHARGE mode with the DSG FET in source follower mode. Enabling PREDSICHARGE mode allows the PDSG FET to turn on prior to the DSG FET and limit the inrush current. This is enabled by setting *Settings:FET:FET Options[PDSG_EN]* high. From here, the device turns on the PDSG FET before DSG. By making *Settings:FET:Predischarge Timeout* equal 0, and *Settings:FET:Predischarge Stop Delta* to be your desired voltage difference (or set to 0), the device remains with the PDSG FET until the threshold voltage difference is met.

Likewise, you must make sure to enable source-follower mode for the DSG FET. This is achieved by setting the *Settings:FET:Chg Pump Control[SFMODE_SLEEP]* bit. Source-follower allows the DSG FET remain off while in SLEEP mode until a discharge current is detected. When combined with PDSG mode, this allows the PDSG FET to turn on prior to DSG FET and limit inrush current when a load is first attached.

3 Coulomb Counter (CC) and ADCs FAQs

3.1 What resolution does the ADC provide for voltage measurement?

All ADC measurements for cell voltages are multiplexed into a single ADC. From there, a voltage with units of 1mV and 16-bit resolution is calculated using the configured trim and calibrations. The raw 24-bit output is also available to be read if so desired by using 32-bit subcommands, where the high 8 bits are sign extended from the 24 bits of data.

3.2 How fast does the BQ769x2 ADC sample?

The ADC can be configured to run in **NORMAL** or **FASTADC** modes by going to *Settings:Configuration:Power Config:FASTADC*. While in normal loop, each measurement takes 3ms, so a typical measurement loop with 21 slots takes 63ms to complete. When FASTADC is set, the sampling time is cut in half to 1.5ms per measurement, making the total loop time down to 31.5ms.

3.3 How does the ADC operates while on SLEEP mode?

While operating in SLEEP mode, the device samples voltage measurements in periodic bursts. When the bursts are not happening, the LFO oscillator is set at 32kHz to save energy. However, when the burst of measurements occur, the device switches that LFO back to 262kHz to maintain the time needed to complete each measurement is still 3ms.

3.4 Does the coulomb counter provide a SoC and SoH measurement?

While the Bq769x2 does not feature a built-in tool for calculating SoC and SoH, the coulomb counter provides high resolution measurements the current flowing from the cells that is in synchronization with the voltage measurements. This gives the user all the necessary data to calculate SoC and SoH for the battery packs.

3.5 Can the coulomb counter be used to measure instantaneous current?

Since the CC is an integrating converter, the CC is unable to measure the instantaneous. Rather, the CC provides the average current over a 250ms period while operating in NORMAL mode, polling every 3ms. This can be sped up to 1.5ms by using FASTADC at a loss of resolution.

3.6 What is the resolution of the coulomb counter?

The device contains three filters for the coulomb counter: CC1, CC2, and CC3. The first two can be viewed using the *0x0075 DAStatus5()* subcommand, while CC3 can be viewed with the *0x0076 DAStatus6()* subcommand.

1. **CC1** is used for charge integration and produces a 16-bit output every 250ms.
2. **CC2** used for current measurement, and produces a 24-bit result, sign extending the last 8 bits to be 32 bits. This is outputted every 3ms in NOMRAL mode and every 1.5ms when the *Settings:Configuration:Power Config[FASTADC]* bit is set.
3. **CC3** is the average of a programmable number of CC2 current samples (up to 255) which produces a 64-bit, fixed point output where the bottom 32-bits are the fractional portion and the upper 32-bits are the whole number portion.

3.7 Is the coulomb counter used for overcurrent detection?

Due to the CC integrating voltages to determine current by an ADC, the CC is only used for trigger the OCD3 protection due to the slow speed. This is the slowest detector for overcurrent with the delay ranging from 1 to 255 sec in units of 1 sec. The time delay can be configured in the Protections:OCD3:Delay register.

The remaining overcurrent protections rely on comparators to generate a fast response in the case of an overcurrent or short circuit condition. To use OCD3, set the *Settings:Protection:Enabled Protections C:[OCD3]* bit.

3.8 What is the difference between OCD1, OCD2, OCD3, and SCD?

While all four are used to detect an excess current, OCD1 (Overcurrent in Discharge 1), OCD2 (Overcurrent in Discharge 2), and SCD (Short Circuit in Discharge) use comparators to measure differential voltage across the coulomb counter (SRN and SRP pins). From there, a fault is generated whenever the comparator detects

a value . Meanwhile, OCD3 (Overcurrent in Discharge 3) uses the digital value of the coulomb counter ADC to determine whether a fault occurs instead of a comparator, which is the slowest method for detecting overcurrent. The delay times to disable the FETS for each method varies as shown below:

1. SCD: Programmable delay time ranging from 15us to 465us.
2. OCD1 and OCD2: Programmable delay time ranging from 3.3ms to 419.1ms. OCD1 is initially programmed to a smaller delay time than OCD2
3. OCD3: Programmable delay time ranging from 1 second to 255 seconds.

The image below shows how the cutoff varies with time.

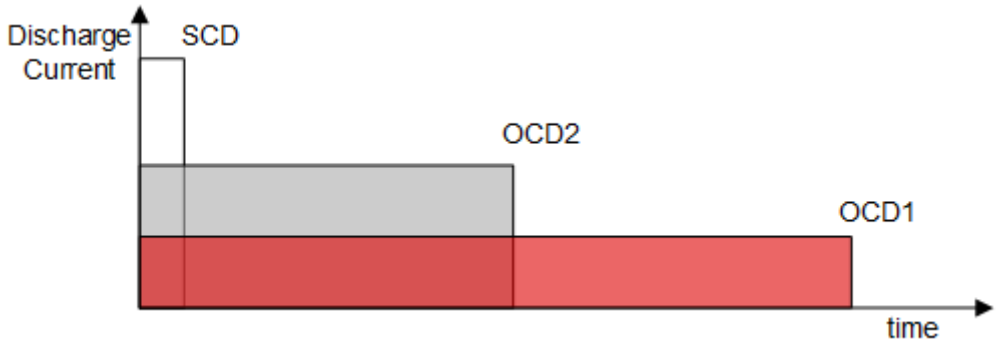

Figure 3-1. Discharge Current Versus Time for Overcurrent Protection (Not To Scale)

3.9 Why is the accumulated charge measurement seems to be producing an incorrect value?

After resetting the device using the RST_SHUT pin, one must use the *RESET_PASSQ()* command to reinitialize the Coulomb Counter. This maintains the proper values when going into operation.

3.10 Why is the voltage of CELL1 seems to be measuring incorrectly?

The most common reason for an error in the voltage measurement of CELL1 is due to a voltage difference between VC0 and VSS. Per the data sheet, the recommended voltage of VC0 must be between -0.2V and 0.5V of VSS. Failure to do this can result in measurements being off by 1-3V per cell. To overcome this issue, is best to have a net-tie or 0 ohm resistor between VC0 and VSS on the same board as the BQ769x2 close to the VCO pin.

On rare occasions in SLEEP mode, an invaldid Cell 1 Voltage() reading has been observed to occur. This is handled by validating a measurement as legitimate by comparing to previous measurements. More information on this is covered in *section 10.1.3 of the data sheet*.

4 Communication Protocols and Programming FAQs

4.1 What communication protocols does the BQ769x2 support?

The BQ769x2 supports SPI up to 2MHz, I²C at both standard (100KHz) and fast-mode (400KHz), and single wire HDQ protocols.

4.2 Does the BQ769x2 support cyclic redundancy checking (CRC)?

The device allows CRC checking with both SPI and I²C communication protocols. These are enabled in *Settings:Configuration:Comm Type*. The CRC check is sent after every byte of data is transmitted to verify the data arrived correctly. The BQ769x2 family uses the polynomial $x^8 + x^2 + x + 1$ for calculating the check.

When using single-byte write transactions, the CRC calculates the value based on the responder address, register address, and data. When using block write, the CRC for the first byte is calculated based on the responder address, register address, and data. Any subsequent bytes is calculated only on the data bytes.

4.3 Does the I²C lines require pull-up resistors to operate?

Yes, if I²C is going to be used, is necessary to have two pull-up resistors for SDA and SCL as the device does not have internal pullup resistors. The recommended values are between 4.7k and 10k ohm resistors.

4.4 Does the BQ769x2 support clock stretching?

For the I²C protocol, clock stretching is available for use on both direct commands and subcommands. However, clock stretching is not available when using SPI protocols.

4.5 Does the BQ769x2 allow block writes and reads?

The BQ76952 allows block read and writes on I²C communications, but not on SPI communications. SPI can go up to 2MHz for the communication frequency while I²C is optimized for a maximum frequency of 400kHz.

4.6 Does the BQ769x2 require isolation to communicate?

Since the device utilizes an internal high-side switching, the GND of the battery pack is always connected to the protector, regardless of whether the FETs are off. This means that isolating the communication lines are not required. If the user decides to use low side switching instead, the device needs isolation for communication.

4.7 When shall I use OTP programming?

In most situations, the microcontroller can set the desired parameters after power-up for typical operations without needed OTP programming. However, if a different default value is needed on power-up, the device has an OTP memory that the customer's production line can change these default values. There are three common use cases:

1. Configuring REG1/2 LDOs during Startup: This is most often used when REG1 needs to power the microcontroller of the system. The BQ7695202 have REG1 defaulting to 3.3V without the user having to modify the OTP memory.
2. Changing Communication Modes: If the user decides to change communication modes, this can be adjusted in the OTP memory. The table in Section 1 highlights the different preconfigurations that are available for the BQ769x2 family.
3. Using the BQ769x2 in Stand-Alone Mode: If the device is not being used in conjunction with a microcontroller, all modifications must be made in the OTP memory to not be wiped when the device enters SHUTDOWN mode. Therefore OTP programming allows permanent modifications to allow the device to operate alone.

4.8 How does the BQ769x2 OTP memory work?

The BQ769x2 includes a one-time programmable (OTP) memory for customers to setup device operation on the production line. The OTP memory consists of two images of the Data Memory configuration settings alongside the initial preconfigured settings. The two frames are initially all-zeroes. On power-up, the device XOR these two frames together and then XOR with the default value for each setting. The result of this XOR operation is what is initialized into the device's settings after power-up. Until something is programmed to the frame, the XOR

of the two frames produces a 0 leaving the initial settings unaffected. The two images allow to change a value with the first image, and then change back to default with the second image. For more information on the OTP programming and limitations, refers to the Technical Reference Manual.

4.9 How many times can the BQ769x2 OTP memory be modified?

OTP memory has two full images of the data memory configuration settings which are both initialized to 0. Each bit on each frame can be modified only once. Since the device XORs the two frames, writing to one frame turns the modified bit high. By setting the corresponding bit in the second frame high, the two high bits then cancel out in the XOR, returning the change to default.

However, the number of changes to the OTP is limited. There are 8 signature values, where one is used each time a change to the OTP is made. Therefore, the total number of partial writes that can be made to the OTP is 8 times. Each write allows the user to change registers as needed, with the limitation that the bits the user writes to have not been modified twice. For more information on the OTP programming and limitations, refers to the Technical Reference Manual.

4.10 What hardware is necessary to program the OTP memory?

To program the OTP memory, 10-12V must be applied to the BAT and VC16 pins. Cells must not be connected to the device when programming OTP memory.

4.11 How can the host reset the ALERT pin interrupt?

The alert pin can be configured to interrupt to the host microntroller when a fault is active. When the ALERT pin is used as an alarm signal (*Settings:Configuration:ALERT Pin Config[PIN_FXN1:0]* = 0b10), the flag raised when an alert is triggered. At this point, the alert can only be lowered by a command sent by an MCU or external device. The required command to clear is *0x62 Alarm Status()*, where a bit set to '1' means to clear the corresponding flag and a bit set to '0' leaves the flag unmodified.

4.12 Why is my subcommand returning incorrect data?

A common root cause of incorrect readings after a subcommand is not waiting enough time for the device to complete the operation. Most subcommands take a typical time of 500us to execute. Some alternatives to make sure the device has completed the operation and data is available are:

- **Polling:** Host controller can poll the subcommand address (0x3E and 0x3F) to make sure the previously writen subcommand value is readback. This maintains that was propertly executed and the data is now available on read transfer buffer (0x40). *Section 3.1 Direct Commands and Subcommands* of the TRM provides a detail pseudocode for polling subcommands.
- **Wait:** Given enough time for the command or command-only subcommand to execute is the best recommendation, this maintains that execution is completed and saves processor power by setting the host on idle state instead of polling the registers. A recommended value of 2ms is suggested to maintain that enough margin is given for all command operations.

For reference, *Table 9-2 Command/Subcommand Operation Time* of the Technical Reference Manual describes the typical execution times to complete command and subcommand operations.

5 Calibration and Temperature Sensing FAQs

5.1 Does the BQ769x2 come calibrated or do I need to calibrate externally?

The BQ769x2 device is initially calibrated at the factory to perform within the limits of the data sheet. In addition, the user can also do a calibration to compensate for board specific conditions, such as parasitics, and further optimized the accuracy of the device. Typical parameters to be calibrated and configured at customer side are thermistors models coeficients and ADC measurements gain and offsets factors.

5.2 Can custom calibrations be stored onto the BQ769x2?

Yes, the device allows custom calibrations for a wide variety of measurements including gain and offset for cell voltages, pack voltages, current gain, and temperature offsets. These can either be programmed by a microcontroller once the device is powered up, or burned into the device using OTP programming so that is configured during power-up.

5.3 How do I modify RAM registers to update calibrations?

RAM is modified in the following steps:

1. Enter FULL ACCESS mode
2. Verify FULL ACCESS mode by reading *0x12 Battery Status[SEC1, SEC0]* to observe 0x01
3. Enter Config Update Mode by sending the *0x0090 ENTER_CFG_UPDATE()* subcommand
4. Modify RAM registers as desired
5. Exit Config Update by sending subcommand 0x0092
6. Read modified registers to confirm changes

5.4 Can each cell measurement have a custom (offset/gain) calibration factor?

The device supports a custom gain for all 16 cells as well as an overall PACK gain. These can be configured in *Calibration:Voltage:Cell x Gain*. In addition, the cells also have a cell offset value that can be modified in *Settings:Calibration:Vcell Offset*.

5.5 How to configure a multipurpose pin to work as a thermistor ?

The BQ769x2 devices support up to 9 external thermistors using the multipurpose pins. The available pins are TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG. When implementing an external thermistor, is generally recommended to place a capacitor in parallel with the thermistor. There are two possible configurations for pullup resistors to use, 18kΩ and 180kΩ. These can be set by going to *Setting:Configuration:[available pin]*.

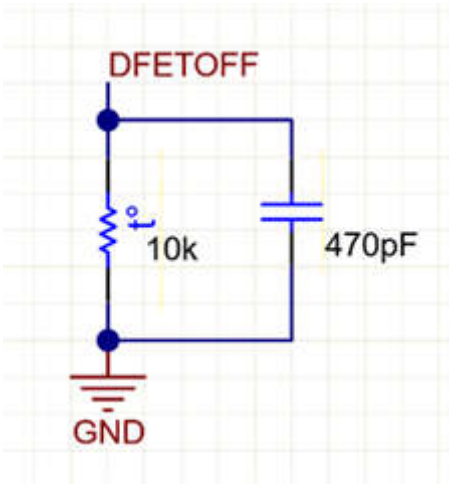

Figure 5-1. Typcial Thermistor Setup Utilizing DFETOFF

Figure 5-2 highlights the parameters to properly configure the pin to work as a temperature sensor with an 18kΩ pull-up resistor. When setting up the device, these four critical values need to be configured for the pin to

function as a temperature sense pin. The circled values configures the pin to act as a temperature sense pin that does not trigger protections with an 18kΩ pull-up resistor.

Bit	Function
OPT[5:4]	Pull-up control 00: selects 18 kΩ pull-up for thermistor measurement 01: selects 180 kΩ pull-up for thermistor measurement 10: selects no pull-up (used for ADCIN)
OPT[3:2]	Polynomial selection for thermistor temperature measurement 00: selects Calibration:18K Temperature Model 01: selects Calibration:180K Temperature Model 10: selects Calibration: Custom Temperature Model 11: no polynomial is used, raw ADC counts are reported.
OPT[1:0]	Measurement type 00: general purpose ADC input 01: thermistor temperature measurement, used for cell temperature protections 10: thermistor temperature measurement, reported but not used for protections 11: thermistor temperature measurement, used for FET temperature protection
PIN_FXN[1:0]	Selects Pin Function 00: Pin is used for communications, or not used at all. 01: General purpose digital output (GPO) 10: Alternate function (ALT) 11: Thermistor measurement or general purpose ADC input (AD)

Figure 5-2. Register Configuration for a Temperature Sense Pin

5.6 How many thermistors does the device support?

The device contains 3 dedicated thermistor pins, TS1, TS2, and TS3. However, the device also has 6 multi-function digital pins that can be configured to act as temperature sense pins, bringing the total number up to 9 unique thermal measurements.

5.7 Can thermal protections be disabled and are thermistors necessary for operation?

Yes, thermal protections can be disabled by modifying registers in memory. The device supports the disabling of protections in *Settings:Protection* for over temperature and under temperature cases. Likewise, the device also supports changing the trigger temperature for these situations in *Settings:Protection* across a range of -40C to 120C.

The bits [1:0] in the *Settings:Configuration:TSx Pin Config* register control whether or not the device uses thermistors. When configured to be 0x0, the pin is not used for thermal measurement. The pin only acts as a temperature sense input when the bits are set to 0x3.

5.8 Why do I need a capacitor across each thermistor?

A capacitor is not required and the device still functions properly without one. While not required, placing a capacitor across the thermistor is often recommended as this provides more consistent readings. Is important to not place too large of a capacitor, as to make the response time too slow for accurate measurement representation.

5.9 How are the thermistor coefficients calculated for temperature calibration?

The default parameters for the temperature sensors are based on the Semitec 103-AT (18k-model) and 204AP-2 (180k-model) thermistors. If these thermistors are not being used, TI provides the BQ769x2 Thermistor Coefficient Calculator. By downloading the *tool* and following the *Guide to Thermistor Coefficient Calculator Tool - BQ769x2*, a zip file is generated that contains a file that holds the necessary coefficients. These coefficients are then added to the *Calibration:Custom Temperature Model* registers.

5.10 Why is the thermistor coefficient calculator tool throwing errors?

The most common error for the thermistor coefficient calculator tool is that requires a space between the two tables in the “thermistor.txt” file as shown below. In addition, make sure the encoding format of the .txt file is UTF-8 and not UTF-16.

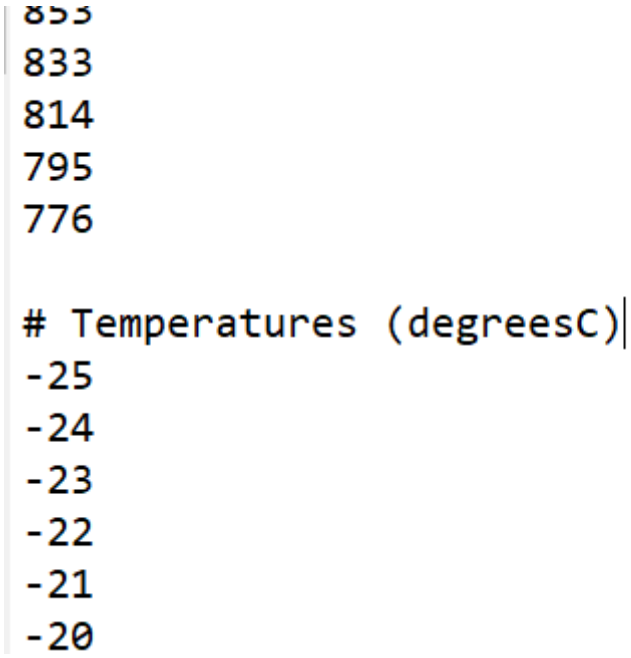

Figure 5-3. Proper Spacing in the thermistor.txt File

6 Cell Balancing FAQs

6.1 How does cell balancing work?

The BQ769x2 uses passive cell balancing. The fundamental circuit relies on an internal FET that can be enabled by the device. Once enabled, current is able to flow through the now connected VCx resistors. When charging, part of the charging current is redirected down this path while during discharge, the current comes from the cells. The excess energy is dissipated as heat from the resistors and FET. The control of balancing can either be handled by an external MCU or be allowed to run autonomously by the cell balancing algorithm of the BQ769x2. More information can be found in the application note Cell Balancing With BQ769x2 Battery Monitors.

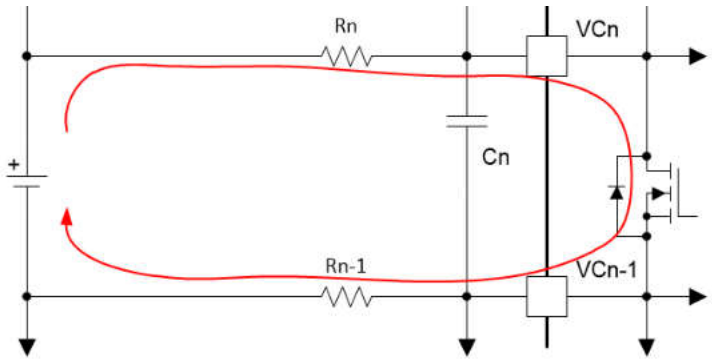

Figure 6-1. Typical Application Circuit of Cell Balancing

6.2 Can all battery cells be balanced simultaneously?

While the BQ769x2 device family allows the user to balance all (up to 16) cells at once, is not recommended. Depending on the balancing current, this can cause a large temperature rise within the chip. Is important to consider the thermal budget while defining the balancing algorithm. Is suggested to balance every other cell at a time to limit power dissipation.

6.3 Does the BQ769x2 support adjacent cell balancing?

Yes, if manual cell balancing is being used, adjacent cells can be balanced. However, on autonomous balancing, the cells are balance on a odd and even pattern. If using adjacent cell balancing on manual mode, considerations must be taken to avoiding exceeding the 100mA max cell balancing current or the max voltage across VC0. While balancing adjacent cells, more heat can also be generated, so thermal considerations must be taken into account. In general, is recommended to balance odd and even cells together.

6.4 How does cell balancing work in RELAX mode?

RELAX mode occurs when the CC1 current measurement falls below the SLEEP threshhold set in the *Settings:Configurations:Power Config[SLEEP]* register. When in RELAX mode, there are three important registers which control balancing that the user needs to configure.

1. **Cell Balance Min Cell V:** This register sets the voltage value where if the battery is not charging or discharging, cell balancing is disabled.
2. **Cell Balance Min Delta:** When not charging or discharging, this register holds the maximum allowed difference between the highest and lowest cell voltage before automatic cell balancing begins.
3. **Cell Balance Stop Delta:** When balancing in RELAX mode, this register holds the smallest possible delta between the highest and lowest cell voltages. Once the measured delta is smaller than the register value, the balancing stops.

6.5 Does the BQ769x2 support external balancing?

Yes, the device supports external N-channel or P-channel FETs to be used in balancing to support higher current for cell balancing while allowing for larger input resistors. Furthermore, external FETs help spread out the generated heat and keeping the device cooler versus internal balancing. With higher current available for

external cell balancing, the device can balance the cells faster to produce better results while avoiding thermal strain on the chip.

6.6 How large can the current sense resistors be at the VCx input pins?

Is recommended that the input resistors be between 20 and 100Ohms. This is to limit the total current flowing during balancing to protect the device from overheating while still balancing at a reasonable speed. Due to the higher current that flows through VC16, is recommended this to be kept at 20 ohms regardless of the other pins resistances. In addition, is also recommended to add a 0.22uF capacitor at each cell input.

6.7 Does cell balancing affect voltage measurement?

When cell balancing is enable, there is additional current flow into the top cell input for each cell balancing. The current produced causes a small IR drop across the top input resistor, resulting in a slightly lower voltage measurement. Is often good practice to have a lower input resistance on VC16 to account for this drop, generally 20Ohms. While a drop does exist in all cells, is larger on the top due to VC16 supplying current to supply current to the internal cell balancing FETs.

6.8 Why are the cells balancing for different amount of times?

There can be a slight difference on balancing time based on your systems configuration, this is more evident on applications with unused input cells and the way these are shorted. While tempting to connect the unused pins at one node, this can cause the same cell terminating at the node to be measured multiple times. Therefore, is best to spread out unused cells evenly throughout all the connections and not just in one central area to produce the best balancing results. An example for a good cell balancing distribution of a 12s configuration using the BQ76952 is shown below.

Cell-1	1
Cell-2	1
Cell-3	0
Cell-4	1
Cell-5	1
Cell-6	0
Cell-7	1
Cell-8	1
Cell-9	1
Cell-10	0
Cell-11	1
Cell-12	1
Cell-13	1
Cell-14	0
Cell-15	1
Cell-16	1

Figure 6-2. Example Unused Cell Distribution (1 = Used, 0 = Unused)

7 Device Power and State Switching FAQs

7.1 What is the maximum voltage of battery packs this device support?

The VCx pins are rated for 85V each, besides the VC0 pin. This limits most designs to 85V if using a single chip solution. If a larger voltage is needed, multiple BQ769x2s can be stacked in series to support higher voltage battery packs beyond 16-s setups. For more information, view the technical document How to stack battery monitors for high-cell-count industrial applications.

7.2 What is the maximum battery pack voltage allowed when using the charge pump?

When using the charge pump, pack voltages can not exceed 80V. Since the pins of the BQ769x2 are rated for 85V, the user needs to be careful when using high side driving when nearing 85V. While the charge pump is active, a V_{BAT} of up to 80V is supported using the 5.5V charge pump. If the 11V charge pump is being used, the peak voltage must be lowered to 74V.

7.3 Is necessary to tie BAT- to VSS?

Yes, BAT- must be tied to VSS when the device is being used. Failure to do so results in incorrect voltage measurements as VC0 (ground of the battery) and VSS (ground of the chip), as these are different. Most applications use a net-tie or 0-Ohm resistor to connect the two nodes at the systems, allowing to distinguish the routing of the BQ IC ground and the high-power ground used for the battery pack.

7.4 How my other signal GNDs needs to be connected to PACK-?

To connect sensitive electronics such as MCUs to the same GND as the battery pack, is recommended to use a net-tie or 0 Ohm resistor between signal GND and PACK- to provide a connection while still isolating most high current paths from low current paths. Is necessary to put this start ground connection near the BQ769x2 device.

7.5 Does a capacitor needs to be placed between VC0 and VC1?

No, a capacitor must not be placed between VC0 and VC1. For VC1, the capacitor mustbe connected to GND rather than VC0 as shown in Figure 7-1 with C9. By directly going to GND, the VC1 is less likely to spike below VSS when a short circuit transient occurs.

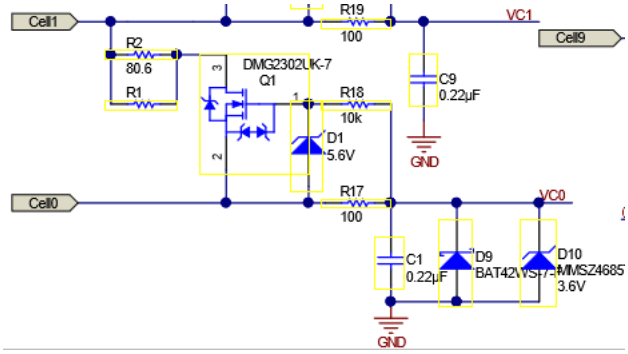

Figure 7-1. Proper Connections for the Capacitor for the CELL1 input (C9)

7.6 What are the recommended typical passive components values for my schematic design?

1. While REG1 and REG2 both use 1uF capacitors, REGIN needs a 22nF capacitor to VSS when used.
2. Adding resistors in series to the BREG BJT helps spread the power dissipation across multiple parts and reduces thermal stress on individual parts.
3. VC0-VC1, VC1-VC2, and VC15-VC16 cannot be shorted.
4. When configuring the BAT pin, is recommended to have a diode between BAT+ and the BAT pin with a capacitor to GND afterward. This allows the device to remain powered in case of a short circuit condition dropping the stack voltage to zero. The typical capacitance values is 1uF.
5. SRP and SRN must have a 0.1uF capacitor between each other. For additional filtering, 0.1uF capacitors from SRP and SRN to VSS can be added.

6. When in use, each SRP and SRN resistor must have a 100Ohm resistor connecting the pin to the respective end of the sense resistor, as shown below.

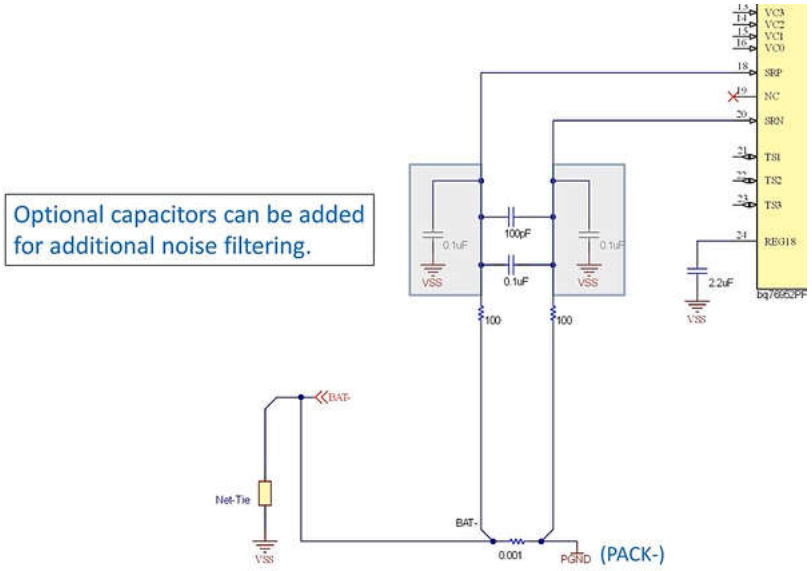

Figure 7-2. Proper Configuration of the SRP and SRN Pins

7. When using a 18kOhm thermistor, a 470nF capacitor is recommended, but when using an 180kOhm thermistor, the capacitance across must not exceed 400pF.
8. The smaller the resistance used at the FET gates, the faster the device can turn-on and turn-off. However, turning on too fast can result in damaging the the FETs so a resistance of more than 10kOhms is used for most single FET applications.
9. For the SRP/SRN sense resistor, the recommended resistance is 1mOhm, but is flexible based on application. However, is critical that the resistor has a thermal coefficient of 50ppm.

7.7 How much current can the two programmable LDOs provide?

Each LDO is capable of providing 45mA at 1.8V, 2.5V, 3V, 3.3V, or 5V. The LDOs are powered through the REGIN pin which can be connected to BAT+ through a BJT.

7.8 Can the LDO input transistor be connected to a lower voltage cell on the pack than BAT+ to increase efficiency?

No, this configuration is not recommended as hurts the efficiency of battery packs. Since the LDOs can draw up to about 90mA while in operation. Assuming the transistor is connected to the 2nd cell, such that the bottom two cells are pulling an additional 90mA. As the other cells are not seeing this extra current, this results in an imbalance between the cells and require balancing the top 10 or so cells down to match the lower two cells. This generates additional heat as the device balance the remaining cells.

7.9 In reference designs, why are two capacitors placed between VC16 and PACK+ as well as PACK+ and PACK-?

The capacitors (C28, C29, C30, and C31 in Fig. 10-1 below) are known as ESD capacitors. These provide a path for current to flow in case of an ESD event that bypasses both the FETs and battery. Two capacitors are put in series as an additional safety measure so that if one capacitor fails, there is not be a short circuit path between the two paths.

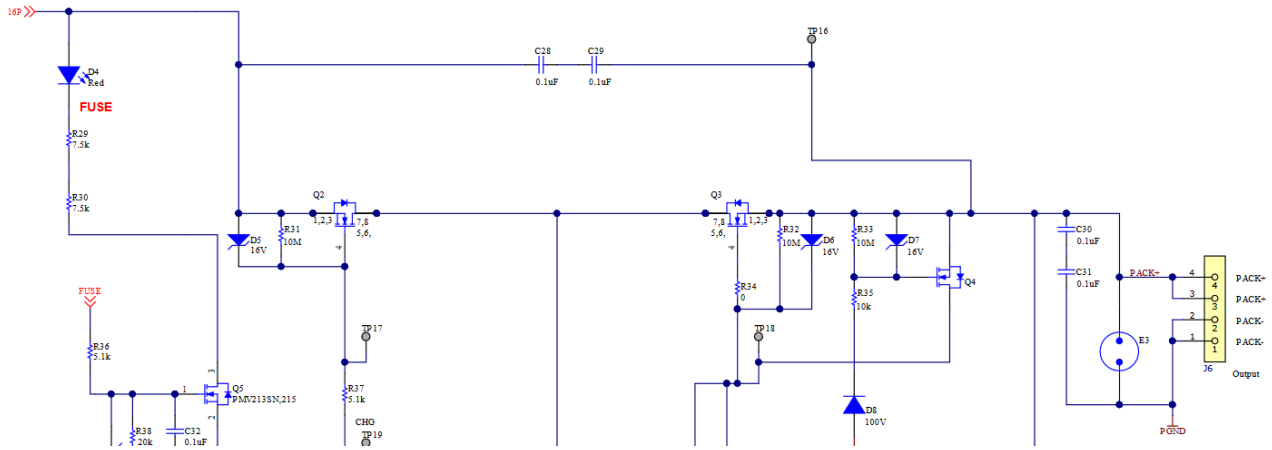

Figure 7-3. Schematic from the Data sheet Featuring ESD Capacitors

7.10 What are the different low power modes of the BQ769x2 device family?

The device features four modes: NORMAL, SLEEP, DEEPSLEEP, and SHUTDOWN. The first is used to operate at the highest performance and power usage when large loads are applied. SLEEP is best used on lighter loads where the risk of things going wrong are lower. DEEPSLEEP is optimized for keeping an MCU powered but little else, providing a very low energy usage. SHUTDOWN is the lowest energy consumption mode that is an excellent choice for long-term storage.

1. NORMAL Mode: All protections are enabled, both CFETs and DFETs can be on, constant voltage, current, and temperature measurements, with the LDO enabled and programmable.
2. SLEEP Mode: Most protections enabled, DFET on but not the CFET, ADC has intermittent sampling, the LDO still runs, and the device can leave SLEEP mode by rising current, communication, a charger, or a reset signal.
3. DEEPSLEEP Mode: Most circuits off, FETs off, no ADC or CC sampling, no protection features enabled, LDO still operates, and the mode can be exited by communication, chargers, or the reset signal.
4. SHUTDOWN Mode: All circuity is off except the wakeup detector, no measurements or protections, the LDO is disabled, and the device can exit the mode by being pulling TS2 to GND or attaching a charger.

7.11 How can an MCU know the BQ769x2 is in shutdown?

The best way to determine whether or not the BQ76952 is to measure the voltage of the REG18. If the voltage at the pin is zero, the device is in shutdown. Another alternative if the pin is configured to be used for SHUTDOWN is the TS2 pin. If the device is in shutdown, TS2 must read at roughly 5 volts.

7.12 Is disabling the SHUTDOWN mode possible?

Yes, by pulling down the TS2 pin low to VSS, the device is not be able to enter SHUTDOWN. Is important to set the SHUT_TS2 bit high in the *Settings: Configuration: Power Config* register so that the device does not rely on the pin to enter SHUTDOWN.

7.13 How does the BQ769x2 exit SHUTDOWN mode?

The device exits shutdown when the TS2 pin gets driven low towards VSS. Likewise, if the LD pin reaches a voltage higher than 1.45V, the device also exits shutdown and enter normal mode. If when trying to enter SHUTDOWN mode initially, not all conditions are met, the device enters soft SHUTDOWN. This is caused by a shutdown sequence being initiaed, but the TS2 or LD pin voltage are too high to be able to safely disable all protection features.

7.14 What is soft SHUTDOWN? How can I exit soft SHUTDOWN mode?

Soft SHUTDOWN acts as an intermediate state for the SHUTDOWN and NORMAL modes. While in this mode, FETs, protections, measurements, and communication are disabled, but the device is not able to completely shutdown until exits soft SHUTDOWN.

The device can exit soft shutdown mode in three ways. First, lowering the LD voltage below $V_{WAKEONLD}$ and then having raised above allows the device to turn on. Next is the RST_SHUT pin is held high for under 1 second and then lowered. This then perform a partial reset which clears the shutdown flag. The last way is to clear the conditions that triggered the soft shutdown and let the device enter SHUTDOWN. This can be done by lowering the LD pin to below $V_{WAKEONLD}$ or by raising the TS2 pin above $V_{WAKEONTS2}$.

8 Evaluation Modules and BQStudio FAQs

8.1 Does the BQ769x2 family have any EVMs?

Yes, there are EVM modules for both the BQ76942 and BQ76952. These can be found on each device's product page on the TI website under Hardware Development.

8.2 How much current the EVM consume while operating?

When powering up the EVM using a single supply and the battery simulator, is recommended to have a power supply that can at least supply 250mA of current. This must be placed across BAT- and CELL16. Make sure to populate cells 1,2, and 16 with resistors to emulate a cell across the pins.

8.3 Can I reduce the number of cells enabled on the EVM?

Yes, to reduce the number of cells tested, simply short the unused cells at the input terminal block. Make sure to always have a cell or resistor across VC0-VC1, VC1-VC2, and VC15-VC16.

8.4 Can multiple EVMs connect to one computer when stacking multiple EVMs?

While multiple EVMs can be connected to one computer for non-stacking applications, as long as an unique window of BQStudio is open for each EVM you wish to use.

For stacking applications, is important to realize that when stacking multiple EVMs that if all the EVMs are connected to the same computer, the GNDs of each board are shorted together inside the computer. In stacking applications, each board have different GNDs so such a short can damage a computer. Therefore, stacking is recommended to use different computers for connecting to EVMs.

8.5 Can the device interface with both SMBus and SPI at the same time?

SMBus utilizes I^2C to be able to communicate with the BQ769x2 devices while operating. While the SMBus is communicating via I^2C, the user must not try to write SPI messages from another microcontroller. SPI must never be used while the SMBus is active.

8.6 Why is BQStudio not detecting to the BQ769x2EVM?

To debug connection issues to BQStudio, first verify that you are running the newest version of BQStudio, which is the BQSTUDIO-TEST file.

Then proceed to follow the steps from the Quick Start Section of the EVM

1. Connect a power supply between BAT+ and BAT-.
2. Connect your computer via a USB cable to the EVM. Three green LEDs are turn on when the computer is connected.
3. Check BQStudio's Dashboard to verify that the on-board microntroller is connected and which firmware is using.
4. Only have one EVM connected to your laptop for each unique window of BQStudio being used.

9 Additional Instructional Material

9.1 How do I access functional safety documents such as a FMEDA and pin FMEA?

To view these documents, an NDA agreement needs to be in place. A local TI sales representative in your area can help set this up.

9.2 Is there any microcontroller code examples for the BQ769x2?

Code examples are available on the product folder and can be download here.

A video explain how to use BQStudio configuration to start your code can be found here.

9.3 Are there any reference designs for the BQ769x2?

Reference design are available on the product page and can be found here.

Currently, there are three reference designs available for the BQ769x2 family:

1. A 16s battery pack with low-side MOSFET control: https://www.ti.com/tool/TIDA-010216
2. A 10-16s battery pack with high-side MOSFET control: https://www.ti.com/tool/TIDA-010208
3. A 32s battery pack with high-side MOSFET control utilizing stacked monitors: https://www.ti.com/tool/TIDA-010247

9.4 Is there any documentation on stacking multiple BQ769x2 devices?

TI currently offers multiple resources for using multiple BQ769x2 devices to achieve higher cell counts. Some key examples are:

- For low-side FET stacking: https://e2e.ti.com/blogs_/b/powerhouse/posts/how-to-stack-battery-monitors-for-high-cell-count-industrial-applications
- For high-side FET stacking: https://www.ti.com/tool/TIDA-010247

9.5 Where can I find training videos to learn more about battery monitors and protectors?

TI has multiple training videos on the BQ769x2 family here.

This link provides both a general overview of battery management systems as well as a more in depth material on the BQ769x2 family by navigating to the Topic category labeled *"Battery Monitors"* on the right-hand side.

10 References

1. *BQ76972 3-Series to 16-Series High Accuracy Battery Monitor and Protector* data sheet (SLUSFC9)
2. *BQ76952 3-Series to 16-Series High Accuracy Battery Monitor and Protector* data sheet (SLUSE13B)
3. *BQ76942 3-Series to 10-Series High Accuracy Battery Monitor and Protector* data sheet (SLUSE14B)
4. *BQ769142 3-Series to 14-Series High Accuracy Battery Monitor and Protector* data sheet (SLUSE91B)
5. *Technical Reference Manual* for BQ76972 (SLUUCW9)
6. *Technical Reference Manual* for BQ76952 (SLUUBY2B)
7. *Technical Reference Manual* for BQ76942 (SLUUBY1B)
8. *Technical Reference Manual* for BQ769142 (SLUUCF2C)
9. *BQ769x2 Calibration and OTP Programming Guide* (SLUAA32A)
10. *BQ769x2 Software Development Guide* (SLUAA11B)
11. *Cell Balancing With BQ769x2 Battery Monitors* (SLUAA81A)
12. *BQ76952EVM User's Guide* (SLUUC33A)
13. *BQ76942EVM User's Guide* (SLUUC32A)

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