Application Note

Configurations of Secondary Rectifier Circuit for LLC Resonant Converter Using UCC24624

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ABSTRACT

The UCC24624 is a high-performance synchronous rectifier (SR) controller dedicated to LLC resonant converters. It integrates two independent SR control channels with interlock to prevent shoot-through into a single 8-pin SOIC package to minimize the external components and allow for easy PCB layout design.

In UCC24624 circuit design, the thermal performance of SR controller (UCC24624) and SR MOSFETs are one of main challenges in high frequency and high-power applications. This application note shows several configurations to help disperse heat to ensure the SR circuit is operating within its thermal safety range.

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1 Introduction

1.1 LLC Resonant Converter

LLC resonant converter is one of the most popular isolated DC-DC Converter because of its advantages of simple control, wide voltage gain regulation capability, and soft switching operation. It operates at 50% duty cycle and power flow is controlled by modulating the switching frequency.

In an LLC resonant converter, the zero-voltage switching (ZVS) at turn-on for the primary-side MOSFETs and zero-current switching (ZCS) at turn-off the rectifiers in the secondary-side can be achieved. Resonant operation of all switching devices in the LLC converter results in minimum switching loss and increased overall efficiency, especially at high operating frequency in the hundreds of kilohertz to Megahertz range.

1.2 Synchronous Rectification (SR)

1.2.1 Diode Rectification and Synchronous Rectification

SR is widely used in LLC resonant converter to improve power supply efficiency to meet stringent energy-saving standards. If a MOSFET is turned on and off in synchronization with the diode rectifier, it can be used to replace the diode. Instead of a fixed voltage drop, when the MOSFET conducts, its voltage drop is proportional to its on-state resistance ($R_{DS(ON)}$) and the instantaneous current (I_F). When the resistance is low enough, the MOSFET can achieve much lower conduction loss and less heat is generated.

Figure 1-1 shows the equivalent circuits for diode and SR MOSFET, respectively. Figure 1-1 (a) shows the linear approximation model of the diode conduction loss as a fixed voltage drop (V_F) in series with a resistor (R_D). As regards SR, if it is ideally controlled in synchronization with the current flowing, the SR MOSFET can be simplified as a resistor ($R_{DS(ON)}$), as shown in Figure 1-1 (b).

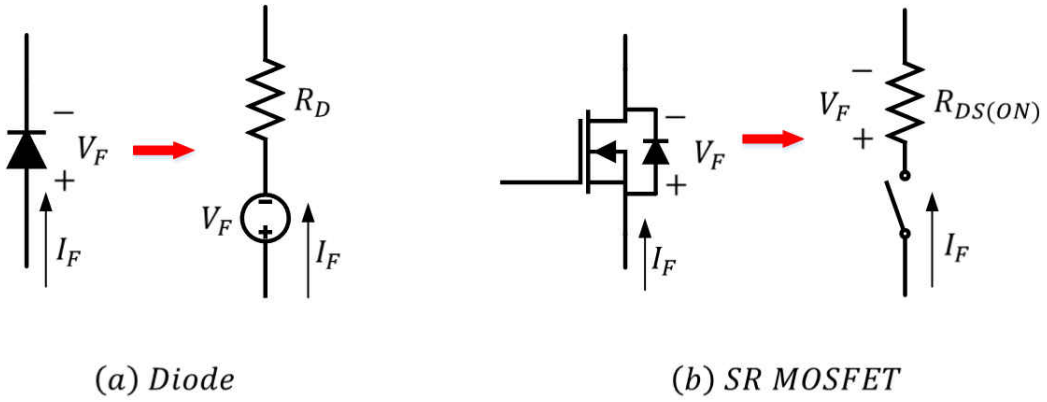

Figure 1-1. Equivalent Circuits for Diode and SR MOSFET

According to equivalent circuits shown in Figure 1-1, forward voltage drop can be calculated with Equation 1 and Equation 2, respectively.

$$V_{DIODE\_RECTIFIER}(I_F) = V_F + I_F * R_D \quad (1)$$

$$V_{SYNC\_RECTIFIER}(I_F) = R_{DS(ON)} * I_F \quad (2)$$

Additionally, SR MOSFETs offer extra advantages such as the ability to operate in parallel to prevent overheating in high-power applications. MOSFETs $R_{DS(ON)}$ have a positive temperature coefficient. When operating in parallel, resistance increases with the temperature rise, shifting power to the cooler device. By contrast, diode forward voltage drop has a negative temperature coefficient. Increasing temperature results in increased current flow in the hotter device, and increases the chance of overheating. It is worth noting that some of Silicon Carbide (SiC) diodes have a positive temperature coefficient, however, the price is still too high in the market and most of SiC diode vendors focus on high voltage rail (≥ 600 V) applications.

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1.2.2 Power Loss for Synchronous Rectification

The designer should compare all SR MOSFET parameters for its optimum selection in a given application instead simply choosing the lowest $R_{DS(ON)}$ MOSFET. The lower $R_{DS(ON)}$ MOSFET usually has higher gate charge Q_g such that the driving losses could become a critical factor for both light load and full load efficiency at high frequency. It means, even though the lower $R_{DS(ON)}$ MOSFET gives better efficiency at a heavy load, it might bring less efficiency at lighter load because of higher Q_g.

SR loss is the sum of conduction losses and switching losses.

Conduction losses are defined by the $R_{DS(ON)}$ of the MOSFET and the forward voltage of the internal body diode, V_{SD}. The calculation for the loss caused by SR MOSFET channel conduction can be done with the following Equation 3 and Equation 4. Note that the current for calculation in Equation 4 is not output current and is the RMS current (I_{RMS}) flowing through the SR MOSFET.

$$I_{RMS} = \frac{\pi}{2\sqrt{2}} * I_{OUT} \tag{3}$$

$$P_{FET\_CON} = R_{DS(ON)} * \ I_{RMS}{}^2 \tag{4}$$

To avoid a current shoot through, a dead time and interlock function need to be added. This causes the current to flow through the MOSFET body diode at the beginning of the SR conduction time(t_{delay}). The diode power loss can be calculated by using diode forward drop (V_F), body diode current (I_{SD}) , t_{delay} and switching frequency (f_{sw}).

$$P_{DIODE\_CON} = V_F * \ I_{SD} * \ t_{delay} * \ f_{sw} \tag{5}$$

Thus, the total conduction loss P_{TOTAL_CON} in SR MOSFETs is calculated as

$$P_{TOTAL\_CON} = P_{FET\_CON} + P_{DIODE\_CON} = R_{DS(ON)} * I_{RMS}{}^2 \ + \ V_F * \ I_{SD} * \ t_{delay} * \ f_{sw} \tag{6}$$

Gate drive losses of the SR P_{GATE} are defined by the gate charge Q_g, the gate driving voltage V_{gs}, switching frequency f_{sw} and the number of the MOSFET in parallel N. This value can be estimated through Equation 7. The gate drive loss P_{GATE} is dissipated in the gate driver circuits, including the driver output impedances, the external gate resistor, and the SR MOSFET internal gate resistance, so P_{DRV} could be calculated as Equation 8.

$$P_{GATE} = 2 \ * Q_g \ * V_{gs} * \ f_{sw} * \ N \tag{7}$$

$$P_{DRV} = \frac{P_{GATE}}{2} * \left(\frac{R_{VG\_PU}}{R_{VG\_PU} + R_{gate} + R'_g} + \frac{R_{VG\_PD}}{R_{VG\_PD} + R_{gate} + R'_g} \right) \tag{8}$$

1.2.3 UCC24624 Introduction

The UCC24624 is a synchronous rectifier (SR) controller designed especially for high efficiency LLC resonant converter. The UCC24624 SR controller uses drain-to-source voltage (VDS) sensing to determine the SR MOSFET conduction time. When the current starts to flow into the SR body diode, the VDS is the body diode forward voltage drop. The SR MOSFET is turned on when its VDS falls below turn-on threshold(-265mV) longer than turn-on delay. After SR turns on, its voltage drops changes from body diode forward voltage drop into the $R_{DS(ON)}$ voltage drop, and is turned off when VDS rises above the programmable turn-off threshold.

The SR MOSFETs are often turned off early than expect which caused by parasitic inductance. The parasitic inductance can be the contribution from both the trace inductance from the layout and the device package inductance. The designer could optimize the layout to eliminate trace inductance, however package inductance cannot be eliminated. The UCC24624 allows designer to further increase the turn-off threshold to accommodate higher parasitic inductance MOSFET. As shown in Figure 1-2, by connecting a resistor R_{offset} from VSS pin to the SR MOSFET source, the voltage drop across the external resistor increases the turn-off threshold.

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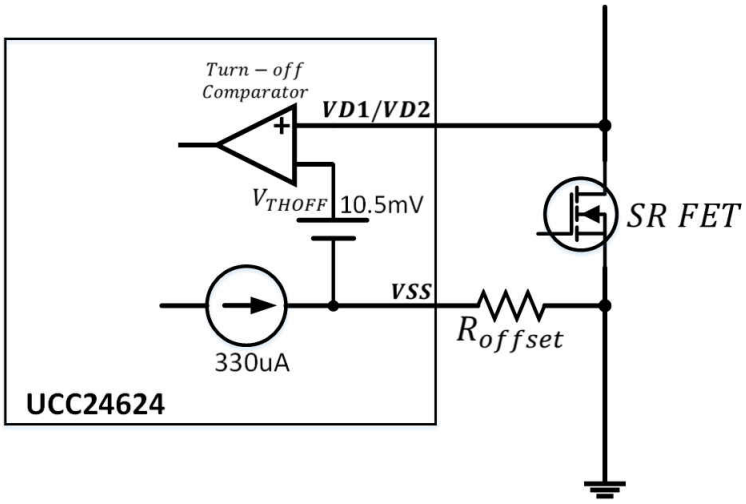

Figure 1-2. Adjustable Turn-off Threshold

The desired turn-off threshold V_{THOFF} could be calculated as:

$$V_{THOFF} = 10.5mV + 330uA * R_{offset} \quad (9)$$

Additionally, the UCC24624 also integrated proportional gate drive feature which could further extend MOSFET conduction time. The proportional gate drive reduces the SR MOSFET gate voltage when the SR current is small, and increases its voltage drop. The increased voltage drop could overwhelm the offset voltage introduced by the package inductance. It could bring higher efficiency, due to reduced body diode conduction time. During the proportional gate driver activated region, the SR gate voltage very close to its threshold, and it allows the SR to be turned off fast without considering the time delay from discharging the gate voltage to the threshold voltage.

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2 Configurations of Secondary Rectifier Circuit using UCC24624

2.1 Typical Configuration

A typical configuration of UCC24624 is shown in Figure 2-1. The UCC24624 provides two high current gate drive outputs, each capable of driving one or N channel power MOSFETs. Each gate driver is controlled separately and an interlock logic circuit prevents the two synchronous rectifiers from being on at the same time.

The control scheme in UCC24624 switches on each SR MOSFET when its VDS falls below -265mV turn-on threshold, and turns it off when VDS rises above the turn-off threshold. The turn-off threshold could be adjusted to maximizing the conduction time of the SR MOSFETs to compensate the offset voltage caused by the parasitic inductance.

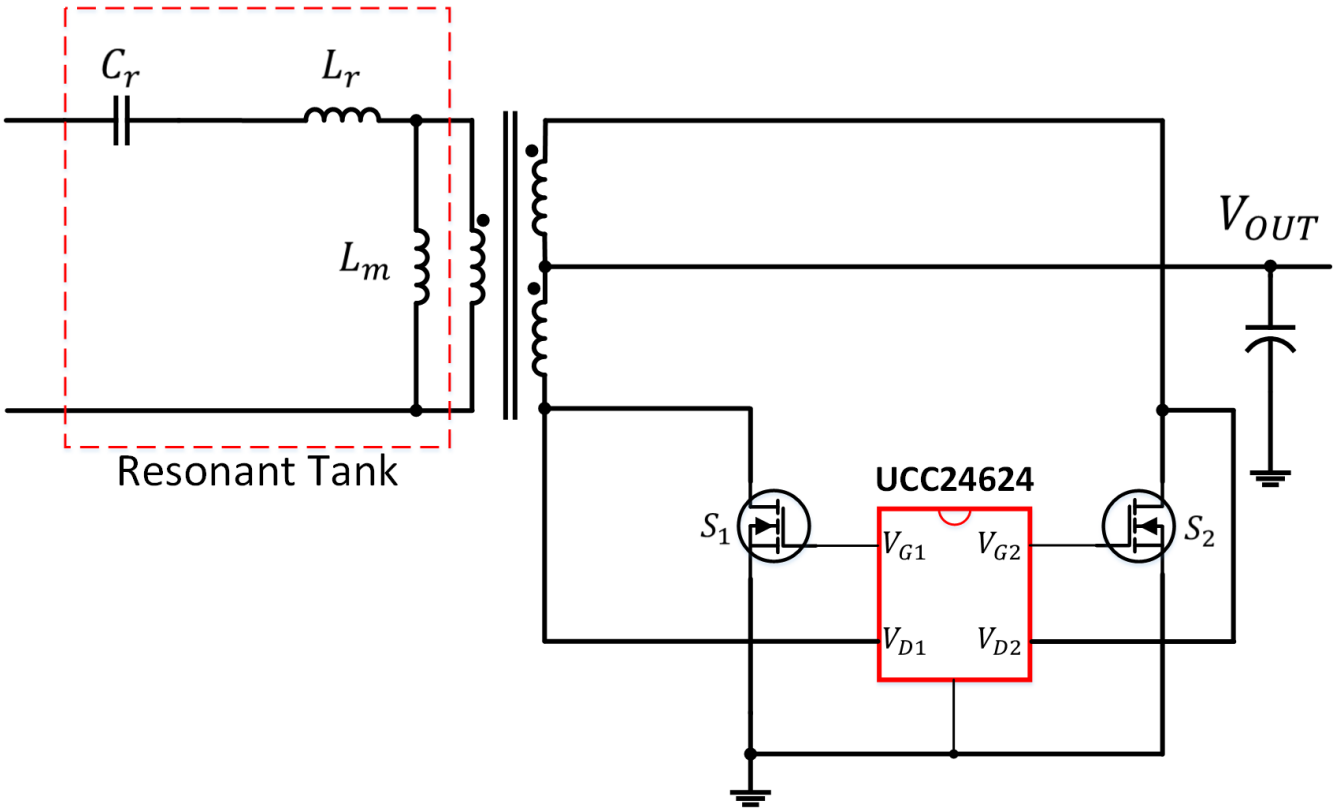

Figure 2-1. UCC24624 Typical Application Schematic

2.2 Single SR Controller with Paralleled MOSFETs Configuration

In higher power level applications, a number of MOSFETs can be paralleled to achieve lower on-state resistance and reduce conduction loss as shown in Figure 2-2. Also, the $R_{DS(ON)}$ has a positive temperature coefficient so the FETs will automatically share current, facilitating optimal thermal distribution among the SR devices. This improves the thermal management.

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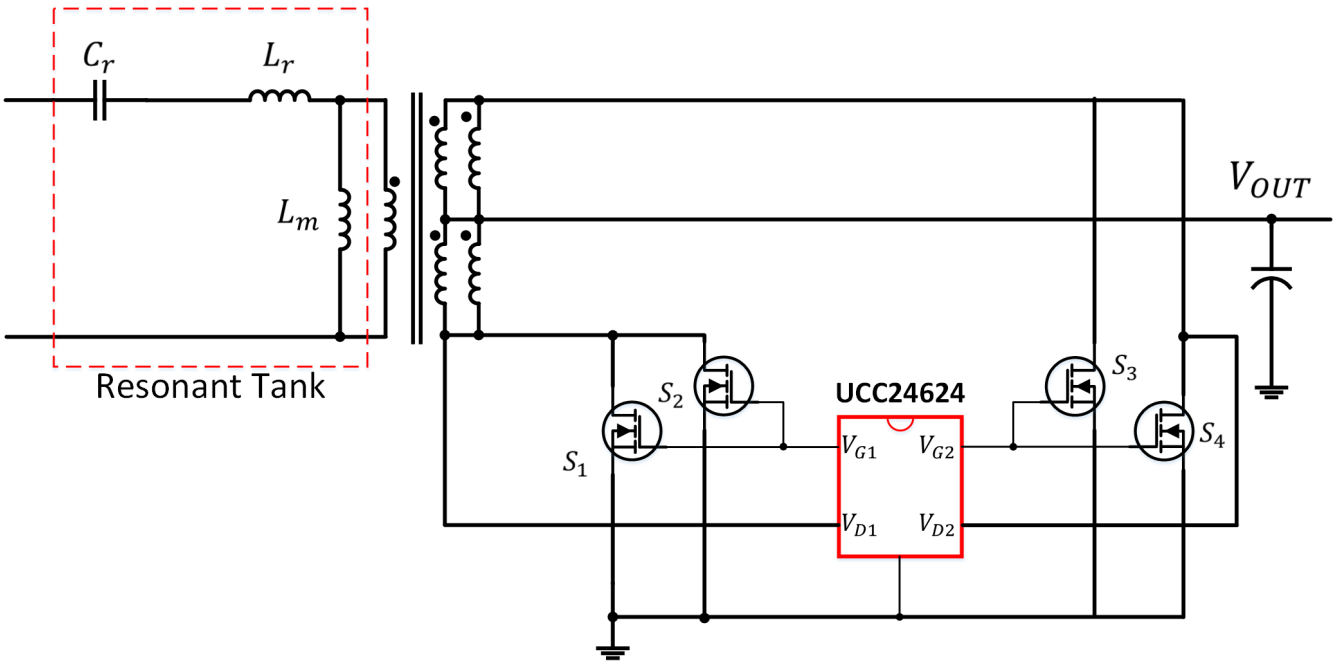

Figure 2-2. Single UCC24624 with Parallel MOSFETs Application Schematic

To minimize the size of the converter and decrease output ripple voltage for low-voltage applications, designers often increase the switching frequency to reduce the size of the output inductor and capacitor. If multiple FETs are in parallel, increased switching frequency increases the gate drive losses which might make UCC24624 overheat. According to Equation 7, the gate driver losses greatly increases as shown in Equation 10.

$$P_{GATE} \uparrow \uparrow = 2 * Q_g * V_{gs} * f_{sw} \uparrow * N \uparrow \quad (10)$$

2.3 Dual SR Controllers with Paralleled MOSFETs Configuration

The SR controller has limited capability to drive paralleled MOSFETs at higher switching frequency, due to its packaging and thermal constrain. To improve the thermal management of the SR controller UCC24624, a new structure of using a dual SR controller is proposed.

The new structure uses one UCC24624 to drive the SR on each side of a center-tapped transformer. The benefit of this structure is UCC24624 just needs to drive one side of the FETs which could reduce the power dissipation to half. Figure 2-3 shows the proposed structure.

Dual SR controller implementation can effectively divide total driving loss into two separate controllers and it can make each UCC24624 operate within its thermal limit. According to Equation 7, each UCC24624 just needs to handle half of the total driving loss as Equation 11.

$$P_{GATE} \uparrow \downarrow = \frac{1}{2} * 2 * Q_g * V_{gs} * f_{sw} \uparrow * N \quad (11)$$

Noted, the introduced additional SR controller UCC24624 increases the static power loss. However, it can be neglected comparing with the overall system power level.

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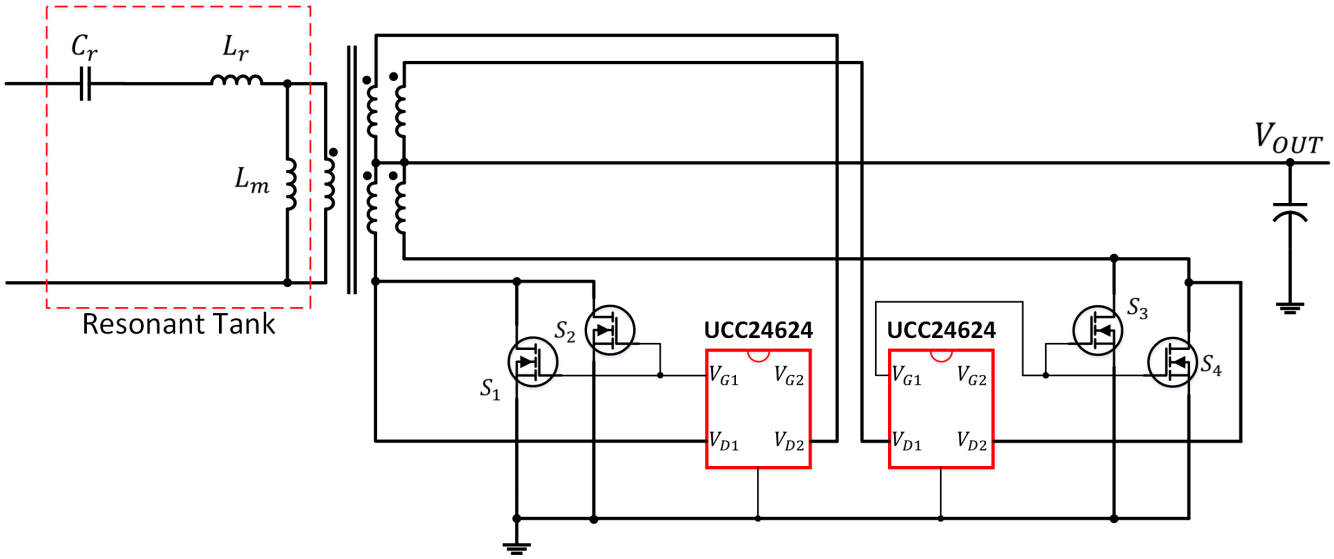

Figure 2-3. Dual UCC24624 Application Schematic

2.4 Multi SR Controllers with Matrix Transformer Configuration

For applications that require low-voltage and high-current outputs, such as OLED TV, server, or telecom, a matrix transformer with multi SR controllers is an attractive solution. The concept of matrix transformer is to use several small transformers to replace the single big transformer, with the primary-side windings in series and the secondary-side windings in parallel. Since the primary-side current for different transformers is the same due to a series connection, the secondary current is balanced.

The benefits of the matrix transformer are that it can share current among secondary windings, reduce leakage inductance and winding resistance, and improve thermal performance by distributing the power loss throughout the transformers.

In Figure 2-4, a single transformer is divided into four transformers.

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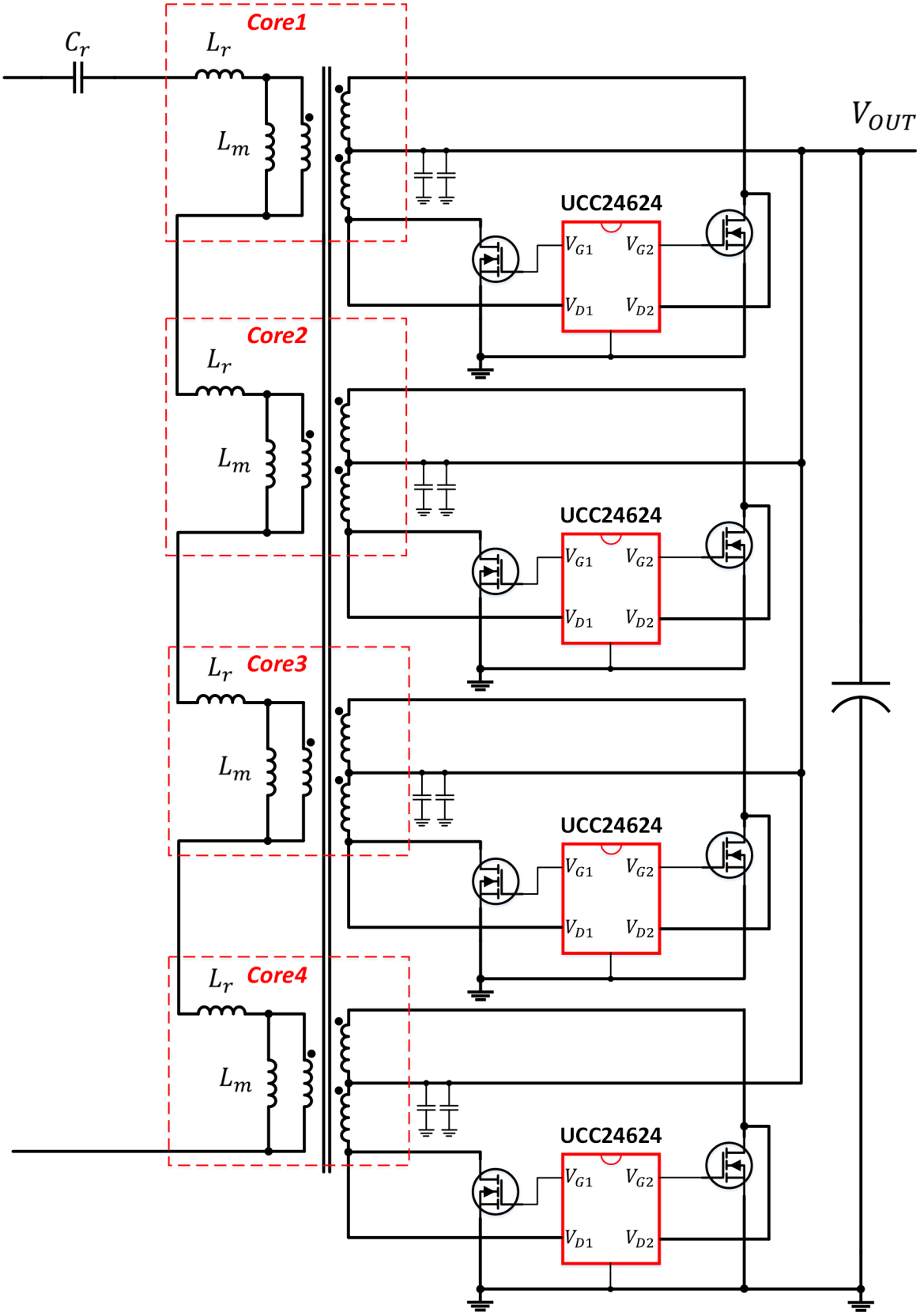

Figure 2-4. Multi UCC24624 with Matrix Transformer Application Schematic

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It is recommended to put the ceramic capacitor locally close to center-tap to filter out the high frequency current and improve the efficiency. Since the electrolytic capacitor has large ESL and ESR, the added ceramic capacitors normally can bypass all the high- frequency current.

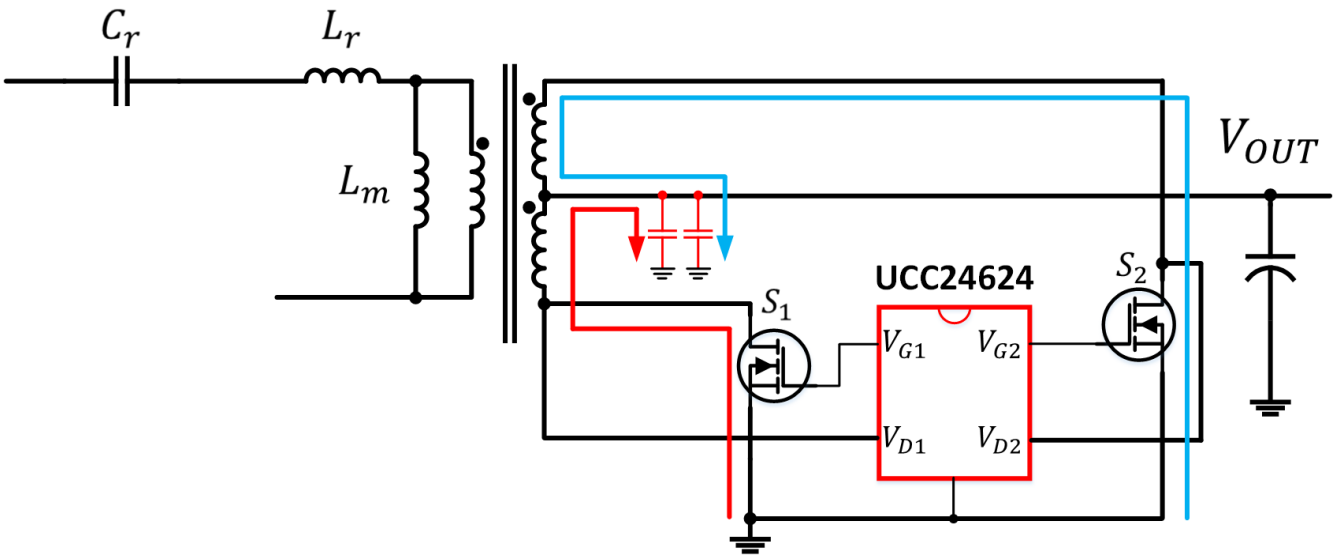

Figure 2-5. Recommended AC Coupling Ceramic Capacitors

Furthermore, a novel matrix transformer structure can be integrated multiple transformers into a single core as shown in Figure 2-6. This winding structure fully utilizes the available PCB copper and space, further minimizes the core loss. For more detailed winding of the transformer, please refer to reference [6].

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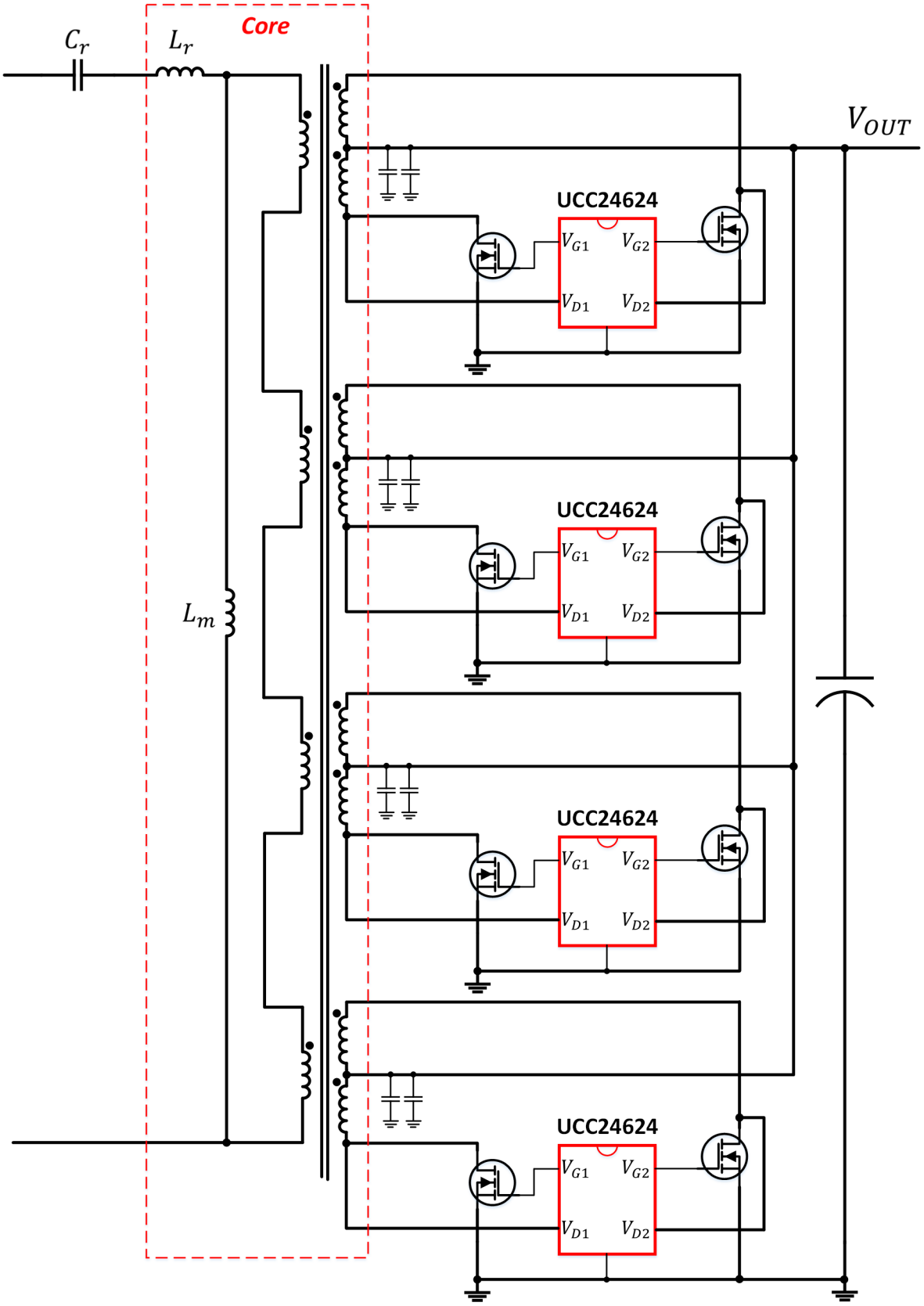

Figure 2-6. Multi UCC24624 with Novel Matrix Transformer Application Schematic

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3 Summary

In an SR design of LLC resonant converter, the designer needs to consider SR not only pass efficiency requirement, but also need to manage the thermals conditions. This application note introduces several secondary rectifier configurations of UCC24624 to help distribute the heat to ensure the SR circuit operating in its thermal safety limit.

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