Tech Note

How to Identify Allocated Power at PD Through TPH, TPL, and $\overline{BT}$ Pins

The state of TPH, TPL and $\overline{BT}$ pins are used to provide information relative to the PSE Type (1-2 or 3-4) and its available power. Table 1 lists the encoding corresponding to various combinations of PSE Types, PD Classes and the allocated power levels when a PSE is able to supply the full PD requested power. Table 2 corresponds to cases where the PSE's available power is lower than what the PD is requesting, and the resulting power that is allocated at the PD. This scenario where a PSE allocates less power to PD than what the PD requested is called Power Demotion, and PD's are required by the IEEE 802.3bt standard to support this.

Note: to simplify this content, this document only focuses on Single Signature PDs, but the same application of the TPH/TPL/$\overline{BT}$ pin statuses can be applied to each channel of a Dual Signature load.

Table 1 describes the condition when PSE's available power (as configured by register 0x29 in TI's Type 3 / Type 4 PSEs) is equal to or exceeds the PD's requested class. Table 1 is only applicable for TPS2372 and TPS2373 family. For other product, please review its data sheet.

Table 2 describes the conditions when a PD presents a classification level is greater than the PSE's available power (as configured in register 0x29 with TI's Type 3 and Type 4 PSEs).

The PD system is required to have intelligence to identify PSE port's power capability through the TPH and TPL pins to determine how much power the load can draw before start drawing any load. The PD is not allowed to draw more power than allocated power at PD based on IEEE802.3bt standard.

The steps should look similar to the following:

1. PD side's MCU should already know PD's class level and expected TPH/TPL/$\overline{BT}$ pin status according to table 1. Note: class 0-4 PDs can have 2 valid pin statuses as Type 1, 2, and 3 PSEs have class overlaps.
2. Upon power on and before drawing any load (MPS should be applied to keep PSE port on), the PD side's MCU should read the TPH/TPL/$\overline{BT}$ pin status and compare this with its expected status based on its designed class level.
   a. If the pin status matches the expected values from Table 1, it means the PSE has enough power capability to support the full PD load. The PD may then apply its full load after inrush (note: the power can't exceed the Pclass).
   b. If the TPH/TPL/$\overline{BT}$ status doesn't match the expected values in table 1, then compare the pin status with Table 2 and determine how much power has been allocated. The max power the PD can draw after inrush then becomes the allocated power at PD.

Example 1: PSE available power > PD requested power

PD is class 6, PSE is Type 4 and PSE's available power is set to 90W

Step 1: PD controller is set to class 6 through Class resistors. From Table 1, the expected TPH/TPL/$\overline{BT}$ pins status of class 6 if PSE has enough power would be Low - High - Low.

Step 2: PSE sees PD class level is lower than PSE's 90W (Class 8) available power, the PSE sends 4-finger classification, and the actual pin status is Low-High-Low which matches the expected pin status. So the PD is able to apply its full load (max 51W) after inrush.

Example 2: PSE available power < PD requested power

PD is class 6, PSE is Type 3, but the PSE port's available power is set to 45W.

Step 1: PD controller is set to class 6 through class resistors. From Table 1, the expected TPH/TPL/$\overline{BT}$ pins status for class 6 if PSE has enough power would be Low - High - Low.

Step 2: Since the PSE sees the PD's requested class level is higher than the PSE's 45W (Class 5) available power. The PSE will only send a 2 or 3 finger classification, and the actual TPH/TPL/$\overline{BT}$ pin status

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will be High-Low-Low which doesn't match the expected pin status.

Step 3: Find the allocated power at PD in table 2 for High-Low-Low which is 25.5W. So, the PD can't draw more than 25.5W after inrush.

Example 3: PSE available power < PD requested power

PD is class 7, PSE is Type 3, but the PSE port's available power is set to 60W.

Step 1: PD controller is set to class 7 through class resistors. From Table 1, the expected TPH/TPL/$\overline{BT}$ pins status of class 7 if PSE has enough power should be Low-Low-Low.

Step 2: Since the PSE sees the PD's requested class level is higher than the PSE's 60W (Class 6) available power. The PSE will only send a 4-finger classification, and the actual TPH/TPL/$\overline{BT}$ pin status will be Low-High-Low which doesn't match the expected pin status.

Step 3: Find the allocated power at PD in Table 2 for Low-High-Low which is 51W. So, the PD can't draw more than 51W after inrush.

Table 1. TPH, TPL, $\overline{BT}$ and Allocated Power Truth Table

PSE Type	PD class	Number of class cycles	Allocated power at PD(W)	TPH	TPL	$\overline{BT}$ (*)	Note
1-2	0	1	12.95	High	High	High	
1-2	1	1	3.84	High	High	High	
1-2	2	1	6.49	High	High	High	
1-2	3	1	12.95	High	High	High	
2	4	2	25.5	High	Low	High	
3-4	0	1	12.95	High	High	Low	
3-4	1	1	3.84	High	High	Low	
3-4	2	1	6.49	High	High	Low	
3-4	3	1	12.95	High	High	Low	
3-4	4	2-3	25.5	High	Low	Low	
3-4	5	4	40	Low	High	Low	
3-4	6	4	51	Low	High	Low	
4	7	5	62	Low	Low	Low	Not applicable for Type 3 PDs
4	8	5	71	Low	Low	Low	Not applicable for Type 3 PDs

Table 2. Power Demotion Cases

PSE Type	PSE Available Power (W)	PD class	Number of class cycles	Allocated power at PD(W)	TPH	TPL	$\overline{BT}$(*)
1-2	15.4	4-8	1	12.95	High	High	High
2	30	5-8	2	25.5	High	Low	High
3-4	15.4	4-8	1	12.95	High	High	Low
3-4	30	5-8	2,3	25.5	High	Low	Low
3-4	60	7-8	4	51	Low	High	Low

Table 1 and Table 2's (*):The $\overline{BT}$ output is not required to indicate how much power is allocated to the PD by an IEEE802.3bt compliant PSE. However, it gives additional information on the Type of PSE that is connected.

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