Application Report
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UCC24610 and UCC24612 Synchronous Rectifier Range Extension Guide

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ABSTRACT

The UCC24610/12 are high-performance controllers and drivers for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification. This guide will demonstrate how to extend the operating range of the UCC24610 from the datasheet's typical application configuration and show the range that the UCC24612 offers. The datasheet of the UCC24610 only shows how to configure the device ground referenced for a 5-V output. This is not the case, as the device can be configured on both high-side and low-side at output voltages beyond the absolute max of the device. However, the UCC24612 has an extended drain voltage limit allowing it to be used in situations considered out of range for the UCC24610.

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1 Purpose of the Synchronous Rectifier and UCC24610/12 Usage

The synchronous rectifier (SR) MOSFET replaces the diode as the output rectifier, thereby drastically reducing the conduction losses. The UCC24610/12 use drain-to-source voltage sensing, making them ideal for isolated switch-mode power supplies, such as flyback and LLC topologies.

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2 When to Use Which Controller

The UCC24610 is optimized for output voltages from 4.5 V to 5.5 V, but can be extended as shown in this document, and offers a programmable false-triggering filter, a programmable timer to automatically switch to light-load mode at light load, and a SYNC input for optional use in continuous conduction mode (CCM) systems. Protection features on TON and EN/TOFF pins prevent run-away on-time due to open-circuit or short-circuit fault conditions.

The UCC24612 offers proportional drive together with the CCM cycle limit pre-turn off to make the part operate more reliably in CCM operations. The wide VDD voltage range allows the UCC24612 to support up to 24-V applications without any range extension modifications. The 9.5-V gate driver clamping level allows for minimum driving loss. The UCC24612 uses adaptive off-time control to improve the noise immunity. This greatly simplifies the design effort and allows the controller be used in wide range of application and frequency ranges.

Both devices can be used in either high-side or low-side configurations. Typically, low-side SR is simplest and easiest to design, whereas high-side SR requires some design adjustments and extra circuitry. Despite the complexity, high-side may be preferred due to its better EMI performance.

NOTE: This configuration guide should not be used in place of the datasheet, but in conjunction with it for SR design.

3 UCC24610 and UCC24612 Comparison

Both UCC24610 and UCC24612 use drain-source sensing to operate. While they have the same function, their electrical specifications showcase important differences.

The absolute maximum ratings and recommended operating conditions for the UCC24612 has a wider voltage range, broadening the range of applications initially not possible with the UCC24610.

Table 1. UCC24610 and UCC24612 Comparison

PARAMETER	DEVICE	MIN	MAX	UNIT
V_{IN} VCC/VDD input voltage	UCC24610	4.5	5.5	V
	UCC24612	4	28	
VD for $I_{VD} \leq -10$ mA	UCC24610	–1.0	50	V
	UCC24612	–1.0	230	

4 VCC/VDD Extension Explained

UCC24610 has a very limited input voltage range, 4.5 V to 5.5 V, which makes it difficult to have any outputs higher than range if the output of the system is tied to the input of the UCC24610, which is usually the case. In order to overcome that limitation and extend the working range of the UCC24610 , small additions are required in the biasing circuitry. The first method described in this application note is to add an LDO voltage regulator from the output to the input of the device to provide proper biasing, as shown in Figure 2 .However, depending on the output voltage of the system, the difference between the output voltage and regulator voltage can lead to additional power losses.

To decrease losses from the LDO, an additional bias winding is added. This winding supplies the synchronous rectifier device with a bias voltage rather than using the output voltage of the system. This configuration is shown in Figure 6.

The UCC24612 has a larger input voltage range than the UCC24610 but the same biasing techniques apply when the output voltage is out of the UCC24612's input range.

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5 UCC24610 in Typical 5V Output Configuration

This is the standard TI low-side SR configuration, where V_{OUT} is +5V and the drain of Q_{SR} ,V_{VD}, is less than 50 Vpk.

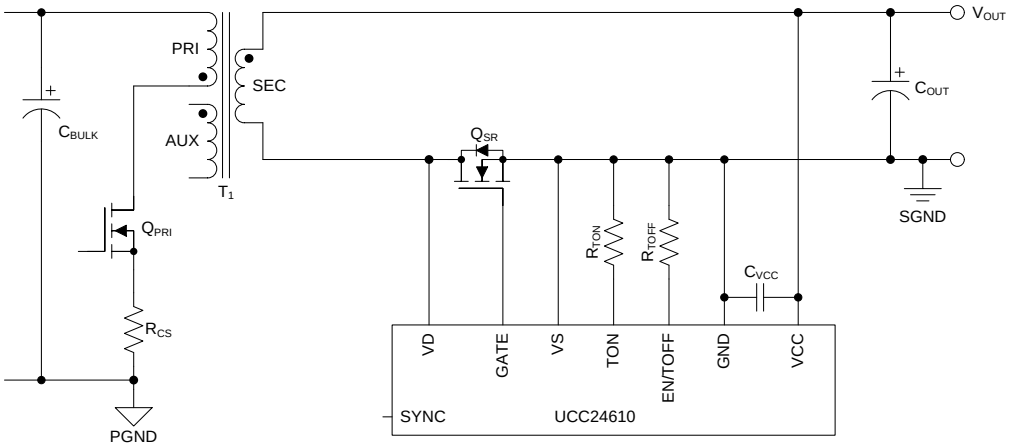

Figure 1. UCC24610 in Typical 5V Output Configuration

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6 UCC24610/12 in Low-Side SR

In all of the following configurations, VD must be less than the VD absolute maximum voltage.

These configurations provide a bias voltage for the UCC24610/UCC24612 when the output voltage of the system would not be appropriate to use.

UCC24610 in Low-Side SR:

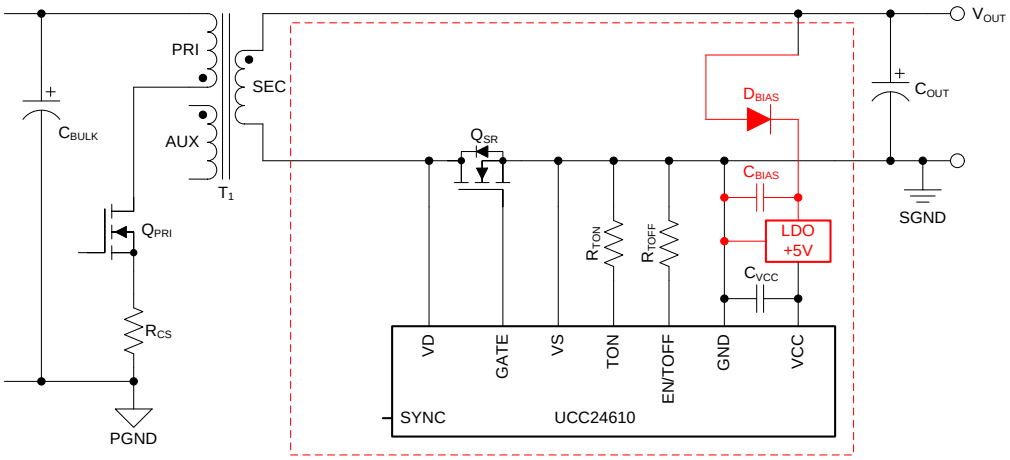

Figure 2. UCC24610 in Low-Side SR

D_{BIAS} is not actually necessary, but shown to complement the high-side arrangement.

UCC24612 in Low-Side SR:

The UCC24612 implementation for output voltage greater than 5 V does not require any additional circuitry because the voltage operating ratings of the UCC24612 are higher than those of the UCC24610.

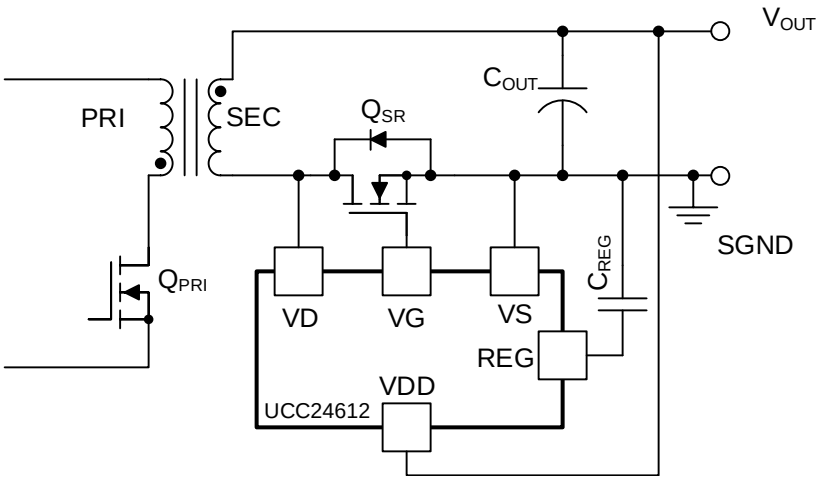

Figure 3. UCC24612 in Low-Side SR Configuration

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7 UCC24610/12 in High-Side SR

UCC24610 in High-Side SR:

In this configuration D_{BIAS} is necessary. During the on time of the primary switch, C_{BIAS} will see a voltage V_{OUT} with respect to V_{SEC} and will get charged. During the off time of the primary switch, the diode D_{BIAS} will prevent the capacitor from discharging.

This configuration may have excess VCC bias loss due to high voltage difference between V_{SEC} and V_{OUT} placed on the LDO.

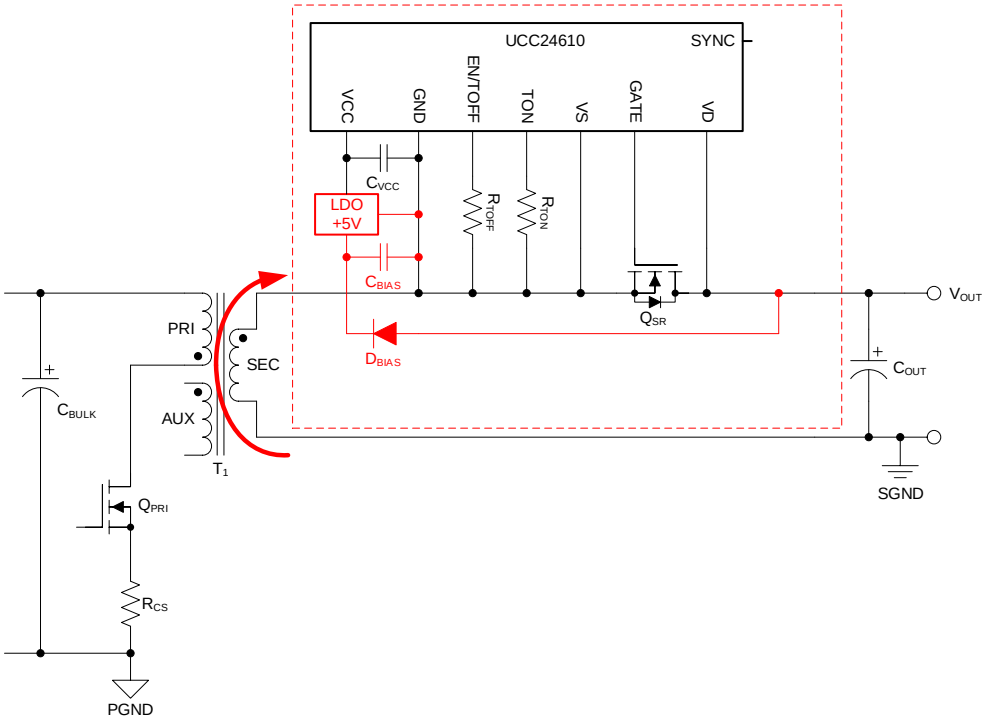

Figure 4. UCC24610 in High-Side SR

UCC24612 in High-Side SR:

The UCC24612 implementation for output voltage greater than 5 V does not require any additional circuitry because the voltage operating ratings of the UCC24612 are higher than those of the UCC24610.

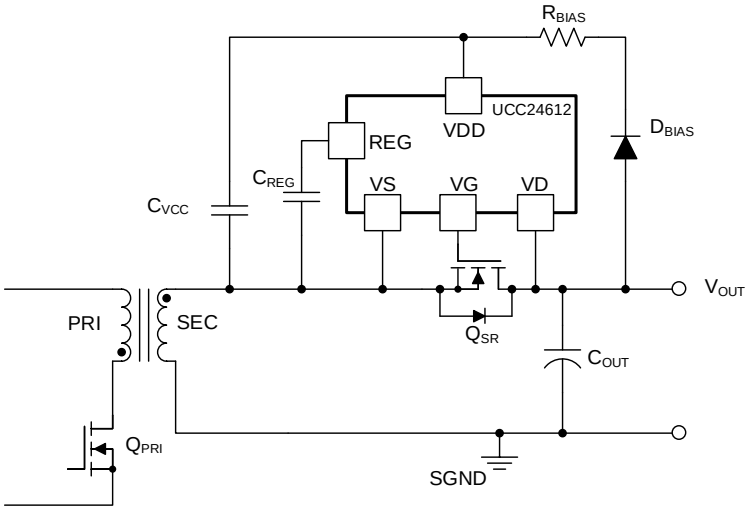

Figure 5. UCC24612 in High-Side SR Configuration

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8 UCC24610/12 in Low-Side SR with Bias Winding

This implementation reduces the VCC bias loss mentioned in Section 7 by using a winding to generate a lower voltage for the LDO.

This configuration can also be used to bias the device when the output voltage would otherwise be too low, such as in USB mobile charging applications where during a constant current under-voltage, the SR controller is expected to operate down to 3.0V or similar.

UCC24610 in Low-Side SR with Bias Winding:

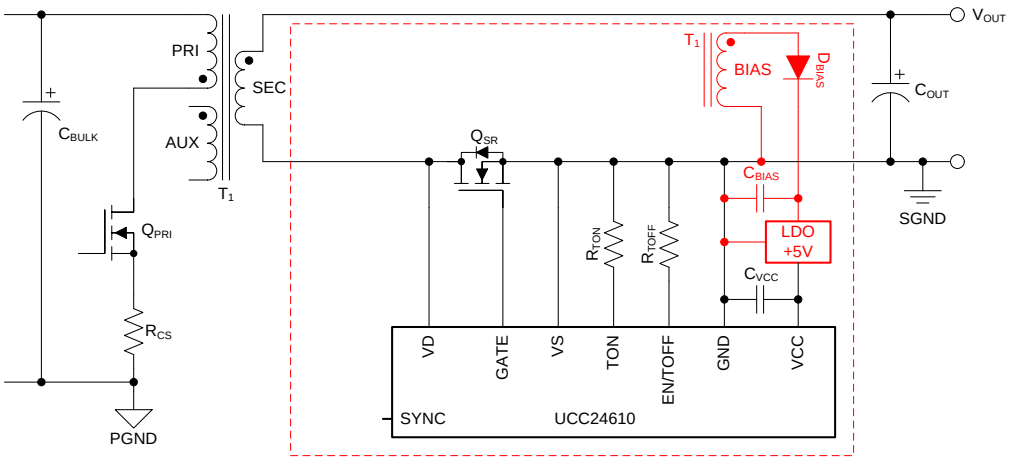

Figure 6. UCC24610 in Low-Side SR with Bias Winding

UCC24612 in Low-Side SR with Bias Winding in Low Output Voltages for Charging and USB Applications:

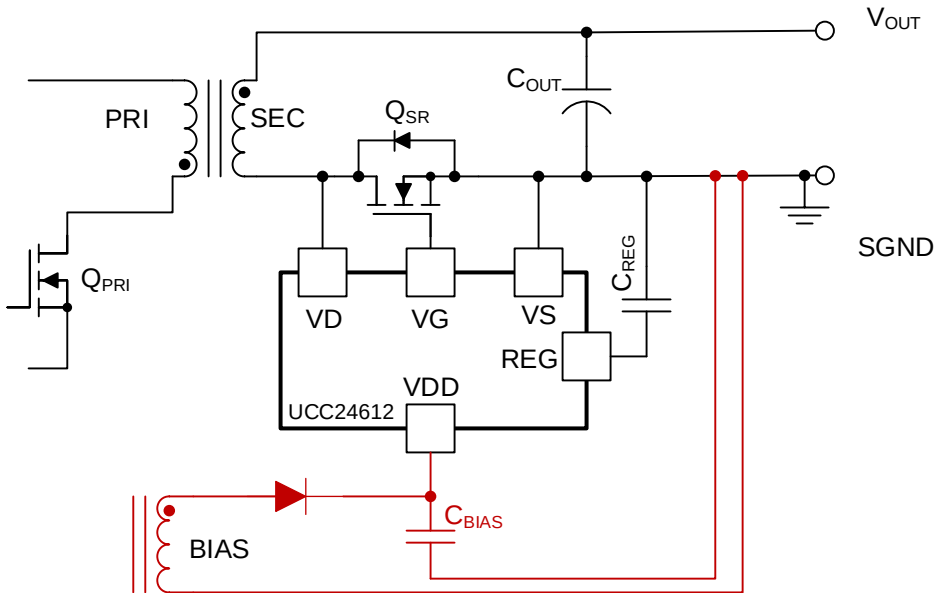

Figure 7. UCC24612 In Low-Side SR for Low Voltage Output for USB and Charging Applications

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9 UCC24610/12 in High-Side SR with Bias Winding

UCC24610 in High-Side SR with Bias Winding:

Like the configuration discussed in Section 8, this method uses a bias winding reduces the VCC bias loss by using a winding to generate a lower voltage for the LDO.

This method can also be used to generate bias voltage when the output voltage is below the minimum input voltage of the devices.

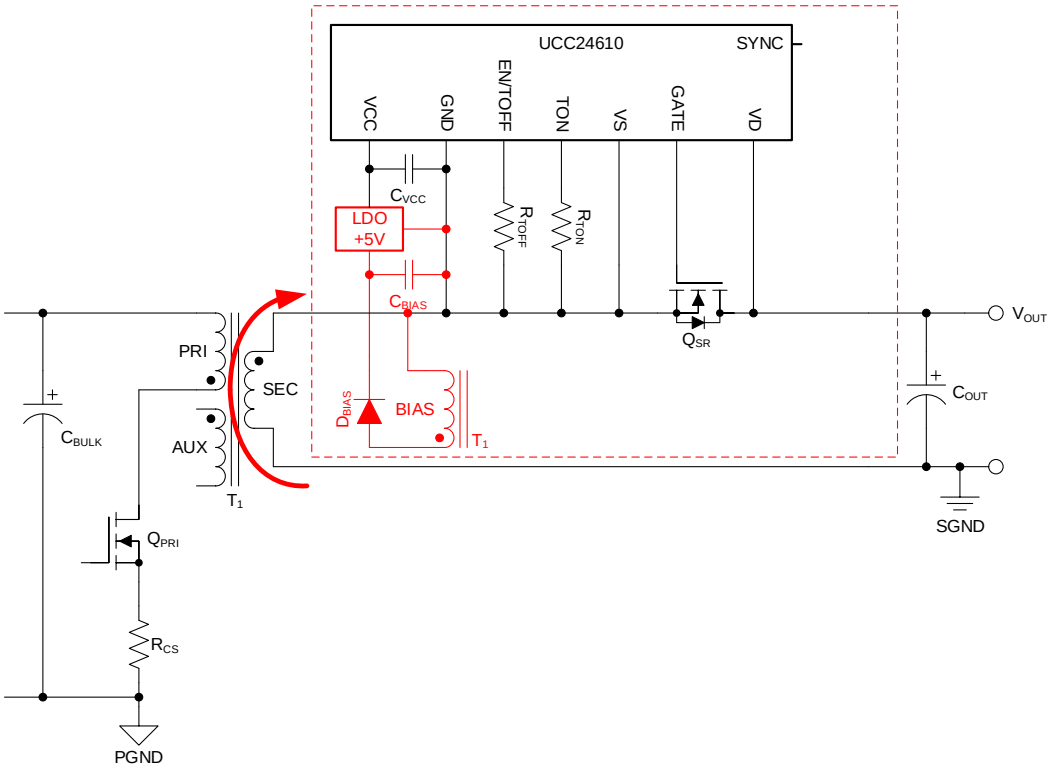

Figure 8. UCC24610 in High-Side SR with Bias Winding

UCC24612 in High-Side SR with Bias Winding:

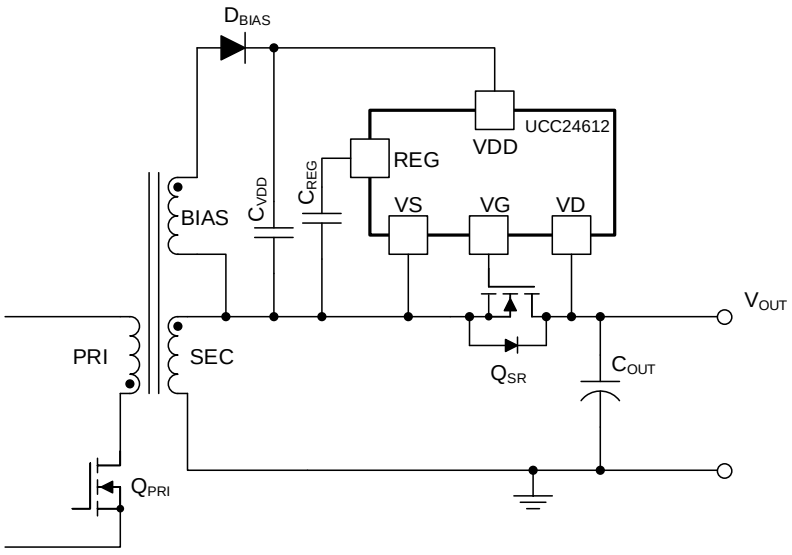

Figure 9. UCC24612 in High-Side SR with Bias Winding

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10 VD Extension Explained

The next configurations are for the UCC24610 in situations where the peak VD voltage V_{VD} > 50Vpk. In these configurations R_{VS} must be added to cancel the $R_{DS(on)}$ rating of Q_{VD} MOSFET and a clamping diode is used to clamp V_{VD} to V_{OUT}. This is explained in more detail in section 8.2.2.1 in the UCC24610 datasheet.

Extending the drain sense pin voltage range is done by adding a voltage clamping circuit. When Q_{SR} in Figure 10 is turned on, Q_{VD} is also turned on. Q_{VD} turns on because the VD and VS pins have a parasitic diode inside the IC. When Q_{SR} is on, VD voltage is the VS voltage minus the forward drop on the parasitic diode. This means that the Q_{VD} gate to source voltage is above the threshold, turning on the device. When Q_{SR} is turned off, the source and drain voltage on Q_{VD} rise together. Therefore, when the source of Q_{VD} reaches a voltage such that $V_{GS} < V_{th}$ of the MOSFET, it will be turned off. This circuit ensures that the VD pin of the UCC24610 device will not see a voltage higher than $V_{OUT} – V_{th}$. However, since the maximum rated voltage of the VD on the UCC24610 is 50 V, there are limitations even with the clamping circuit.

The UCC24612 has a much larger maximum voltage on the VD pin: 230 V. For the same applications, the UCC24612 will not require any additional clamping circuitry, but may need an additional voltage regulator to receive the right biasing voltage.

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11 UCC24610/12 in Low-Side SR with Extended VD Voltage

The following implementation is the modified TI low-side SR configuration for extended VD, and restricts the output voltage to 6.5 V < V_{OUT} < 20 V. The $V_{GS(max)}$ rating of Q_{VD} generally limits this configuration to V_{OUT} < +20 V.

UCC24610 in Low-Side SR with Extended VD Voltage:

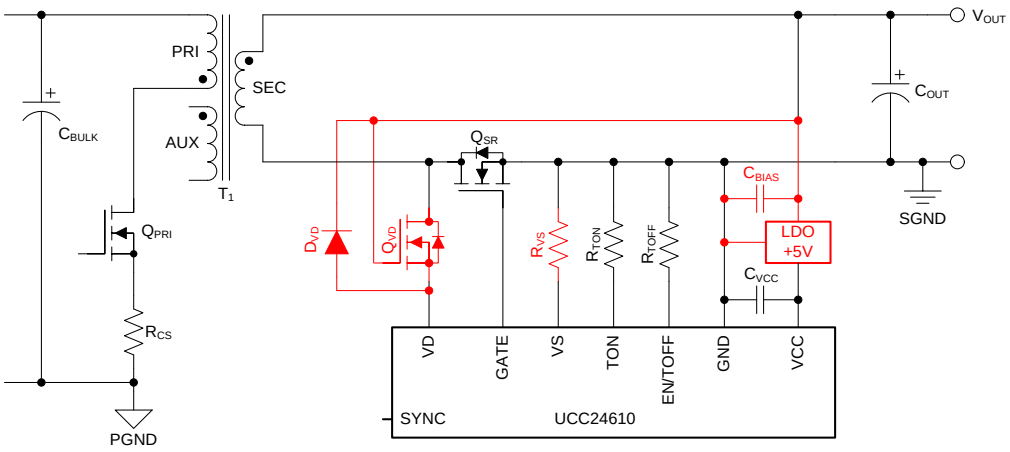

Figure 10. UCC24610 in Low-Side SR with Extended VD Voltage

UCC24612 in Low-Side SR with High Output Voltage:

The UCC24612 VD pin has a maximum voltage rating of 230 V, compared to the 50 V of the UCC24610. Therefore, the output voltage can range much higher than the UCC24610 without having to use a voltage clamping circuit.

In situations where the output voltage is far greater than the VDD range of the UCC24612, maximum 28 V, similar techniques discussed earlier to extend the VDD range of the UCC24610 can be applied here as well.

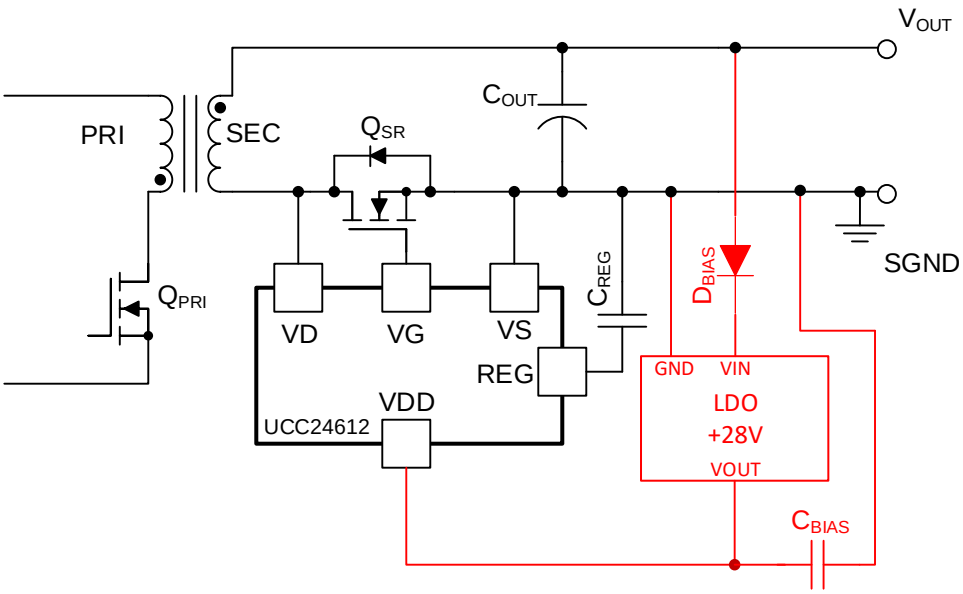

Figure 11. UCC24612 in Low-Side SR with High Output Voltage

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12 UCC24610 in Low-Side SR with Bias Winding with Extended VD Voltage

The bias winding in this configuration keeps the LDO input and Q_{VD} gate voltage at reasonable levels and minimizes losses. The $V_{GS(max)}$ rating of Q_{VD} generally limits this configuration to V_{OUT} < +20V.

UCC24610 in Low-Side SR with Bias Winding with Extended VD Voltage:

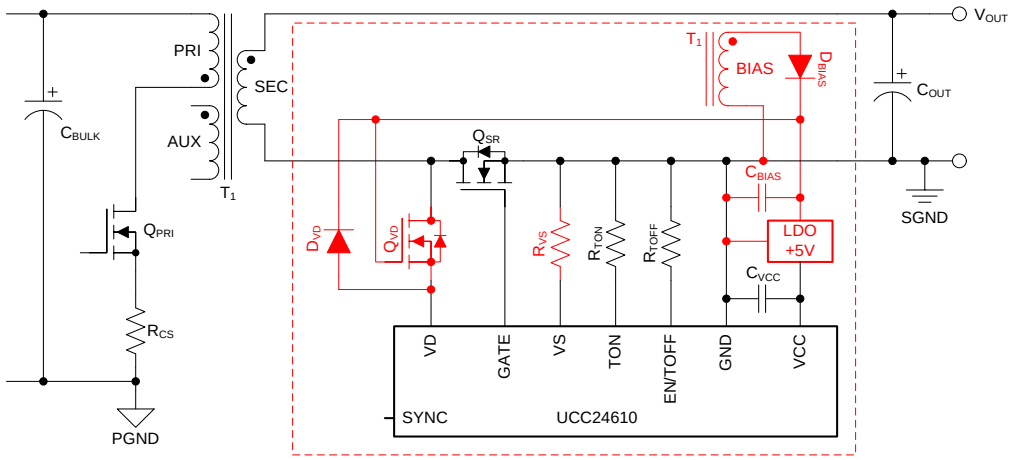

Figure 12. UCC24610 in Low-Side SR with Bias Winding and Extended VD Voltage

13 UCC24610 in High-Side SR with Bias Winding with Extended VD Voltage

The bias winding in this configuration keeps the LDO input and Q_{VD} gate voltage at reasonable levels and minimizes losses. The $V_{GS(max)}$ rating of Q_{VD} generally limits this configuration to V_{OUT} < +20V.

UCC24610 in High-Side SR with Bias Winding with Extended VD Voltage:

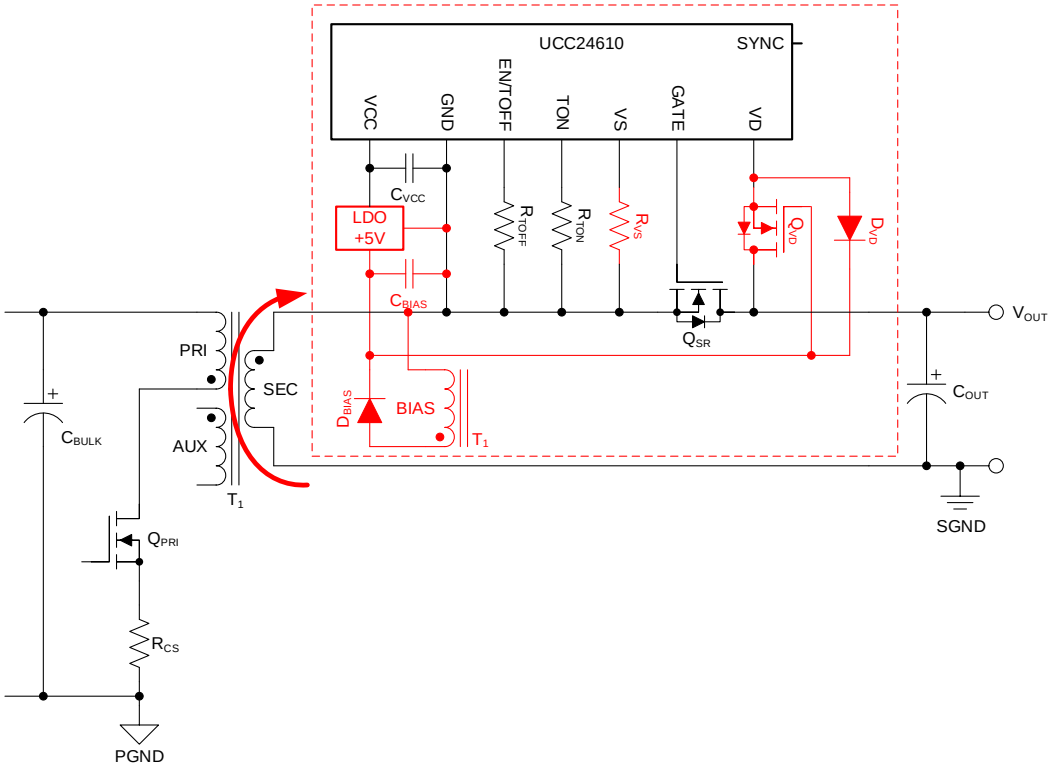

Figure 13. UCC24610 in High-Side SR with Bias Winding and Extended VD Voltage

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