Application Report
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Analyzing Power Dissipation and Circuit Design for the bq241xx (bqSWITCHER™) Synchronous Switching Battery Charger

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ABSTRACT

The bqSWITCHER™ (bq24100/03/05/08/13/15) is a highly integrated, switch-mode, Li-ion and Li-polymer battery charger IC. With two power MOSFETs, the gate drivers, and the controller fully integrated in the chip, the circuit design as well as the PCB layout has been appreciably simplified. However, it is still important to have a good understanding of the charger circuit design, layout principles, and issues and to have the capability to calculate the circuit parameters and power losses for better thermal design. This application report presents the fundamentals of synchronous switching, buck-based battery charger circuit, the loss calculation, and the PCB layout design guideline. A design example is given to demonstrate the entire process of a charger design based on the bqSWITCHER.

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1 Power Stage Design Based on the bqSWITCHER

1.1 Fundamentals of a Buck Converter

The buck converter is used in battery charger applications where linear chargers cannot be used due to their high power dissipation for higher capacity battery packs, or high input-output voltage difference applications. As a means of reducing the dc voltage and achieving voltage and current regulations, a buck converter uses only non-dissipative components, such as switches, inductors, and capacitors. Its basic topology is shown in Figure 1. The two switches alternate to produce a rectangular waveform whose duty ratio D ($0 \le D \le 1$) is the fraction of time that the switch Q1 is on.

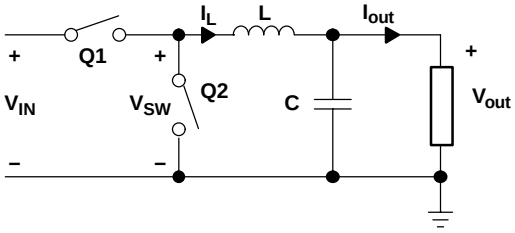

Figure 1. Circuit Diagram of a Synchronous Buck Converter

Figure 2 shows the equivalent circuits when Q1 is on and off. In steady state, it requires that the net change in inductor current over one switching period be zero. From Faraday's Law, it leads to the principle of inductor volt-second balance: the net volt-seconds applied to an inductor over one switching cycle must be zero. As demonstrated visually in Figure 3, the two shaded areas which present the volt-second products at on-time and off-time equal each other, or

$$\left(V_{IN} - V_{OUT}\right) \times D \times T_S = V_{OUT}(1 - D) \times T_S \quad (1)$$

Solution for the voltage gain yields,

$$\frac{V_{OUT}}{V_{IN}} = D \quad (2)$$

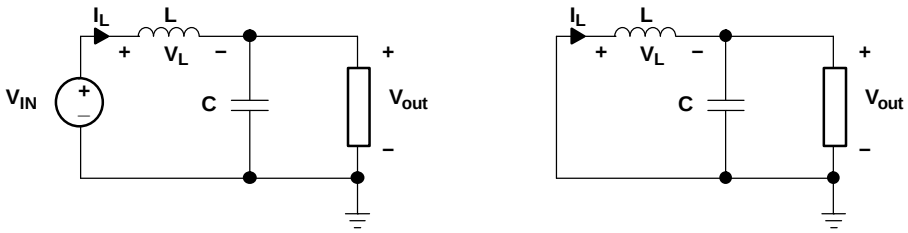

Figure 2. The Equivalent Circuits When (a) Q1 Is On and (b) Q1 Is Off

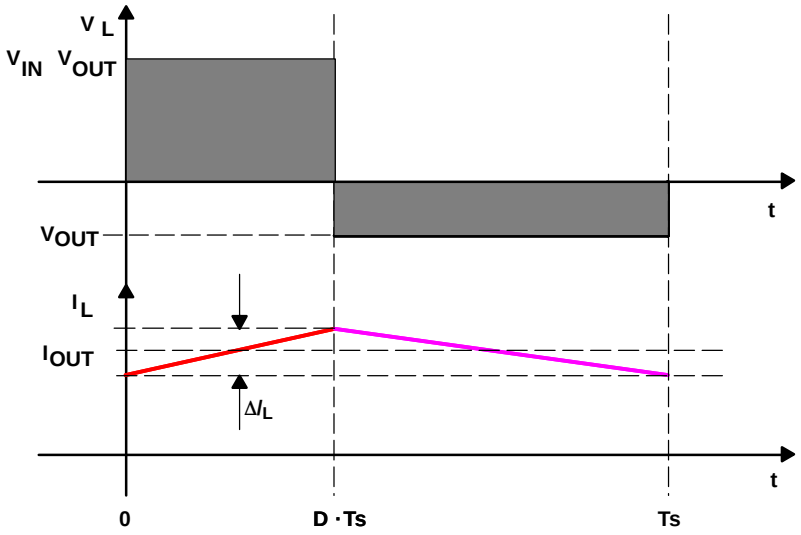

Figure 3. Principle of Volt-Seconds Balance

1.2 Power Stage Design and Component Selection

Given the defining relation of an inductor during Q1 on-period:

$$V_{IN} - V_{OUT} = L\frac{\Delta I_L}{D \times T_S} = L\frac{\Delta I_L}{D \times \frac{1}{f_S}} \quad (3)$$

The inductance can be obtained by

$$L = \frac{V - V_{OUT}}{\Delta I_L}\frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_S} \quad (4)$$

ΔI_L can be empirically determined as about 30% of the fast-charge current.

$$I_{Lpk} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

To select the inductor, follow these tips:

1. Pick the right inductance based on Equation 4
2. Make sure the peak current I_{Lpk} is lower than the inductor saturation current I_{SAT}. Normally I_{SAT} = (1.1~1.5) × I_{Lpk}. I_{Lpk} must be the worst-case peak current.
3. Pick the right RMS current value (normally from thermal point of view).
4. A shielded inductor is preferred due to EMI considerations.
5. Low DCR and core loss are preferred.
6. Low profile and compact size (SMT inductor preferred).
7. Cost

The determination of the output capacitance must meet the requirement of the built-in compensator of the bqSWITCHER. The best stability occurs when the LC resonant frequency f_o is about 16 kHz. Therefore,

$$f_o = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \Rightarrow C = \frac{1}{\left(2 \times \pi \times f_o\right)^2 L} \quad (6)$$

2 Loss Calculations

Estimation of losses is critical in power electronic circuit design. It is not only an issue of efficiency, but also one of thermal management and reliability. Awareness of the losses on each component will also help the designer to better layout the PCB, e.g., selecting PCBs with the right copper thickness and number of layers, determining the size of the circuit, determining the placement of the components, etc.

2.1 Losses of the MOSFETs

Power dissipations in the MOSFETs depend on their on-resistances, gate charge factors, and current and voltage rise and fall times, as well as the switching frequency. Losses on the MOSFETs consist of: conduction losses, switching losses, body diode conduction losses, and gate drive losses. The waveforms associated with the MOSFETs are shown in Figure 4.

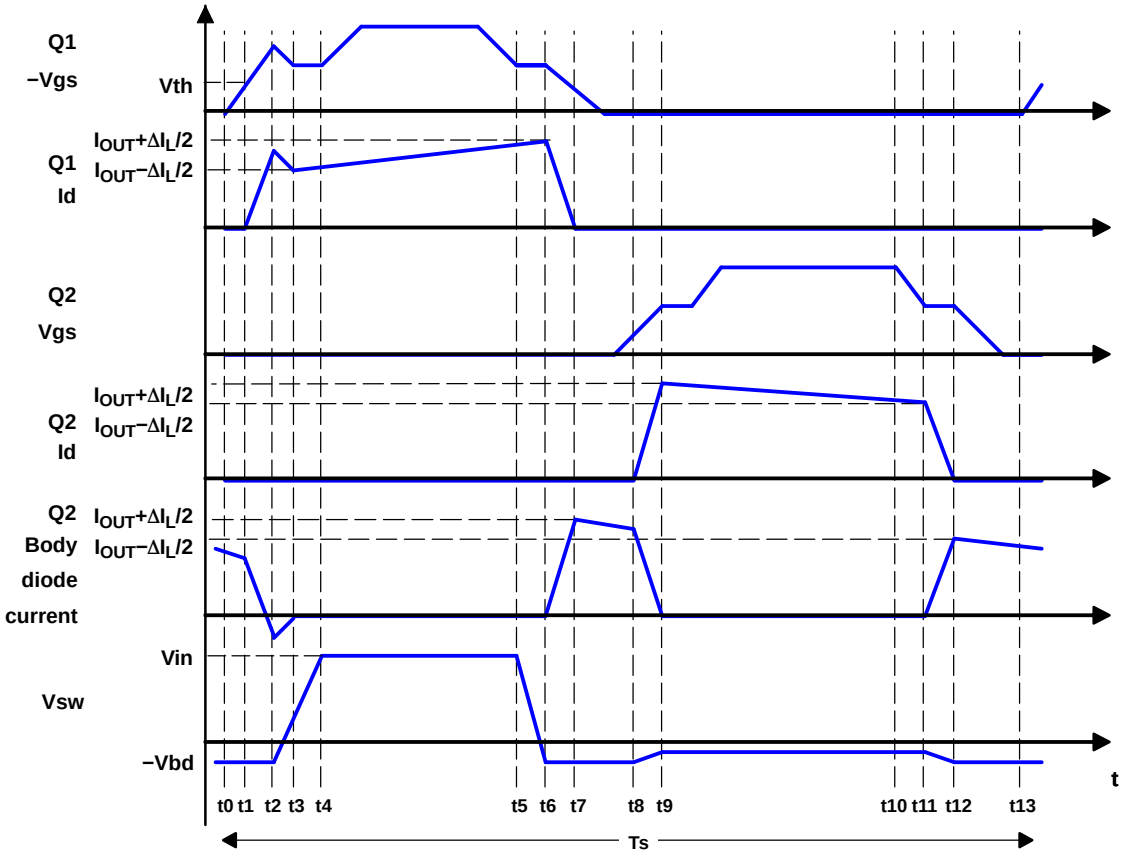

Figure 4. Key Waveforms of Synchronous Buck MOSFETs (not to scale)

2.1.1 Conduction Losses

Based on the switching waveforms in Figure 4, to simplify the conduction loss calculation, assume that the switching time is negligible compared with the switching period. The RMS current of the upper switch Q_1 can be estimated by

$$I_{RMS\_Q1} = \sqrt{\frac{1}{T_S}\int_0^{D \times T_S}\left[\left(I_{OUT} - \frac{\Delta I_L}{2}\right) + \frac{\Delta I_L}{D \times T_S} \times t\right]^2 dt} = \sqrt{D\left(I_{OUT}^2 + \frac{1}{12}\Delta I_L^2\right)} \quad (7)$$

In this calculation, an ideal switch with instant switching capability has been assumed.

The conduction losses of the upper switch Q_1 is given by

$$P_{COND\_Q1} = I^2_{RMS\_Q1} \times R_{DSON\_Q1} \quad (8)$$

The RMS current of the lower switch Q_2 can be estimated by

$$I_{RMS\_Q2} = \sqrt{\frac{1}{T_S}\int_0^{(1-D)\times T_S}\left[\left(I_{OUT} + \frac{\Delta I_L}{2}\right) - \frac{\Delta I_L}{D \times T_S} \times t\right]^2 dt} = \sqrt{(1-D)\left(I^2_{OUT} + \frac{1}{12}\Delta I^2_L\right)} \quad (9)$$

The conduction losses of the lower switch Q_2

$$P_{COND\_Q2} = I^2_{RMS\_Q2} \times R_{DSON\_Q2} \quad (10)$$

The on-resistance of a MOSFET is temperature-dependent. It normally can be estimated as:

$$R_{DSON}(T) = R_{DSON\_am} \times (1 + K \times \Delta T) \quad (11)$$

where K is the temperature coefficient ($K \approx 0.0039/°C$) and R_{DSON_am} is the on-resistance under ambient temperature.

2.1.2 Switching Losses

2.1.2.1 Switching Losses – Upper Switch

From Figure 4, the turn-on loss of Q_1 during $t_1 \sim t_2$:

$$P_{swon\_Q1\_I} = 0.5 \times V_{IN} \times \left(I_{OUT} - \frac{\Delta I_L}{2}\right) \times \Delta t_{ISW\_ON1} \times f_S \quad (12)$$

where $\Delta t_{ISW\_ON1} = t_2 - t_1$.

The turn-on losses of Q_1 during $t_2 \sim t_4$.

$$P_{swon\_Q1\_V} = 0.5 \times V_{IN} \times \left(I_{OUT} - \frac{\Delta I_L}{2}\right) \times \Delta t_{VSW\_ON1} \times f_S \quad (13)$$

where $\Delta t_{ISW\_ON1} = t_4 - t_2$. The total turn-on losses:

$$P_{swon\_Q1} = Pswon\_Q1\_I + P_{swon\_Q1\_V} \quad (14)$$

From Figure 4, the turn-off losses of Q_1 during $t_5 \sim t_6$:

$$P_{swoff\_Q1\_V} = 0.5 \times V_{IN} \times \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times \Delta t_{VSW\_OFF1} \times f_S \quad (15)$$

where $\Delta t_{ISW\_ON1} = t_6 - t_5$. The turn-off losses of during Q_1 during $t_6 \sim t_7$:

$$P_{swoff\_Q1\_I} = 0.5 \times V_{IN} \times \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times \Delta t_{ISW\_OFF1} \times f_S \quad (16)$$

where $\Delta t_{ISW\_ON1} = t_7 - t_6$. The total turn-off losses:

$$P_{swoff\_Q1} = Pswoff\_Q1\_V + P_{swoff\_Q1\_I} \quad (17)$$

The total switching losses of Q_1:

$$P_{sw\_Q1} = Pswon\_Q1 + P_{swoff\_Q1} \quad (18)$$

2.1.2.2 Switching Losses – Lower Switch

From Figure 4, during the switching period of Q_2: t_8~t_9 and t_{11}~t_{12}, the Q_2 body diode is on all the time. Therefore, the voltage drop on Q_2 during switching is only the forward conduction voltage of the body diode. This is called zero-voltage switching (ZVS); thus, the switching losses can be neglected.

2.1.2.3 Lower FET Body Diode Reverse Recovery Effect

As the lower FET Q_2 turns off, conduction of output current takes place through the body diode. To turn off the diode and reverse bias across it, charge stored in the body diode has to be evacuated from the junction. This adds to the switching losses of Q_1. The loss can be estimated as:

$$P_{QRR} = Q_{RR} \times V_{IN} \times f_S \tag{19}$$

where Q_{RR} is the reverse recovery charge of the lower MOSFET body diode.

2.1.3 Body Diode Conduction Losses

From Figure 4, before Q_2 turns on and after Q_2 turns off, the body diode of Q_2 conducts for a period called dead-time, t_{DT}. This leads to body diode conduction losses:

$$P_{BD\_Q2} = 2 \times V_{BD} \times I_{OUT} \times t_{DT} \times f_S \tag{20}$$

where V_{BD} is the body diode forward voltage drop.

2.1.4 Gate Drive Losses

The gate capacitor of Q_1 is charged every cycle to an energy level equal to $\frac{1}{2} C_{in\_Q1} \times V^2_{DRV\_Q1}$. The same amount of energy is dissipated internally in the MOSFET gate resistance to provide this charge. The same energy must be discharged once during each cycle. The gate drive power dissipated by Q_1 can therefore be given by

$$P_{DRV\_Q1} = Q_{g\_Q1} \times V_{DRV\_Q1} \times f_S \tag{21}$$

where $Q_{g\_Q1} = Q_{gs\_Q1} + Q_{gd\_Q1}$.

The gate drive power dissipated by Q_2 can therefore be given by

$$P_{DRV\_Q2} = Q_{g\_Q2} \times V_{DRV\_Q2} \times f_S \tag{22}$$

where $Q_{g\_Q2 = Qgs\_Q2}$ (Q_{gd_Q2} = 0 since Q2 operates in zero-voltage switching and Q_{gd_Q2} is recovered).

2.1.5 Thermal Calculations

The temperature rise of the MOSFETs is given by:

$$\Delta T = \left[I^2_{RMS\_Q1} \times R_{DSON\_Q1\_am} \times (1 + K \times \Delta T) + I^2_{RMS\_Q2} \times R_{DSON\_Q2\_am} \times (1 + K \times \Delta T) + P_{MOS\_fixed} \right] \times \theta_{JA} \tag{23}$$

$$\text{where } P_{MOS\_fixed} = P_{sw\_Q1} + P_{QRR} + P_{BD\_Q2} + P_{DRV\_Q1} + P_{DRV\_Q2} \tag{24}$$

Seeking solutions to the equation, one obtains:

$$\Delta T = \frac{I^2_{RMS\_Q1} \times R_{DSON\_Q1\_am} + I^2_{RMS\_Q2} \times R_{DSON\_Q2\_am} + P_{MOS\_fixed}}{\frac{1}{\theta_{JA}} - K \times \left(I^2_{RMS\_Q1} \times R_{DSON\_Q1\_am} + I^2_{RMS\_Q2} \times R_{DSON\_Q2\_am} \right)} \tag{25}$$

After obtaining ΔT, the losses of the MOSFETs need to be re-calculated based on the calculated temperature rise.

2.2 Losses of the Inductor

The inductors losses consist of winding loss and core loss. The total winding loss is a function of frequency and temperature. The core loss depends on the core material. It is also a function of frequency, maximum flux density, as well as the volume. This can be discovered by examining the curves provided by the manufacturers. However, the calculation based on dc resistance (DCR) is adequate for general-purpose estimation.

$$I_{RMS\_L} = \sqrt{\frac{1}{T_S}\int_0^{D\times T_S}\left[\left(I_{OUT}-\frac{\Delta I_L}{2}\right)+\frac{\Delta I_L}{D\times T_S}\times t\right]^2 dt + \int_0^{(1-D)\times T_S}\left[\left(I_{OUT}+\frac{\Delta I_L}{2}\right)-\frac{\Delta I_L}{D\times T_S}\times t\right]^2 dt}$$

$$= \sqrt{D\left(I_{OUT}^2+\frac{1}{12}\Delta I_L^2\right)+(1-D)\left(I_{OUT}^2+\frac{1}{12}\Delta I_{OUT}^2\right)} = \sqrt{\left(I_{OUT}^2+\frac{1}{12}\Delta I_L^2\right)} \quad (26)$$

The winding loss can be estimated as

$$P_{L\_winding} \approx I_{L\_RMS}^2 R_{L\_DCR} \quad (27)$$

The DCR of an inductor is also temperature-dependent. It normally can be estimated as:

$$R_{DSON}(T) = R_{DSON(25°C)} \times (1 + K \times \Delta T) \quad (28)$$

where K is the temperature coefficient and K ≈ 0.0039/°C.

2.3 Losses of the Sense Resistor

$$P_{RSNS} = I_{OUT}^2 R_{SNS} \quad (29)$$

2.4 Losses of the Capacitors

The RMS current flowing through the input capacitor is given by:

$$I_{RMS\_CIN} = \sqrt{\frac{1}{T_S}\left\{\int_0^{D\times T_S}\left[\left(I_{OUT}(1-D)\right]^2 dt + \int_0^{(1-D)\times T_S}\left[\left(I_{OUT}\times D\right]^2 dt\right\}\right.} = I_{OUT}\times\sqrt{D\times(1-D)} \quad (30)$$

The current flowing through the output capacitor can be approximated by the ac component of the inductor current. The RMS current of the output capacitor is given by:

$$I_{RMS\_COUT} = \sqrt{\frac{1}{T_S}\left\{\int_0^{D\times T_S}\left[-\frac{\Delta I_L}{2}+\frac{\Delta I_L}{D\times T_S}\times t\right]^2 dt + \int_0^{(1-D)\times T_S}\left[\frac{\Delta I_L}{2}-\frac{\Delta I_L}{(1-D)\times T_S}\times t\right]^2 dt\right\}} = \frac{\Delta I_L}{2\sqrt{3}} \quad (31)$$

The losses due to the ESR of the input capacitor:

$$P_{CIN\_ESR} = I_{RMS\_CIN}^2 R_{CIN} \quad (32)$$

The losses due to the ESR of the output capacitor:

$$P_{COUT\_ESR} = I_{RMS\_COUT}^2 R_{COUT} \quad (33)$$

2.5 Other Losses

Other factors may also contribute to losses, such as losses on the PCB traces, losses on the control circuit, etc.

3 Design Example

3.1 Specifications

- Adapter Voltage: 12 V
- Battery Packs: 2S (Two Cells in Series) Li-Ion Battery, 1800 mAH
- Battery Voltage: 4.2 V/Cell (V_{BAT_max} = 8.4 V, V_{BAT_min} = 6 V)
- Fast-Charge Current I_{BAT} = 1.2 A
- Precharge and Charge Termination Current: 120 mA
- Safety Timer: 5 hours

The schematic of a typical charger circuit using bq24103 is shown in Figure 5.

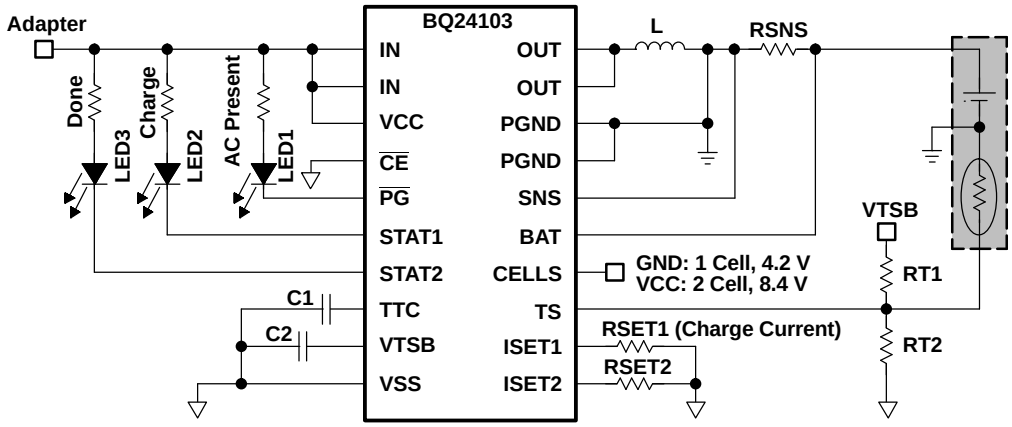

Figure 5. Schematic of the Design Example.

3.2 Determine the Inductor L

Given 30% ripple current, the inductance when $V_{OUT} = V_{BAT\_max}$:

$$L = \frac{V_{IN} - V_{BAT\_max}}{\Delta I_L} \frac{V_{BAT\_max}}{V_{IN}} \times \frac{1}{f_S} = \frac{12 - 8.4}{30\% \times 1.2} \frac{8.4}{12} \times \frac{1}{1.1 \times 10^6} = 6.364\ \mu H \quad (34)$$

The inductance when $V_{OUT} = V_{BAT\_min}$:

$$L = \frac{V_{IN} - V_{BAT\_min}}{\Delta I_L} \frac{V_{BAT\_min}}{V_{IN}} \times \frac{1}{f_S} = \frac{12 - 6}{30\% \times 1.2} \frac{6}{12} \times \frac{1}{1.1 \times 10^6} = 7.576\ \mu H \quad (35)$$

Select L = 10 µH,

$$\Delta I_{L\_MAX} = \frac{V_{IN} - V_{BAT\_max}}{L} \frac{V_{BAT\_max}}{V_{IN}} \times \frac{1}{f_S} = \frac{12 - 8.4}{10 \times 10^{-6}} \frac{8.4}{12} \times \frac{1}{1.1 \times 10^6} = 0.229\ A \quad (36)$$

$$I_{Lpk} = I_{OUT} + \frac{\Delta I_{L\_MAX}}{2} = 1.2 + \frac{0.229}{2} = 1.315\ A \quad (37)$$

Select Sumida CDRH74-100 inductor (10 µH, SMT, 1.84 A, 49 mΩ)

3.3 Determine the Output Capacitor C

$$C = \frac{\left(2 \times \pi \times f_O\right)^2}{L} = \frac{1}{(2 \times \pi \times 16 \times 10^3)^2 \times 10 \times 10^{-6}} = 9.895 \times 10^{-6}(F) \quad (38)$$

Select 10 µF, 25 V X5R SMT with 1206 size ceramic capacitor.

3.4 Determine the Sense Resistor R_{SNS}

Better Charge Current Accuracy: ±10%

V_{RSNS}: 100 mV to 200 mV

In order to get a standard resistance value, select V_{RSNS} = 120 mV

$$R_{SNS} = \frac{V_{RSNS}}{I_{BAT}} = \frac{120\ mV}{1.20\ A} = 0.1\ \Omega$$

$$R_{RSNS} = I_{BAT}^2 R_{SNS} = 144\ mW \quad (39)$$

Select 100 mΩ/0.25 W with 0806 or 1206 size High Precision Sensing Resistor

3.5 Determine the R_{SET1} and R_{SET2}

I_{FAST_CHARGE} = 1.2A, I_{PRE_CHARGE} = $I_{TERMINATION}$ = 120 mA, V_{ISET1} = 1.0 V, V_{ISET2} = 0.1 V, K_{SET1} = K_{SET2} = 1000V/A R_{SNS} = 0.1 Ω

$$R_{SET1} = \frac{V_{ISET1} \times K_{SET1}}{I_{FAST-CHARGE} \times R_{SNS}} = 8.33\ k\Omega \quad (40)$$

$$R_{SET2} = \frac{V_{ISET2} \times K_{SET2}}{I_{PRE-CHARGE} \times R_{SNS}} = 8.33\ k\Omega \quad (41)$$

Select 1%, 8.33 kΩ resistors.

3.6 Determine C_1

For 1800 mAH Li-Ion Cell, set TSAFETY TIMER = 5 hours

$$C_1 = \frac{300\ min}{2.6\ min/nF} = 0.115\ \mu F \quad (42)$$

Select 0.12 µF or 0.1 µF/X5R or X7R Ceramic Capacitor for Good Temperature performance.

3.7 Determine R_{T1} and R_{T2}

The equivalent circuit of the temperature sensing circuit is shown in Figure 6, in which R_{TS} is the resistance of the thermistor.

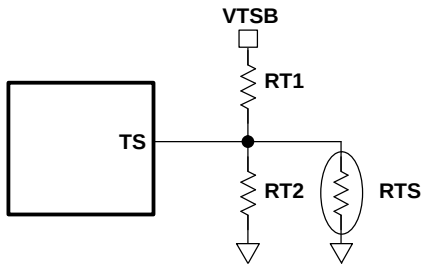

Figure 6. The Equivalent Circuit of the Temperature Sensing Circuit

R_{TS}, a function of temperature, normally drops with temperature. Assuming the use of a 103AT-2 thermistor, the resistance at cold temperature and hot temperature are R_{TS_COLD} = 27306 Ω and R_{TS_HOT} = 4935 Ω, respectively.

The voltage threshold at cold temperature is V_{LTF} = 73.5% x VTSB. The voltage threshold at hot temperature is V_{HTF} = 34.4% x VTSB. Therefore, it can be obtained that

$$\frac{R_{T2} \,//\, R_{TS\_COLD}}{R_{T1} + R_{T2} \,//\, R_{TS\_COLD}} = 73.5\% \tag{43}$$

$$\frac{R_{T2} \,//\, R_{TS\_HOT}}{R_{T1} + R_{T2} \,//\, R_{TS\_HOT}} = 34.4\% \tag{44}$$

Solving Equation 43 and Equation 44, one obtains: R_{T1} = 9.31 kΩ, R_{T2} = 475 kΩ.

3.8 Losses Calculation

The data of the circuit:

Q_1: R_{DSON_Q1} = 227 mΩ at 25°C, V_{DRV_Q1} = 6 V (if V_{IN} > 7 V) or V_{IN}– 1 V (if V_{IN} < 7 V), Q_{g_Q1} = 6.722 nC, Δt_{ISW_ON1} = 2.042 ns, Δt_{VSW_ON1} = 7.49 ns, $\Delta t_{ISW\_OFF1} = \Delta t_{ISW\_ON1}$, $\Delta t_{VSW\_OFF1} = \Delta t_{VSW\_ON1}$.

Q_2: R_{DSON_Q2} = 61 mΩ at 25°C, $V_{DRV\_Q2} = V_{DRV\_Q1}$, Q_{g_Q2} = 6.979 nC, Q_{RR} = 0.02 nC, V_{BD} = 0.7 V, t_{DT} = 25 ns

L: R_{L_DCR} = 49 mΩ

C_{IN}: R_{CIN} = 8 mΩ.

C_{OUT}: R_{COUT} = 8 mΩ

The losses calculation examples below assume an output voltage 8.4 V.

3.8.1 Losses on the MOSFETs

The RMS current of the upper switch Q_1 can be estimated by

$$I_{RMS\_Q1} = \sqrt{D\left(I_{OUT}^2 + \frac{1}{12}\Delta I_L^2\right)} = \sqrt{\frac{8.4}{12}\left(1.2^2 + \frac{1}{12} \times 0.386^2\right)} = 1.006 \text{ A} \tag{45}$$

The RMS current of the lower switch Q_2 can be estimated by

$$I_{RMS\_Q2} = \sqrt{(1 - D)\left(I_{OUT}^2 + \frac{1}{12}\Delta I_L^2\right)} = 0.658 \text{ A} \tag{46}$$

The upper switch switching losses

$$P_{swon\_Q1} = 0.5 \times V_{IN} \times \left(I_{OUT} - \frac{\Delta I_L}{2}\right) \times \left(\Delta t_{ISW\_ON1} + \Delta t_{VSW\_ON1}\right) \times f_S = 0.068 \text{ W} \tag{47}$$

$$P_{swoff\_Q1} = 0.5 \times V_{IN} \times \left(I_{OUT} - \frac{\Delta I_L}{2}\right) \times \left(\Delta t_{VSW\_OFF1} + \Delta t_{ISW\_OFF1}\right) \times f_S = 0.083 \text{ W} \tag{48}$$

The total switching losses of Q_1:

$$P_{sw\_Q1} = P_{swon\_Q1} + P_{swoff\_Q1} = 0.151 \text{ W} \tag{49}$$

The switching losses due to lower FET body diode reverse recovery effect

$$P_{QRR} = Q_{RR} \times V_{IN} \times f_S = 2.64 \times 10^{-4} \text{ W} \tag{50}$$

The body diode conduction losses:

$$P_{BD\_Q2} = 2 \times V_{BD} \times I_{OUT} \times t_{DT} \times f_S = 0.046\ W \quad (51)$$

The gate drive losses of Q_1:

$$P_{DRV\_Q1} = Q_{g\_Q1} \times V_{DRV\_Q1} \times f_S = 0.044\ W \quad (52)$$

The gate drive losses of Q_2:

$$P_{DRV\_Q2} = Q_{g\_Q2} \times V_{DRV\_Q2} \times f_S = 0.046\ W \quad (53)$$

The fixed losses on the MOSFETs

$$P_{MOS\_fixed} = P_{sw\_Q1} + P_{QRR} + P_{BD\_Q2} + P_{DRV\_Q1} + P_{DRV\_Q2} = 0.288\ W \quad (54)$$

The temperature rise (assuming T_{am} = 25°C):

$$\Delta T = \frac{I^2_{RMS\_Q1} \times R_{DSON\_Q1\_am} + I^2_{RMS\_Q2} \times R_{DSON\_Q2\_am} + P_{MOS\_fixed}}{\frac{1}{\theta_{JA}} - K \times \left(I^2_{RMS\_Q1} \times R_{DSON\_Q1\_am} + I^2_{RMS\_Q2} \times R_{DSON\_Q2\_am}\right)} = 26.74°C \quad (55)$$

The on-resistance of Q_1

$$R_{DSON\_Q1} = R_{DSON\_Q1\_am} \times (1 + K \times \Delta T) = 251\ m\Omega \quad (56)$$

The on-resistance of Q_2

$$R_{DSON\_Q2} = R_{DSON\_Q2\_am} \times (1 + K \times \Delta T) = 67\ m\Omega \quad (57)$$

The conduction losses of the upper switch Q_1

$$R_{COND\_Q1} = I^2_{RMS\_Q1} \times R_{DSON\_Q1} = 0.253\ W \quad (58)$$

The conduction losses of the lower switch Q_2

$$R_{COND\_Q2} = I^2_{RMS\_Q2} \times R_{DSON\_Q2} = 0.029\ W \quad (59)$$

The total losses of the MOSFETs:

$$P_{FETs} = P_{COND\_Q1} + P_{COND\_Q2} + P_{MOS\_fixed} = 0.570\ W \quad (60)$$

3.8.2 Losses on the Inductor

The inductor RMS current

$$I_{L\_RMS} = \sqrt{I^2_{OUT} + \frac{1}{12}\Delta I^2_L} = 1.202\ A \quad (61)$$

The winding loss can be estimated as

$$P_{L\_winding} \approx I^2_{L\_RMS} R_{L\_DCR} = 0.071\ W \quad (62)$$

3.8.3 Losses on the Sense Resistor

$$P_{RSNS} = I^2_{OUT} R_{SNS} = 0.144\ W \quad (63)$$

3.8.4 Losses on Capacitors

The RMS current flowing through the input capacitor is given by:

$$I_{RMS\_CIN} = I_{OUT} \times \sqrt{D \times (1 - D)} = 0.55\ A \tag{64}$$

The RMS current of the output capacitor is given by:

$$I_{RMS\_COUT} = \frac{\Delta I_L}{2\sqrt{3}} = 0.066\ A \tag{65}$$

The losses on the ESR of the input capacitor:

$$P_{CIN\_ESR} = I^2_{RMS\_CIN} R_{CIN} = 2.419\ mW \tag{66}$$

The losses on the ESR of the output capacitor:

$$P_{COUT\_ESR} = I^2_{RMS\_COUT} R_{COUT} = 0.035\ mW \tag{67}$$

The total capacitor ESR losses:

$$P_{C\_ESR} = P_{CIN\_ESR} + P_{COUT\_ESR} = 2.45\ mW \tag{68}$$

3.8.5 Calculation Results

The total losses of the charger with V_{BAT} = 8.4 V, I_{chrg} = 1.2 A are given by:

$$P_{total} = P_{FETs} + P_{L\_winding} + P_{RSNS} + P_{C\_ESR} = 0.788\ W \tag{69}$$

The calculation results and the measurement results of the charger efficiency vs output current when V_{IN} = 12 V are shown in Figure 7 (a) and (b), respectively. The calculation results correlate with the measurement results well.

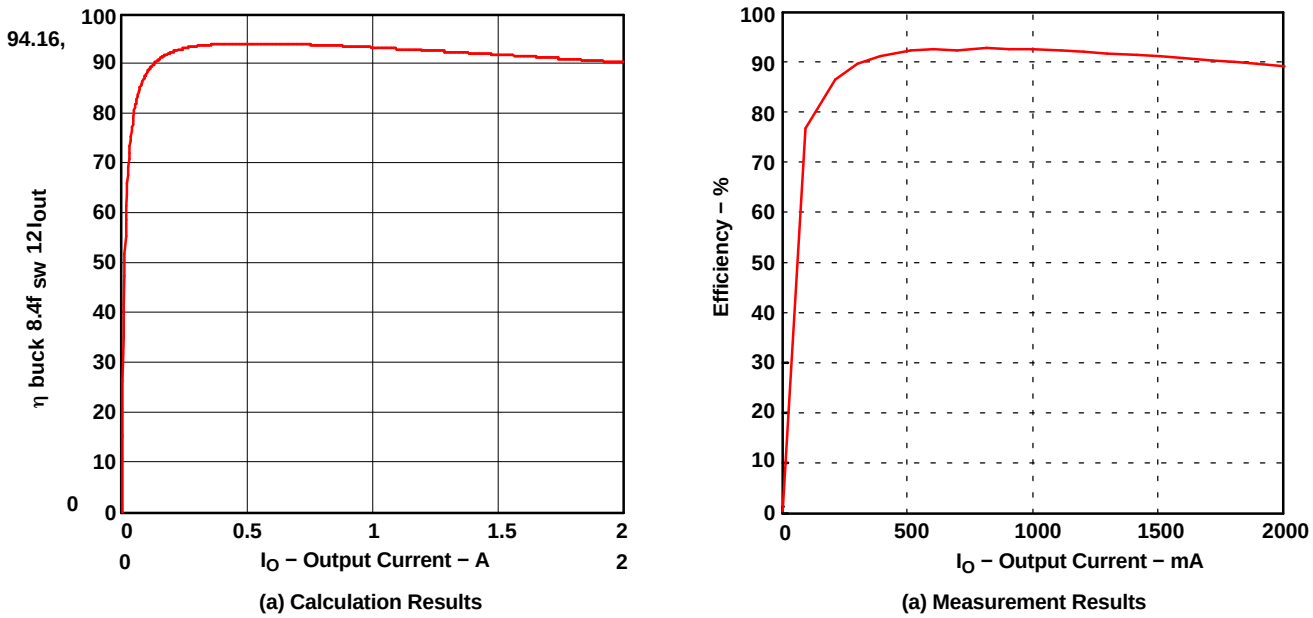

Figure 7. Efficiency vs I_{out} (V_{IN} = 12 V, V_{BAT} = 8.4 V)

3.9 Losses Breakdown Under Different Conditions

3.9.1 V_{IN} = 12 V, V_{BAT} = 8.4 V, I_{chrg} = 1.2 A

ITEM	SYMBOL	T_{am} = 25°C	T_{am} = 55°C
Losses of the MOSFETs	P_{COND}	0.282 W	0.318 W
	P_{sw_Q1}	0.151 W	0.151 W
	P_{QRR}	0.264 mW	0.264 mW
	P_{BD_Q2}	0.046 W	0.046 W
	P_{DRV}	0.090 W	0.090 W
	P_{FETs}	0.570 W	0.605 W
Losses of the inductor	$P_{L\_winding}$	0.071 W	0.071 W
Losses of the sense resistor	P_{RSNS}	0.144 W	0.144 W
Losses of the capacitors	P_{C_ESR}	2.45 mW	2.45 mW
Total Losses	P_{total}	0.788 W	0.822 W
Efficiency	η	92.75%	92.46%
IC temperature rise	ΔT	26.7°C	28.2°C
IC Junction Temperature	T_J	51.7°C	83.2°C

3.9.2 V_{IN} = 9 V, V_{BAT} = 8.4 V, I_{chrg} = 1.2 A

ITEM	SYMBOL	T_{am} = 25°C	T_{am} = 55°C
Losses of the MOSFETs	P_{COND}	0.344 W	0.387 W
	P_{sw_Q1}	0.113 W	0.113 W
	P_{QRR}	0.20 mW	0.20 mW
	P_{BD_Q2}	0.046 W	0.046 W
	P_{DRV}	0.090 W	0.090 W
	P_{FETs}	0.595 W	0.638 W
Losses of the inductor	$P_{L\_winding}$	0.071 W	0.071 W
Losses of the sense resistor	P_{RSNS}	0.144 W	0.144 W
Losses of the capacitors	P_{C_ESR}	0.72 mW	0.72 mW
Total Losses	P_{total}	0.810 W	0.853 W
Efficiency	η	92.56%	92.20%
IC temperature rise	ΔT	27.9°C	29.7°C
IC Junction Temperature	T_J	52.9°C	84.7°C

From the losses breakdown in the two preceding tables, it can be seen that:

1. The dominant losses of the MOSFETs are the conduction losses.
2. The lower the ambient temperature, the lower the conduction losses.
3. A lower input voltage normally leads to lower losses.
4. The junction temperature for single-cell applications is much lower than that of two-cell applications. For a 55°C ambient temperature, the IC junction temperature could reach as high as 90°C.

4 PCB Layout Considerations

The mechanical construction of the circuit is just as important as the calculation of the component values for the switching battery chargers. When designing the layout of the printed-circuit board for the charger, care must be taken that the high-frequency switching does not generate interference, either in the circuit or in the outside environment. At the same time, compact size and good thermal performance are also good layout design goals .

4.1 Make the Connections of the Power Stage as Wide and Short as Possible

The reasons for doing so are:

1. The metallization which conducts the high-frequency, high-power switching signals on the circuit board should be kept as short as possible, so that interference emitted to the outside or coupled into the circuit can be minimized.
2. When a fast-changing current is present, even low values of inductance in the connections can result in considerable voltage drops. This also reduces the inductance of the connections.
3. Making the connections short and wide reduces the PCB copper resistance, thus reducing the power losses and helping to improve the thermal performance. For example, a 10 cm long, 1 mm wide 1-oz PCB trace carrying 2 A dissipates about 0.2 W of power losses.

The major connection loops that need to be minimized are shown in Figure 8.

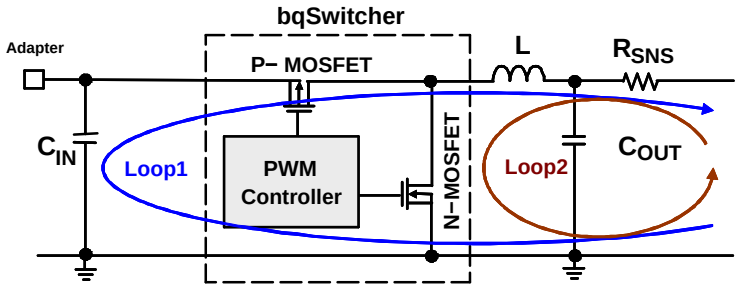

Figure 8. Loops That Need to be Minimized

4.2 Star Ground

The ground planes of the power stage and of the control stage should be run separately, so that high currents in the main circuit cannot influence the regulating circuitry. However, both ground planes must be connected together at a single point, so that different potentials for the two grounds cannot occur. This single point should be located at the power pad of the IC, for the case of bqSWITCHER, as shown in Figure 9. The areas that are not used for other connections should be filled with ground plane. Multiple vias are necessary to drill on the IC power pad area. On one hand, they connect the ground planes on all the layers to the power pad of the IC. On the other hand, it helps distribute the heat.

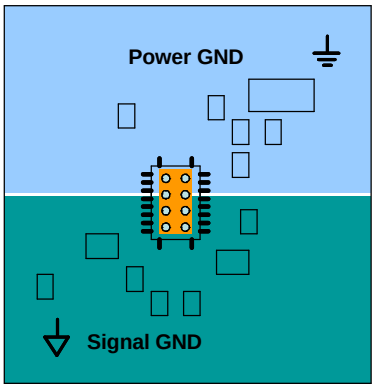

Figure 9. Star Ground of bqSWITCHER Charger Layout

4.3 Decoupling Capacitors Close to the Decoupling Target

A decoupling capacitor of about 0.1 µF – 1 µF should be connected between the V_{IN} pins and ground, which is able to carry the necessary current when switching occurs and to minimize the ringing on the switching devices. Decoupling capacitors are also needed at the SNS pin and the VTSB pin as well as the BAT output. It is important to keep the wiring short, and to locate the capacitor as close as possible to the pin or the decoupling target. For example, the decoupling capacitor for V_{IN} pin can be placed on the bottom layer with one terminal on the power pad area in order to minimize the decoupling loop, as illustrated in Figure 10.

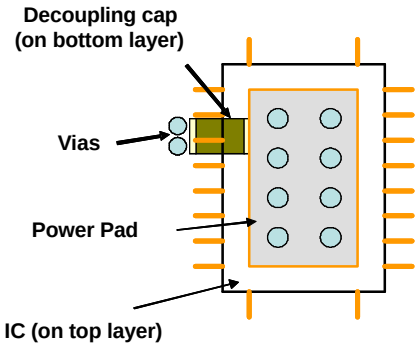

Figure 10. Placement of the Decoupling Capacitors for V_{IN} Pin

4.4 Minimization of the Feedback Loop

The voltage and current feedback loop design is one of the key issues in the bqSWITCHER charger layout. The current sensing feedback signals are normally in the 100-mV to ~200-mV range, therefore very sensitive to the external noise perturbations. To enhance the noise immunity of the current sensing feedback, a Kelvin connection located at the terminals of the sense resistor is required and the entire feedback loop area needs to be minimized, as shown in Figure 11. Considering the voltage-sensing trace is part of the current-sensing loop for some of the variations of the bqSWITCHER, the sense resistor should be placed close to the battery so that a better voltage feedback can be achieved. Both the voltage and current feedback paths must be routed far from the switching node (connected to the OUT pin) of the power stage.

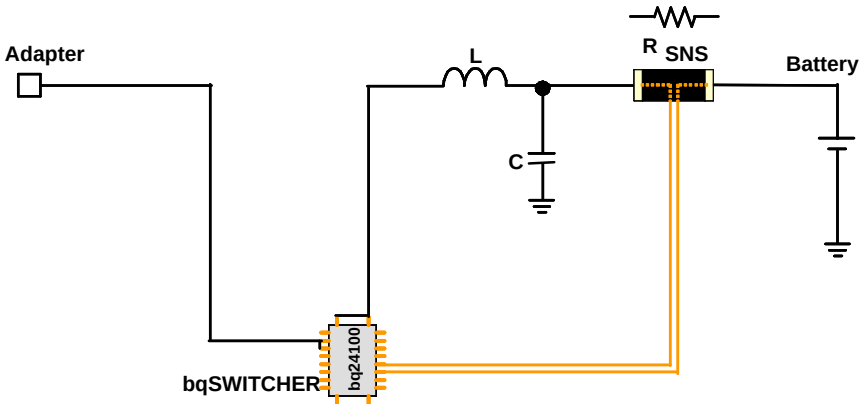

Figure 11. Current Feedback Loop Layout

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