Application Report
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Optimizing MOSFET Characteristics by Adjusting Gate Drive Amplitude

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ABSTRACT

Most publications related to power supply gate drive highlight switching properties of the MOSFET and various methods that can be used to turn the devices on and off as efficiently as possible. One aspect often overlooked is the issue of gate drive voltage amplitude and the role it can play in overall power converter efficiency. The operating characteristics of a MOSFET change according to the amplitude of the gate drive pulse. As a result, trade-offs exist when considering one gate drive voltage level versus another. Although these principles can apply to most switching power supply topologies, a synchronous buck is used as an application example. Graphs showing frequency and load current trade-offs present general MOSFET power loss equations. For discrete MOSFET gate drive circuits, driver ICs and PWM controllers, this methodology can apply to any power supply application with the capability to vary the gate drive voltage amplitude.

1 Introduction

Power supply designers can sometimes gain additional efficiency increases by properly matching the gate drive voltage with the MOSFETs being driven. Driving a MOSFET gate with a higher voltage, results in a lower associated on-resistance, $R_{DS(on)}$, up to a particular point of diminishing return. This can be extremely beneficial to low voltage high current VRM designs and control driven synchronous rectifiers found in many high current isolated power supply applications. In synchronous buck power applications, lowering the MOSFET on-resistance is especially critical for the synchronous rectifier, since in most cases the power loss due to the freewheeling current through the MOSFET channel resistance is the highest single contributor to total dissipated power. There are, however, additional factors to consider.

Higher gate drive voltage levels place additional charge into the gate-to-source junction of the MOSFET, resulting in increased losses within the MOSFET driver stage. In addition, a higher gate charge requirement will produce longer rise and fall times, which impact switching losses in the high-side MOSFET of a synchronous buck converter. To increase efficiency, the applied voltage should drive the MOSFET gates such that the added gate charge and switching losses are less than the power savings gained by lowering $R_{DS(on)}$. For example, taking on an additional 0.5 W of power dissipated in the high-side MOSFET may be acceptable when 1 W of power is saved in the synchronous MOSFET.

2 Definition of Symbols and Abbreviations

The following list of symbols and abbreviations are used throughout the application example of this article.

D— Duty Cycle

F_{SW} — Switching Frequency

G1— Control MOSFET Gate Drive

G2— Synchronous Rectifier MOSFET Gate Drive

$I_{G(sink)}$ — Driver Sink Current

$I_{G(source)}$ — Driver Source Current

I_{OUT} — Output Load Current

L_{LUMP} — Driver to MOSFET Parasitic Inductance

P_{BD} — Synchronous Rectifier MOSFET Body-Diode Power Loss

P_C — MOSFET Conduction Power Loss

P_D — Total Dissipated Power (G1, Q1, G2, Q2)

P_{OUT} — MOSFET Output Capacitance Loss

P_{RR} — Synchronous Rectifier MOSFET Body-Diode Reverse Recovery Power Loss

P_{SW} — MOSFET Switching Loss

Q_G — Total Gate Charge

Q_{RR} — Body-Diode Reverse Recovery Charge

Q1— Control MOSFET

Q2— Synchronous Rectifier MOSFET

$R_{DS(on)}$ — MOSFET Drain-to-Source On Resistance

R_G — MOSFET External Discrete Gate Resistance

R_{GI} — MOSFET Internal Gate Resistance

$R_{G1(sink)}$ — G1 Driver Sink Resistance

$R_{G1(source)}$ — G1 Driver Source Resistance

$R_{G2(sink)}$ — G2 Driver Sink Resistance

$R_{G2(source)}$ — G2 Driver Source Resistance

t_{BDF} — MOSFET Body-Diode Conduction Time, Switch Node Falling

t_{BDR} — MOSFET Body-Diode Conduction Time, Switch Node Rising

t_f — MOSFET Turn Off Fall Time

t_r — MOSFET Turn On Rise Time

V_F — MOSFET Body-Diode Forward Voltage Drop

V_{GS} — Gate-to-Source Voltage

V_{IN} — Input Voltage

V_{TH} — MOSFET Turn On Threshold Voltage

V_{OUT} — Output Voltage

$\Delta\eta$— Change in Overall Efficiency

3 Gate Drive Voltage Considerations

Driving the gates of control MOSFET Q1 and synchronous MOSFET Q2 (see Figure 1) with one voltage level verses another requires careful consideration. The need for additional discrete components, impact to the PCB routing, and the requirement of optimal drive voltage amplitudes that may or may not be readily available are all trade-offs to weigh against the potential efficiency savings from possibly lowering the MOSFET $R_{DS(on)}$.

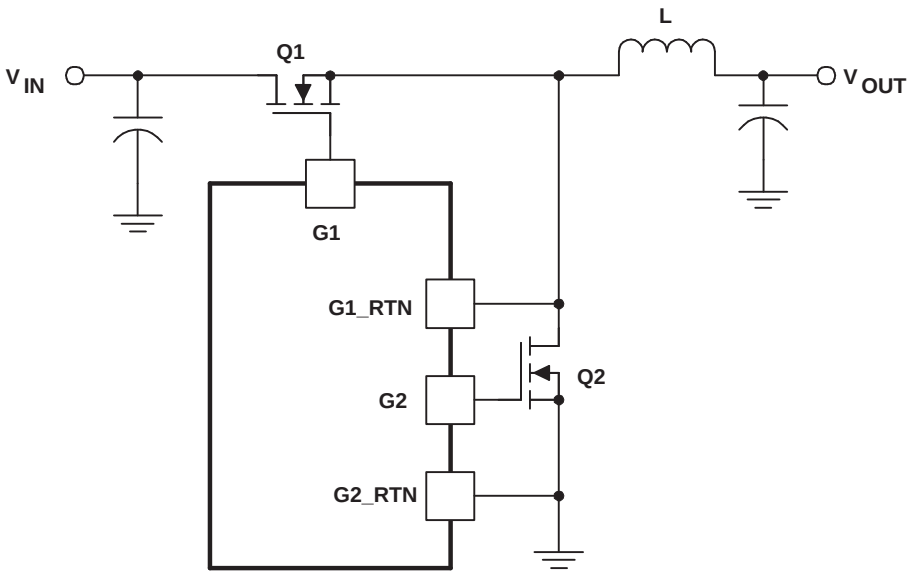

Figure 1. Synchronous Buck Power and Driver Stage

As an example, consider the following analysis using arbitrary devices for the control MOSFET and synchronous rectifier MOSFET. In order to weigh the benefit of one gate-source voltage (V_{GS}) versus another, the $R_{DS(on)}$ versus gate drive voltage and gate drive voltage versus gate charge curves for each MOSFET must be carefully looked at.

The graphs shown in Figure 2 through Figure 4 show typical MOSFET performance characteristic curves found in most manufacturers' data sheets and will be used as a basis for the following application example.

4 Q1 - Control MOSFET

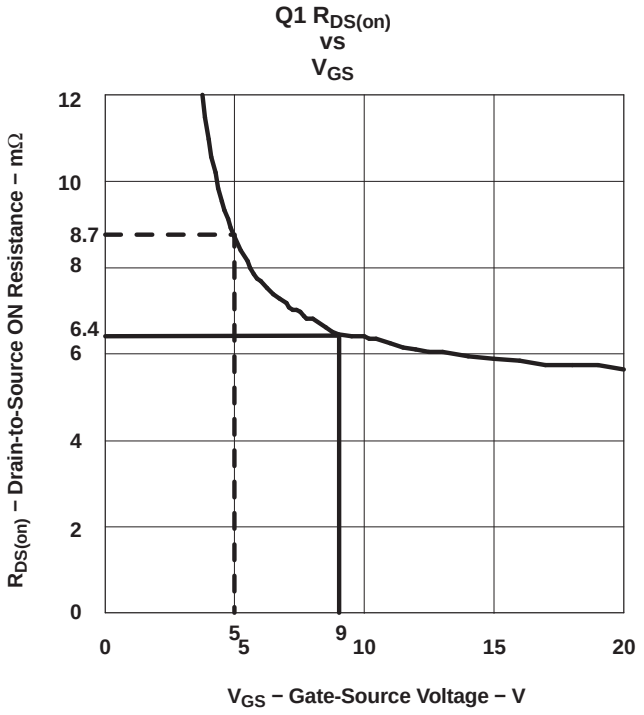

Figure 2.

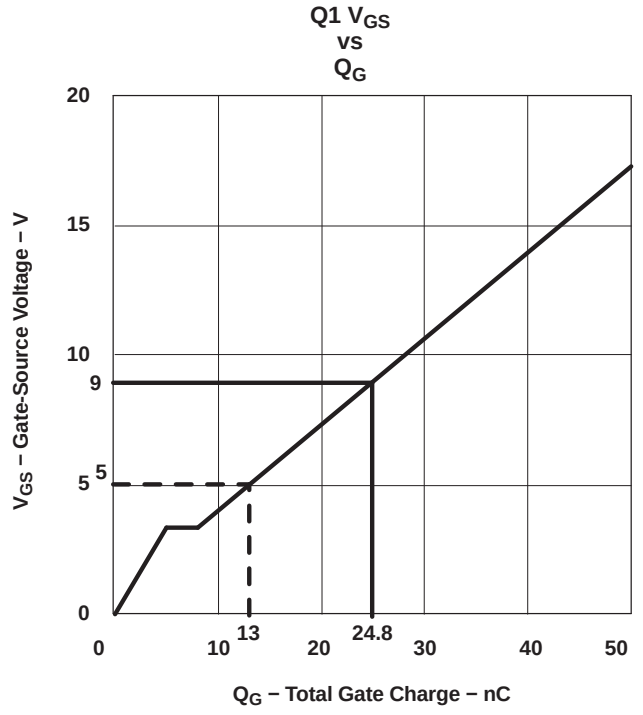

Figure 3.

Figure 2 highlights the $R_{DS(on)}$ values for V_{GS} = 5 V and V_{GS} = 9 V for the control MOSFET, Q1. Since it is more prone to switching loss, Q1 is normally selected based primarily upon lower gate charge, with secondary consideration given to $R_{DS(on)}$. For V_{GS} = 5 V, $R_{DS(on)}$ = 8.7 mΩ , and for V_{GS} = 9 V, $R_{DS(on)}$ = 6.4 mΩ. Similarly Figure 3 shows the impact on gate charge for increasing V_{GS} from 5 V to 9 V. For V_{GS} = 5 V, Q_G = 13 nC, and for V_{GS} = 9 V, Q_G = 24.8 nC. Table 1 summarizes the results.

5 Q2 – Synchronous Rectifier MOSFET

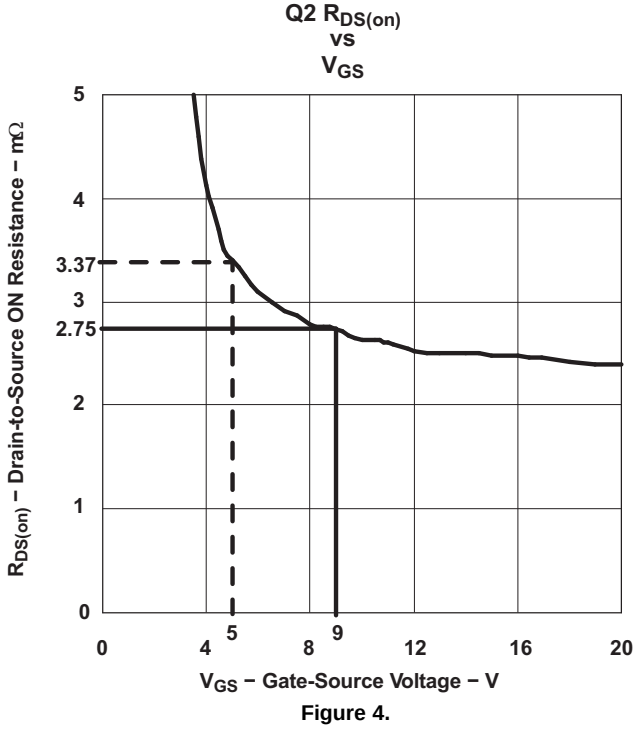

Figure 4.

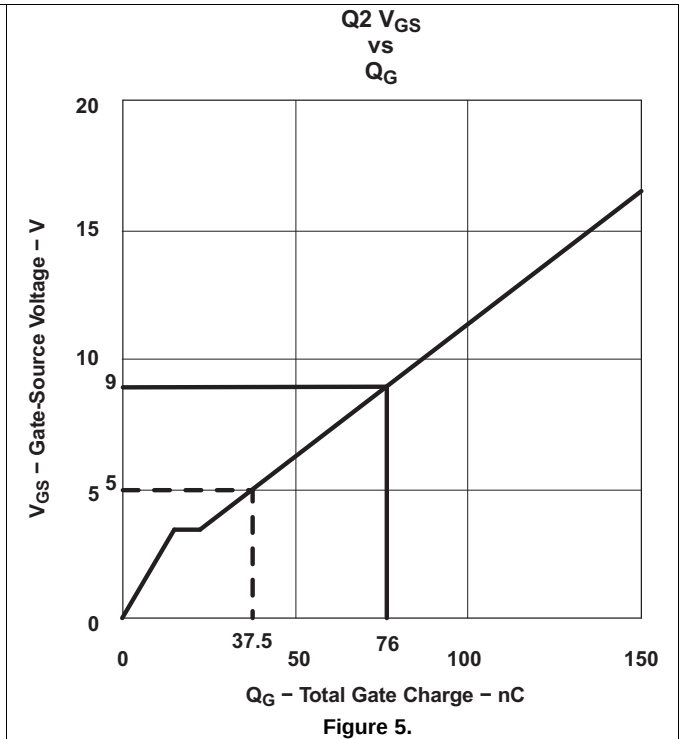

Figure 5.

Figure 4 highlights the $R_{DS(on)}$ values for V_{GS} = 5 V and V_{GS} = 9 V for the synchronous rectifier MOSFET, Q2. Since it is more prone to conduction loss, Q2 is selected based upon lowest possible $R_{DS(on)}$, with secondary consideration given to gate charge. For V_{GS} = 5 V, $R_{DS(on)}$ = 3.37 mΩ , and for V_{GS} = 9 V, $R_{DS(on)}$ = 2.75 mΩ. Similarly, Figure 5 shows the impact on gate charge for increasing V_{GS} from 5 V to 9 V. For V_{GS} = 5 V, Q_G = 37.5 nC, and for V_{GS} = 9 V, Q_G = 76 nC. MOSFET parameters for each case of V_{GS} are summarized in Table 1.

Table 1. MOSFET Parameters for Varying V_{GS}

V_{GS} (V)	$R_{DS(on)}$ (mΩ)	Q_G (nC)	C_{OSS} (pF)	R_{GI} (Ω)	V_{TH} (V)
Q1 – Control MOSFET					
5	8.7	13	400	0.5	2
9	6.4	24.8	400	0.5	2
Q2 – Synchronous Rectifier MOSFET					
5	3.37	37.5	1200	0.5	2
9	2.75	76	1200	0.5	2

Depending upon the maximum load current, the lower $R_{DS(on)}$ resulting from higher V_{GS} yields lower power losses up to some cut-off frequency where switching losses begins to dominate. At higher frequencies where switching losses dominate the lower gate charge resulting from lower V_{GS} will be preferred. At lower frequencies where conduction losses dominate the lower $R_{DS(on)}$ resulting from higher V_{GS} will be preferred. In terms of increasing efficiency, the best choice may be to drive the control MOSFET with a lower V_{GS} to minimize switching losses, and the synchronous rectifier with higher V_{GS} to lower conduction loss. However, since most synchronous buck MOSFET drivers do not offer the option of independently driving the control gate and synchronous gate with different voltages, this may not be a practical solution.

6 MOSFET Driver Parasitics

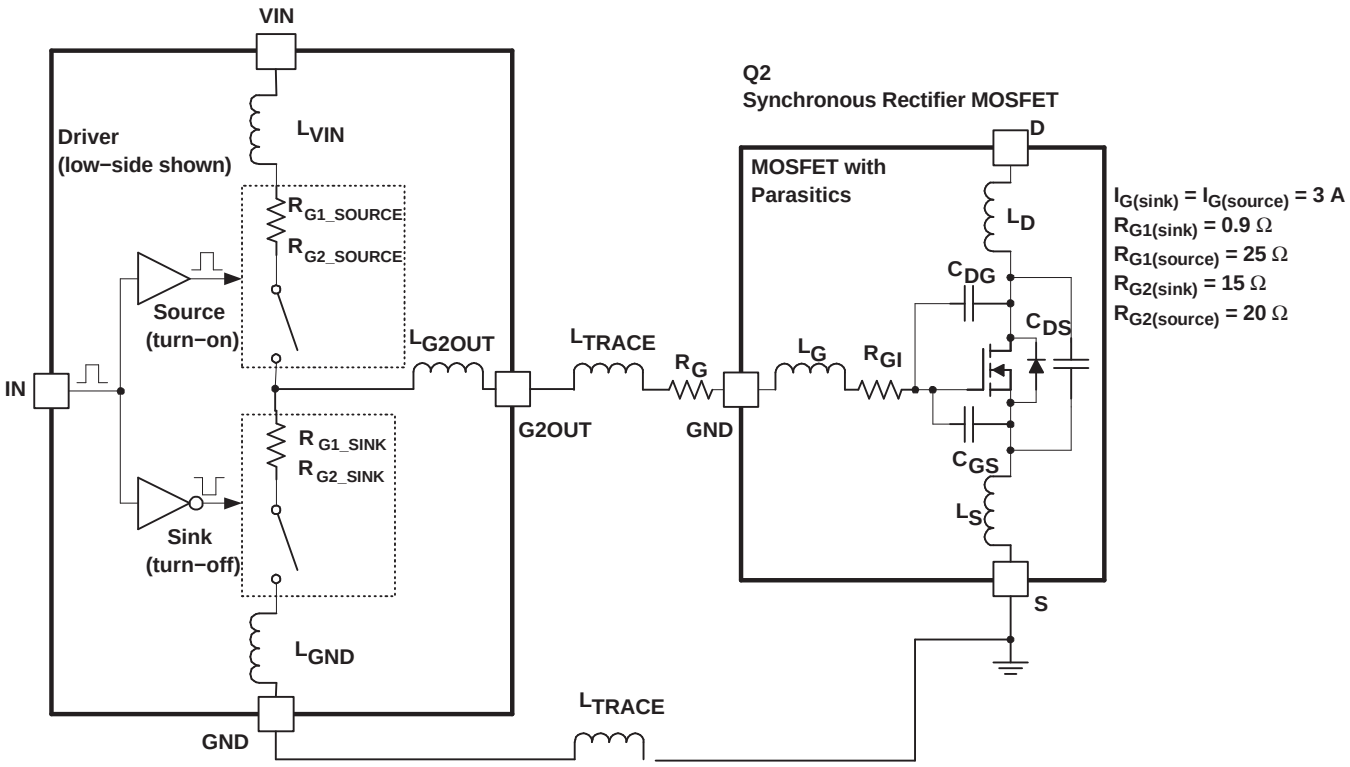

Figure 6. Low-Side Drive and MOSFET Parasitic Model

Figure 6 shows a representative model illustrating most of the parasitic elements that can impact switching power supply performance. For simplicity only the low-side synchronous rectifier MOSFET and driver stage are shown. The resistances associated with the driver sink and source impedances quite often are not the same value and should be specified in a manufacturer's data sheet. It is also important to mention the effect of parasitic inductance between the driver and the MOSFET. At higher frequency operation, this inductance can limit the gate current trying to charge the MOSFET input capacitance. Equation 3 verifies that this results in slower rise and fall times and additional switching losses. The total lumped parasitic inductance, L_{LUMP}, for this example is assumed to be 50 nH. As shown in Figure 6, L_{LUMP} consists mostly of internal lead inductances associated with the MOSFET and driver package type. Since the designer really has no control over these parameters, the only component of parasitic inductance that can be controlled is trace inductance, L_{TRACE}. Therefore minimizing the length of trace between the driver and the MOSFET, as well as running a short and wide gate trace directly over a ground plane, will reduce parasitic trace inductance.

7 Application Example

The following application example compares the efficiency results for two cases of V_{GS}. For simplicity, the same amplitude V_{GS} is used for the control MOSFET and synchronous MOSFET for each case.

Given the following specifications:

- V_{IN} = 5 V
- V_{OUT} = 1.8 V
- I_{OUT} = 20 A
- D = 0.36
- F_{SW} = 200 kHz
- R_G = 0 Ω
- L_{LUMP} = 50 nH

8 Control MOSFET Power Loss Calculations

$$P_C = I_{OUT}^2 \times R_{DS(on)} \times D \quad (1)$$

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times \left(t_R + t_f\right) \times F_{SW} \quad (2)$$

Where tr ≈ tf, and is approximated by:

$$t_r = t_f = \frac{Q_G}{I_G} + \frac{L_{LUMP} \times I_G}{V_{GS} - V_{TH}} \quad (3)$$

$$P_{OUT} = \frac{1}{2} \times \frac{4}{3} \times C_{OSS} \times V_{IN}^2 \times F_{SW} \quad (4)$$

9 High Side Driver Power Loss

Since the sink and source resistances of the driver are so much greater than the MOSFET's internal gate resistance, most of the switch loss associated with charging and discharging the MOSFET gate is dissipated in the driver device.

$$P_{G1} = Q_G \times V_{GS} \times F_{SW} \times \left(\frac{R_{G1(sink)}}{R_{G1(sink)} + R_G + R_{GI}} + \frac{R_{G1(source)}}{R_{G1(source)} + R_G + R_{GI}} \right) \quad (5)$$

Using Equation 1 through Equation 5, the total losses for the control MOSFET and driver can be approximated for each case of V_{GS}.

10 Synchronous Rectifier MOSFET Power Loss

For simplification of calculations, assume the following body-diode characteristics:

- $t_{BDR} + t_{BDF}$ = 10 ns
- Q_{RR} = 48 nC
- V_F = 1 V

$$P_{BD} = V_F \times I_{OUT} \times F_{SW} \times \left(t_{BDR} + t_{BDF}\right) \quad (6)$$

$$P_C = I_{OUT}^2 \times R_{DS(on)} \times (1 - D) \quad (7)$$

$$P_{RR} = Q_{RR} \times V_{IN} \times F_{SW} \quad (8)$$

$$P_{SW} = 0 \quad (9)$$

$$P_{OUT} = 0 \quad (10)$$

11 Low Side Driver Power Loss

$$P_{G2} = Q_G \times V_{GS} \times F_{SW} \times \left(\frac{R_{G2(sink)}}{R_{G2(sink)} + R_G + R_{G1}} + \frac{R_{G2(source)}}{R_{G2(source)} + R_G + R_{GI}} \right) \quad (11)$$

Using Equation 6 through Equation 11, the designer can approximate the total losses for the synchronous rectifier MOSFET and driver for each case of V_{GS}. Since many of the individual losses represented by Equation 1 through Equation 11 are frequency dependant, an EXCEL spreadsheet was designed to calculate and plot the total losses associated with the upper control MOSFET and lower synchronous MOSFET, versus frequency for each case of V_{GS}. A spreadsheet or MathCAD can make it is easy to determine the effect of varying the V_{GS} value.

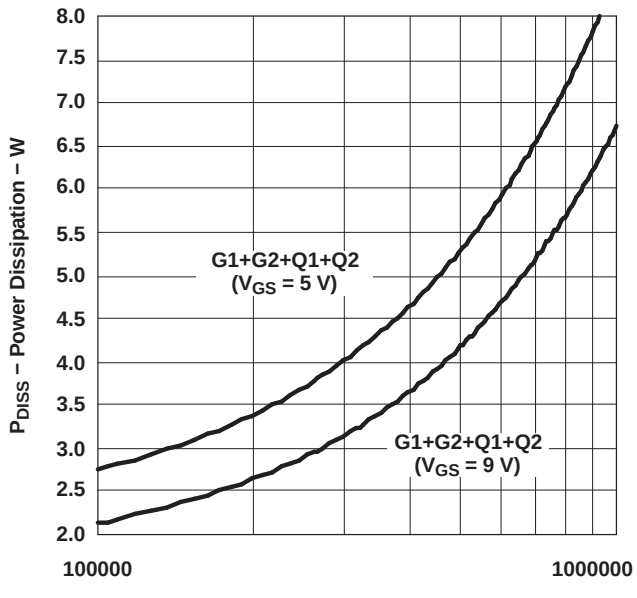

Figure 7.

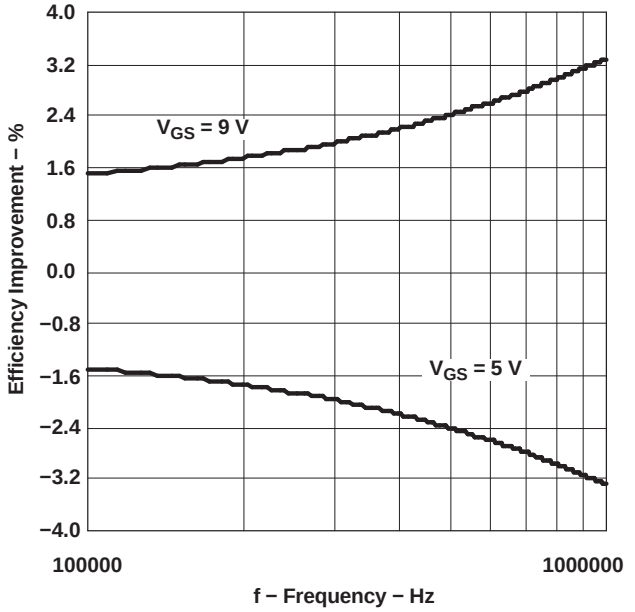

Figure 8.

Figure 7 shows Equation 1 through Equation 11 plotted against varying frequency (100 kHz to 1 MHz) for each case of V_{GS}. Although these graphs can be generated at any output load current of interest, the results of Figure 7 are shown at $I_{OUT(max)}$ = 20 A, which is the point where rising MOSFET junction temperatures benefit most from higher efficiency. For I_{OUT} = 20 A, it is clear that V_{GS} = 9 V results in significantly less dissipated power over all frequencies of interest. Having calculated the total dissipated power for each case of V_{GS}, and knowing the maximum output power, the graph of Figure 8 is developed using Equation 12.

$$\Delta\eta = \left[\frac{\pm\, P_{OUT(max)} \times \left(P_{DISS(9V)} - P_{DISS(5V)}\right)}{\left(P_{OUT(max)} + P_{DISS(5V)}\right) \times \left(P_{OUT(max)} + P_{DISS(9V)}\right)} \right] \times 100\% \tag{12}$$

In addition to the driver and MOSFET effects, the power stage components must also be considered when selecting the optimal switching frequency. Since analyzing the power stage frequency effects are beyond the scope of this example, it is assumed that 200 kHz is a good trade-off between optimizing the MOSFET and gate drive circuitry and maintaining a fairly high frequency to minimize the size of the passive components in the power stage. The graph of Figure 8 shows an efficiency increase of approximately 1.7 percent at 200 kHz, for V_{GS} = 9 V and I_{OUT} = 20 A.

Selecting a switching frequency of 200 kHz, it would be helpful to know what effect V_{GS} has over the entire load range at the selected frequency. Equation 1 through Equation 11 can next be plotted versus load current at a fixed 200-kHz frequency.

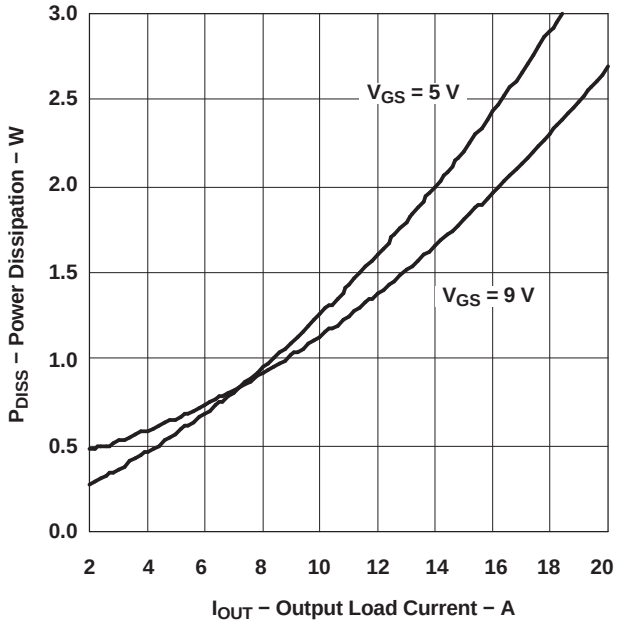

Figure 9.

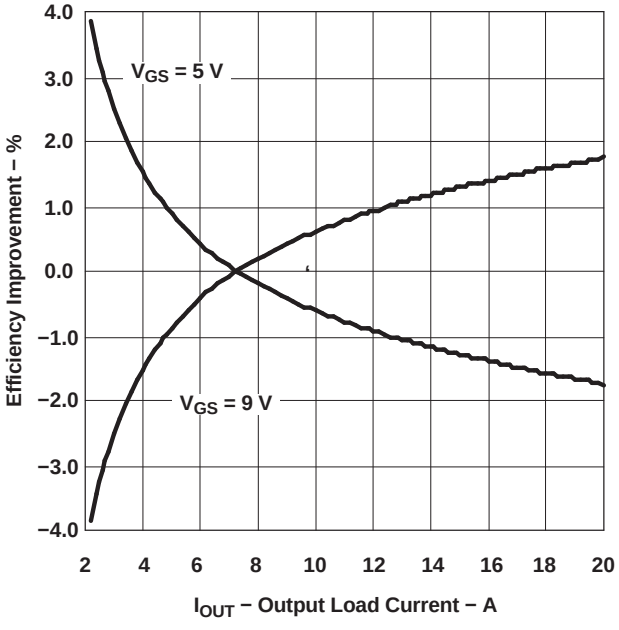

Figure 10.

Figure 9 shows the effects of power dissipation versus load current for V_{GS} = 5 V and V_{GS} = 9 V at a fixed 200 kHz frequency. As expected, Figure 10 shows a 1.7 percent efficiency increase for V_{GS} = 9 V at I_{OUT} = 20 A. However, at I_{OUT} less than 7 A, V_{GS} = 9 V results in an efficiency loss compared to V_{GS} = 5 V. For I_{OUT} less than 7 A, the efficiency improvement resulting from lower conduction loss has less effect, as is evident by Equation 1 and Equation 7. At lighter load current, frequency dependant losses begin to dominate over current dependant (conduction) losses, so a lower V_{GS} = 5 V, hence a lower overall gate charge, is preferred.

It is interesting to note that by iterating through this graphical process, we can optimize the combination of V_{GS} and switching frequency. In this example, for instance using V_{GS} = 9 V, at a frequency of 200 kHz we can gain 1.7 percent efficiency at maximum output current, at the cost of lower efficiency at lighter load current. Conversely, using V_{GS} = 5 V at 200 kHz would result in higher efficiency just below the mid range of load current, but a lower efficiency at higher load current.

Following are the detailed calculations used to generate the graphs shown in Figure 7 through Figure 10:

11.1 Control MOSFET, V_{GS} = 5 V

$$P_{C(5V)} = 20\ A^2 \times 8.7 \times 10^{-3}\ \Omega \times 0.36 = 1.253\ W \quad (13)$$

$$t_{R(5V)} = t_{f(5V)} = \frac{13 \times 10^{-9} C}{3\ A} + \frac{50 \times 10^{-9} H \times 3\ A}{5\ V - 2\ V} = 54.3 \times 10^{-9}\ s \quad (14)$$

$$P_{SW(5V)} = \frac{1}{2} \times 5\ V \times 20\ A \times \left(54.3 \times 10^{-9}\ s + 54.3 \times 10^{-9}\ s\right) \times \left(200 \times 10^{3}\ Hz\right) = 1.09\ W \quad (15)$$

$$P_{OUT(5V)} = \frac{1}{2} \times \frac{4}{3} \times 400 \times 10^{-12}\ F \times 5\ V \times 200 \times 10^{3}\ Hz = 0.27\ mW \quad (16)$$

And the power dissipated in the driver device at V_{GS} = 5 V is:

$$P_{G1(5V)} = 13 \times 10^{-9}\ C \times 5\ V \times 200 \times 10^{3}\ Hz \times \left(\frac{0.9\ \Omega}{0.9\ \Omega + 0 + 0.5\ \Omega} + \frac{25\ \Omega}{25\ \Omega + 0 + 0.5\ \Omega}\right) = 21.1\ mW \quad (17)$$

The total power loss of the upper control MOSFET and the gate driver device is simply the sum of all the losses given by Equation 13 through Equation 17.

$$P_{G1\_TOTAL(5V)} = 1.253\ W + 1.09\ W + 0.27 \times 10^{-3}\ W + 21.1 \times 10^{-3}\ W = 2.36\ W \quad (18)$$

11.2 Control MOSFET, V_{GS} = 9 V

$$P_{C(9V)} = 20\ A^2 \times 6.4 \times 10^{-3}\ \Omega \times 0.36 = 0.922\ W \quad (19)$$

$$t_{R(9V)} = t_{f(9V)} = \frac{24.8 \times 10^{-9} C}{3\ A} + \frac{50 \times 10^{-9} H \times 3\ A}{9\ V - 2\ V} = 30 \times 10^{-9}\ s \quad (20)$$

$$P_{SW(9V)} = \frac{1}{2} \times 5\ V \times 20\ A \times \left(30 \times 10^{-9}\ s + 30 \times 10^{-9}\ s\right) \times \left(200 \times 10^{3}\ Hz\right) = 0.6\ W \quad (21)$$

$$P_{OUT(9V)} = \frac{1}{2} \times \frac{4}{3} \times 400 \times 10^{-12}\ F \times 5\ V \times 200 \times 10^{3}\ Hz = 0.27\ mW \quad (22)$$

And the power dissipated in the driver device at V_{GS} = 9 V is:

$$P_{G1(9V)} = 24.9 \times 10^{-9}\ C \times 9\ V \times 200 \times 10^{3}\ Hz \times \left(\frac{0.9\ \Omega}{0.9\ \Omega + 0 + 0.5\ \Omega} + \frac{25\ \Omega}{25\ \Omega + 0 + 0.5\ \Omega}\right) = 72.46\ mW \quad (23)$$

The total power loss of the upper control MOSFET and the gate driver device is simply the sum of all the losses given by Equation 19 through Equation 23.

$$P_{G1\_TOTAL(9V)} = 0.922\ W + 0.6\ W + 0.27 \times 10^{-3}\ W + 72.46 \times 10^{-3}\ W = 1.595\ W \quad (24)$$

11.3 Synchronous Rectifier MOSFET, V_{GS} = 5 V

$$P_{BD(5V)} = 1\ V \times 20\ A \times 200 \times 10^{3}\ Hz \times \left(10 \times 10^{-9} s\right) = 40 \times 10^{-3}\ W \quad (25)$$

$$P_{C(5V)} = 20\ A^2 \times 3.37 \times 10^{-3}\ \Omega \times (1 - 0.36) = 0.863\ W \quad (26)$$

$$P_{RR(5V)} = 37.5 \times 10^{-9}\ C \times 5\ V \times 200 \times 10^{3}\ Hz = 37.5 \times 10^{-3}\ W \quad (27)$$

And the power dissipated in the driver device at V_{GS} = 5 V is:

$$P_{G2(5V)} = 37.5 \times 10^{-9}\ C \times 5\ V \times 200 \times 10^{3}\ Hz \times \left(\frac{15\ \Omega}{15\ \Omega + 0 + 0.5\ \Omega} + \frac{20\ \Omega}{20\ \Omega + 0 + 0.5\ \Omega}\right) = 72.88 \times 10^{-3}\ W \quad (28)$$

The total power loss of the synchronous rectifier MOSFET and the gate driver device is simply the sum of all the losses given by Equation 25 through Equation 28.

$$P_{G2\_TOTAL(5V)} = 40 \times 10^{-3}\ W + 0.863\ W + 37.5 \times 10^{-3}\ W + 72.88 \times 10^{-3}\ W = 1.014\ W \quad (29)$$

11.4 Synchronous Rectifier MOSFET, V_{GS} = 9 V

$$P_{BD(9V)} = 1\ V \times 20\ A \times 200 \times 10^{3}\ Hz \times \left(10 \times 10^{-9} s\right) = 40 \times 10^{-3}\ W \quad (30)$$

$$P_{C(9V)} = 20\ A^{2} \times 2.75 \times 10^{-3}\ \Omega \times (1 - 0.36) = 704 \times 10^{-3}\ W \quad (31)$$

$$P_{RR(9V)} = 76 \times 10^{-9}\ C \times 5\ V \times 200 \times 10^{3}\ Hz = 76 \times 10^{-3}\ W \quad (32)$$

And the power dissipated in the driver device at V_{GS} = 9 V is:

$$P_{G2(9V)} = 76 \times 10^{-9}\ C \times 9\ V \times 200 \times 10^{3}\ Hz \times \left(\frac{15\ \Omega}{15\ \Omega + 0 + 0.5\ \Omega} + \frac{20\ \Omega}{20\ \Omega + 0 + 0.5\ \Omega}\right) = 265.85 \times 10^{-3}\ W \quad (33)$$

The total power loss of the synchronous rectifier MOSFET and the gate driver device is simply the sum of all the losses given by Equation 30 through Equation 33.

$$P_{G2\_TOTAL(9V)} = 40 \times 10^{-3}\ W + 704 \times 10^{-3}\ W + 76 \times 10^{-3}\ W + 265.85 \times 10^{-3}\ W = 1.086\ W \quad (34)$$

Results from the application example are summarized in Table 2:

Table 2. F = 200 kHz, I_{OUT} = 20 A, Power Dissipation Summary for Varying V_{GS}

V_{GS} (V)	Q1 – Control MOSFET	Q2 – Synchronous Rectifier MOSFET	Driver IC (G1)	Driver IC (G2)	Total Power Loss (MOSFETs + Driver IC)	Δη
5 V	2.34 W	0.941 W	21.1 mW	72.88 mW	3.375 W	N/A
9 V	1.52 W	0.820 W	72.46 mW	265.85 mW	2.678 W	1.65%

For F_{SW} = 200 kHz and I_{OUT} = 20 A, driving Q1 and Q2 with V_{GS} = 9 V as opposed to V_{GS} = 5 V results in an overall efficiency improvement of nearly 1.7 percent as shown in Table 2. For this example, a significant full load overall efficiency improvement can be gained by driving Q1 and Q2 with V_{GS} = 9 V, at the trade-off of slightly lower efficiencies below I_{OUT} = 7 A. The total losses for Q1 and Q2 given in Table 2 seem reasonable; however the thermal impedances of each MOSFET package should also be considered to make sure that junction temperatures are within rated limits. If junction temperatures are not being exceeded by chosen design constraints, it may be possible to further increase the switching frequency.

12 Conclusion

Using a given set of design parameters for a synchronous buck power stage, a full load efficiency gain of up to 1.7 percent can be realized when the MOSFET gates are driven at 9 V as opposed to 5 V. For this example, conduction losses were dominant at load currents greater then 7 A. For load currents less than 7 A, switching losses were dominant and efficiency was shown to actually decrease by up to 4%. In summary, higher light load efficiency could be expected for V_{GS} = 5 V, and higher full load efficiency was shown at V_{GS} = 9 V. When considering what level of V_{GS} to design for, examining the MOSFET power loss equations graphically can offer better insight as to where the benefits lie when frequency and output current are varied.

Given the choice, what is the optimal gate drive voltage amplitude for driving a switching MOSFET in a power supply application? The answer is not always clear, but with the aid of a spreadsheet or MATHCAD, the designer can make a fair comparison to graphically examine the trade-offs and potential benefits.

For more information about gate drive considerations, see the TI.com Gate Drivers portal.

13 References

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4. *Estimating MOSFET Switching Losses Means Higher Performance Buck Converters*, by Peter Markowski, PlanetAnalog.com, December 18, 2002

Revision History

Changes from Original (June 2005) to A Revision	Page
• Corrected axes on Figure 4 and Figure 5	5
• Added link to TI.com Gate Drivers portal	12

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