

TUSB1210 ES2.0 Errata

This errata document is for the TUSB1210 device, TI literature number [SLLSE09](#).

1 TUSB1210 fails on EL_34 certification test (CHIRP width) in slave HOST mode

ERRATA REFERENCE: Errata ID: TUSB1210-200-001 (Unique reference for communication)

CRITICALITY: Medium

DESCRIPTION: In ULPI clock input mode (60 MHz clock provided by the Link) , NXT toggles during CHIRP. This causes the link to sometimes send CHIRP K or CHIRP J twice. As a result the EL_34 certification test can fail (but failure is not systematic), since an individual CHIRP may last up to 100 us (instead of 60 μ s max allowed by the spec). No impact on functionality has been observed to date. All external devices tried so far enumerate correctly with OMAP3630 Link + TUSB1210 ES2.0. This does not affect ULPI clock output mode (60 MHz clock provided by TUSB1210).

WORKAROUND: No functional issue observed to date, therefore no workaround is required.

REVISIONS IMPACTED:

TUSB1210		
Revision	ES1.0	ES2.0
Impacted	No	Yes

2 TUSB1210 OFF mode leakage observed on VDD18 pin on some parts when external supplies are present and chip is powered down (CS=0)

ERRATA REFERENCE: Errata ID: TUSB1210-200-002 (Unique reference for communication)

CRITICALITY: Low

DESCRIPTION: Current leakage in OFF mode (platform sleep) on VDD18 pin when TUSB1210 is OFF (CS=0) and external supplies VBAT, VDDIO are present, may exceed the 5 μ A typical target.

The max leakage observed is 300 μ A.

WORKAROUND: OFF mode leakage can be avoided by tying CS pin to VDDIO supply permanently.

This is already the default implementation used in the majority of customer applications.

REVISIONS IMPACTED:

TUSB1210		
Revision	ES1.0	ES2.0
Impacted	Yes	Yes

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