Errata to TFP101(A), TFP201(A), TFP401(A), TFP403, Datasheet Literature Numbers SLDS116A, SLDS119C, SLDS120B, SLDS125A

Revision History
Revision 1.0 –
- Packaging information

Revision 1.1 –
- Packaging information update from Revision 1.0
- SCDT information

1. **PowerPAD dimension**.
ISSUE:

The previous data sheet PowerPAD dimensions were not shown. Those have been added as a new sheet in the current data sheet under the title 'Thermal Pad Mechanical Data'.

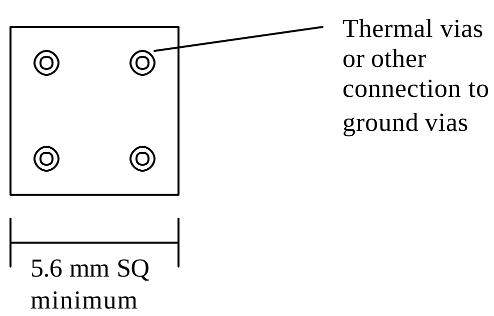
Changes to document:

In the "PowerPAD…" section, add a sentence to paragraph 1, reword paragraph 2 and add figure and paragraphs between existing paragraphs 2 &3 to read:

… Soldering the back side of the … to the application board is not required thermally as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back side pad.

Soldering the back side pad of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5.6mm sq. minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.



More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com

Table 1 outlines the thermal properties of the TI 100-TQFP.

2. Sync Detect Description

2.1 Changes to document:

In the Sync Detect description information on page 15 in the TFP401(A) datasheet and page 14 in the TFP201(A), TFP101(A) datasheet change:

FROM

The TFPX01 offers an output, SCDT to indicate link activity. The TFPX01 monitors activity on DE to determine if the link is active. When 1 million (1e6) pixel clock periods pass without a transition on DE, the TFPX01 considers the link inactive and SCDT is driven low. While SCDT is low, if two DE transitions are detected within 1600 pixel clock periods, the link will be considered active and SCDT is pulled high.

TO

The TFPX01 offers an output, SCDT, to indicate link activity. The TFPX01 monitors activity on DE to determine if the link is active. When 2^18 clocks produced by an on-chip free running oscillator whose frequency is around 10-15 MHz pass without a transition on DE, the TFPX01 considers the link inactive and SCDT is driven low. Hence SCDT goes low after the terminal count of the counter is reached that is 17~26 ms. When SCDT is low, if 8 DE edges are detected within the terminal count of 2^18 clocks, the link is considered active and SCDT goes high.

In the Sync Detect description information on page 14 in the TFP403 datasheet change:

FROM

The TFP403 offers an output, SCDT to indicate link activity. The TFP403 monitors activity on DE to determine if the link is active. When 1 million (1e6) pixel clock periods pass without a transition on DE, theTFP403 considers the link inactive and SCDT is driven low. The SCDT goes high immediately after the first transition on DE. The SCDT again becomes low when no more transitions are seen after 2^18 oscillator clocks.

TO

The TFP403 offers an output, SCDT to indicate link activity. The TFP403 monitors activity on DE to determine if the link is active. When 2^18 clocks produced by an on-chip free running oscillator whose frequency is around 10-15 MHz pass without a transition on DE, the TFP403 considers the link inactive and SCDT is driven low. Hence SCDT goes low after the terminal count of the counter is reached that is 17~26 ms. When SCDT is low, if 8 DE edges are detected within the terminal count of 2^18 clocks, the link is considered active and SCDT goes high.

Refer to the page 8 of the TFP403, TFP401(A) datasheet and page 7 of the TFP201(A) datasheet, table AC specifications, change:

FROM

$t_{t(HSC)}$ Transition time between DE transition to SCDT low: 1e6 t_{pix}

TO

$t_{t(HSC)}$ Transition time between DE transition to SCDT low: ~17-26 ms

FROM

$t_{t(FSC)}$ Transition time between DE transition to SCDT high: 1600 t_{pix}

TO

$t_{t(FSC)}$ Transition time between DE transition to SCDT high: 8 DE transitions

Refer to page 7 of the TFP101(A) data sheet, table AC specifications, change:

FROM

$t_{t(HSC)}$ Transition time between DE transition to SCDT low: 1e6 t_{pix}

TO

$t_{t(HSC)}$ Transition time between DE transition to SCDT low: ~17-26 ms

FROM

$t_{t(FSC)}$ Transition time between DE transition to SCDT high: 1024 t_{pix}

TO
$t_{t(FSC)}$ Transition time between DE transition to SCDT high: 8 DE transitions

2.2 Sync Detect Operation

- Some graphics card when in sleep/standby mode send characters that can make the DE toggle and make SCDT high, hence in such applications, to robustly determine if the link is in active or inactive mode, it is recommended that a sync signal like HSYNC can be used in addition to the SCDT. Timing format on the recovered HSYNC signal can be used in addition to SCDT to determine if the link is receiving a valid video format.

- In applications where PD is being pulsed (to save power while in sleep/standby mode) when the link is inactive, and SCDT is used solely to determine the link activity, then in such cases SCDT should not be used until 25 ms of signal and power application.

- There is a rare possibility that SCDT can get stuck high on power up or removal of the DVI signal. For example: If the power on a DVI distribution box sourcing the signal to the receiver is cycled rapidly (2-3 times/second), then there is a small possibility, (1 in ~40-50 times) of cycling power that SCDT may be stuck high when the box is powered off.

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