EVM User's Guide: TCAN284XEVM

TCAN284x-Q1 Evaluation Module

Description

The TCAN284XEVM is an evaluation module that supports testing any CAN/LIN Integrated SBC within the TCAN284XX and TCAN285XX families of devices. This user guide explains how the board is setup as well as how to leverage this board as a base of new project development.

Get Started

Board is ready to operate out of box. The user should apply SPI signals to J29 after device has been powered up to begin configuring the device. Please see device specific data sheet for register and programming information.

Features

- The TCAN284XX and TCAN285XX families are AEC-Q100: Qualified for automotive applications
- Meets the requirements for CAN FD ISO 11898-2:2024
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987–4:2023 compliant and conforms to SAEJ2602 recommended practice for LIN
- CAN FD and LIN transceiver higher data rates
  - CAN FD supports 5Mbps
  - LIN transceiver supports fast mode of 200kbps
- Classic CAN backwards compatible
- Functional Safety Quality Managed
  - Multiple methods to wake from sleep mode
  - CAN and LIN bus wake up pattern (WUP)
- Local wake up (LWU) via WAKE pins
  - Using a high side switch, cyclic sensing wake up is supported
  - CAN selective wake up frame (WUF)
  - Digital wake up using the SW pin
- Low drop out (LDO) regulator supporting 250mA externally at 3.3V or 5V, VCC1
- 5V LDO regulator supports up to 200mA externally, VCC2
- Control of an external PNP transistor supporting 350mA at 1.8V, 2.5V, 3.3V or 5V
- 3.3V and 5V MCU support
- CAN and LIN support ±58V Bus fault protection
- Timeout, window and Q&A watchdog support
- EEPROM to save device configuration
- Advanced CAN bus fault diagnostics

Applications

- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric and power train systems
- Industrial transportation

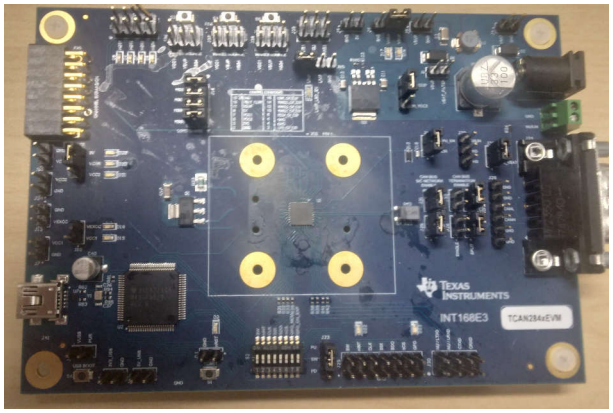


Figure 1-1. TCAN284XEVM - Top View

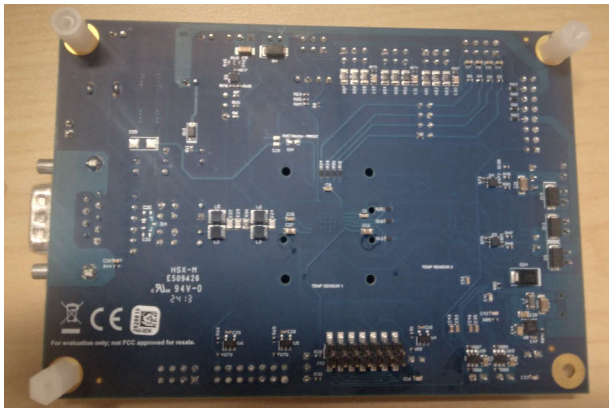


Figure 1-2. TCAN284XEVM - Bottom View

1 Evaluation Module Overview

1.1 Introduction

The TCAN284XX and TCAN285XX lines of Integrated CAN/LIN SBCs allow for a vast array of potential use cases that can be quickly tested on the TCAN284XEVM. The EVM provides a base to test multiple configurations on the SBC including CAN and LIN communication, SBC state, Fail-Safe Mode, watchdog timer configuration, power regulation in the form of 2 integrated LDOs. There is an option to add a PNP transistor to have a full 3 LDOs controlled by the single SBC.

1.2 Kit Contents

Table 1-1 lists the contents of the EVM kit. A TCAN284XEVM board with a TCAN28475 preinstalled. No other assembly is required, and works directly out of box.

Table 1-1. Kit Contents

ITEM	QUANTITY
TCAN284XEVM test board	1

1.3 Specification

This board closely follows the TCAN284xx and TCAN285xx family of devices limiting factors and recommended operating conditions. The temperature conditions do no imply that the board generates that much heat. The IC and board components can withstand higher heat.

Operational Parameter	Description	Min	Typical	Max	Unit
VSUP	Supply Voltage	4.5	-	28	V
VHSS	HSS Supply Voltage	5	-	28	V
VCAN	CAN Transceiver Supply Voltage	4.5	-	5.5	V
V_LIN	LIN Bus Input Voltage (TCAN28X7X Only)	0	-	28	V
V_CANBUS	CAN Bus Voltage (Absolute Max/Min)	-58	-	58	V
V_LOGIC	Logic Pin Voltage (Absolute Max/Min)	-0.3	-	6	V
IOH(DO)	Digital Output Current High Level	-2	-	-	mA
IOL(DO)	Digital Output Current Low Level	-	-	2	mA
IO(LIMP)	LIMP Pin Current when Configured as LIMP	-	-	6	mA
IO(HSSx)	HSS Pin Current	-	60	100	mA
IO(VCC1)	Output Current VCC1	-	-	250	mA
IO(VCC2)	Output Current VCC2	-	-	200	mA
IO(VEXCC)	Output Current VEXCC	-	-	350	mA
TSDWR	Thermal Shutdown Waring	145	-	165	C
TSDWF	Thermal Shutdown Waring Release	130	-	155	C
TSDR	Thermal Shutdown	165	-	200	C
TSDF	Thermal Shutdown Release	155	-	190	C
TJ	Junction Temperature	-40	-	150	C

1.4 Device Information

The TCAN284xx-Q1 is a family of system basis chips (SBC) that provide a control area network flexible data rate capable (CAN FD) transceiver that supports selective wake. The TCAN2847x-Q1 includes a local interconnect network (LIN) transceiver. The CAN FD transceiver supports data rates up to 5Mbps while the LIN transceiver supports fast mode data rates up to 200kbps. The VCC1 LDO provides 3.3V or 5V ±2% with up to 250mA of current and determines the digital IO logic values. If more current is needed an external PNP transistor can be used to support up to 350mA and voltages of 1.8V, 2.5V, 3.3V or 5V. VCC2 LDO provides 5V up to 200mA.

The TCAN284xx-Q1 includes features such as LIMP, three local wake inputs and four high side switches. The high side switch can be on/off, 10-bit PWM or timer controlled. Using the GFO pin, the user can control an external CAN FD, LIN transceiver, CAN SBC or LIN SBC. The WAKE pins can be configured for static sensing, cyclic sensing (with HSS4 pin) and pulse based for waking up. These devices provide EEPROM to store specific device configuration information. Thus, avoiding extensive reprogramming after power fluctuations. WAKE1 and WAKE2 can enable an internal switch between pins to enable external VBAT monitoring. WAKE3 can be configured as a direct drive control pin for any combinations of high-side switches when cyclic sensing wake is enabled.

2 Hardware

2.1 Power Requirements

The TCAN284XEVM only requires a single power input to power on the entire board for 5V, but it should be noted that the SBC requires 3 separate power inputs, VSUP (device), VCAN (CAN bus), and VHSS (High Side Switch supply). The suggestion is to allow up to 1A to 1.5A of power depending on use case of the integrated LDOs and LDO controller. Power can be applied at J3, which is a barrel jack that can accept between 4.5V and 28V, power can also be applied across headers J4 which bypasses the barrel jack located at J3. If the end user wants to test the reverse polarity protection no action is necessary after placing power connection, at J3 or J4; however, as a bypass, shunt header J1. Power can also be applied directly to ICs VSUP pin through J5 which inherently bypasses battery EMI filter and reverse polarity protection. To power the high side switch supply, VHSS, the end user can apply a separate voltage to J6 pin 2, or the user can shunt J6 pin 2 to VSUP (also located on J6) to power VHSS with VSUP (a relatively standard implementation of this pin). The VCAN pin depends on the device soldered down for U1. J9 pin 2 is the breakout connection for the VCAN pin. The pin can be shunted to either the external 5V LDO U3 (if enabled) or VCC2 for a 5V source, this guidance applies for any device variant. If the end user is using a 5V SBC (TCAN28XX5), the user can also attach a jumper wire from VCC1 (located at J19) to power VCAN.

Only VSUP is required for the board to operate. Everything except CAN and HSS source is powered through the VSUP pin. If HSS and CAN, testing must be performed.

Beyond device power there is an external LDO, U3, that is used in up to three ways on the board. The first is to supply a source voltage for indicator LED driving. The second is to provide a bias voltage for the SW pin if pulled up. Finally, U3 can be used to power VCAN. To enable U3, J12 must not be left floating and either shunt J12 pin 2 to pin 1 or pin 3 (VSUP or VCC2) for the enable signal. For current measurement tests, the best option is to leave J12 floating to prevent the LDO from drawing current during testing. This comes at the cost of no LED driving and if SW is being pulled high a different pull-up source must be used.

As a first check of the board before any modification, the suggestion is to do the following steps:

1. Apply 4.5V to 28V source to J3 or J4. If using 4.5V source shunt J1 to remove the diode drop. Keep this supply off at the moment.
2. Shunt VHSS to VSUP through J6.
3. Shunt J12 pin 2 to either pin 1 or pin 3 on J12 to turn on U3 5V LDO.
4. Shunt J9 pin 2 to either pin 1 or pin 3 on J9 to power VCAN
5. Shunt “SW” to “PU” on J23 to hold SW high during power up.
6. Turn on main supply power. If everything is powered correctly, the power LED indicators light up. Letting the end user know the board is powered properly.

2.2 Setup

The board is ready for most applications directly out of the box after basic configuration. After initial power up test as described in Power Requirement section the board is ready for configuration. The SW pin should be held in the active state (which is high by default) during prototyping and debugging so the standby watchdog doesn’t send the device to sleep mode.

Many device applications can be tested on the TCAN284XEVM without the need for further modification. This section is intended to highlight common application elements that can be utilized with the TCAN284XEVM with a focus on power management, transceiver operation, special use pins, protection features, and finally a look into simple modifications on the board for other testing purposes.

2.2.1 Power Management Setup

The TCAN284XX and TCAN285XX families both share two integrated fixed voltage LDOs, a variable voltage integrated LDO controller, and four high side switches as power management subsystems to the main IC.

The integrated LDOs represent VCC1 and VCC2 output pins on the TCAN284XX/TCAN285XX device. VCC1 is considered the primary LDO of the system. The device cannot enter standby until VCC1 is at a proper level for a preset period of time and many subsystems are internally referenced or powered directly by VCC1 including SPI operation and logic interface voltage ranges. The TCAN284X5/TCAN285X5 variants of the IC VCC1 has a 5V output and is rated to supply up to 250mA while the TCAN284X3/TCAN285X3 variants of the IC, VCC1 has a

3.3V output and is rated to the same 250mA. If the interfacing controller is a 3.3V device, then the TCAN284X3/ TCAN285X3 variant is chosen and a variant ending in “5” is for 5V interfaces. VCC1 can be accessed for routing to external loads from header J7 on the board and configured at register addresses Ch, Dh, and Eh. VCC2 is powered by the second LDO which regardless of device variant is always 5V rated up to 200mA of output current. VCC2 can be accessed for external loads from header J34 and can be configured at register address Ch.

The LDO controller is comprised of 3 pins (VEXMON, VEXCTRL, VEXCC) that are connected to an external PNP transistor with a β of 50 to 500. VEXMON is the voltage monitor pin and is connected to both the emitter of the PNP and the VSUP pin through a shunt resistor. The shunt resistor sets the current limit of the of the external LDO. VEXCTRL is connected to the base of the PNP transistor and controls the external LDO. VEXCC is the connected to the collector of the PNP and acts as the output of the VEXCC.

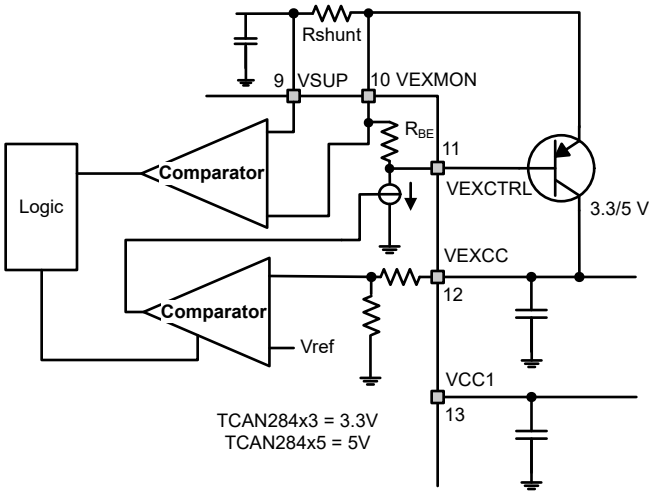


Figure 2-1. Stand-Alone Configuration for VEXCC

In applications where VEXCC is not used, make sure that VEXMON is not left floating and is connected to VSUP. This external LDO controller can support 1.8V, 2.5V, 3.3V, and 5V output levels with up to 350mA of rated current. The controller can be accessed through header J13 and configured at register address Dh.

In some applications, the current allowed from any of the LDO, integrated, or otherwise, may not be enough. The TCAN284XX/TCAN285XX designs did take this into consideration and gave the ability of load sharing; therefore, increasing the total available current output for a specific load. There is simple test with the EVM where the first thing done is to configure VEXCC to be on (the EVM is off by default). Change the voltage control method to be load sharing. This can be accessed at the register address Dh. After the device has been properly configured, shunting J19 shorts VCC1 and VEXCC together, and a load sharing application can now be further tested.

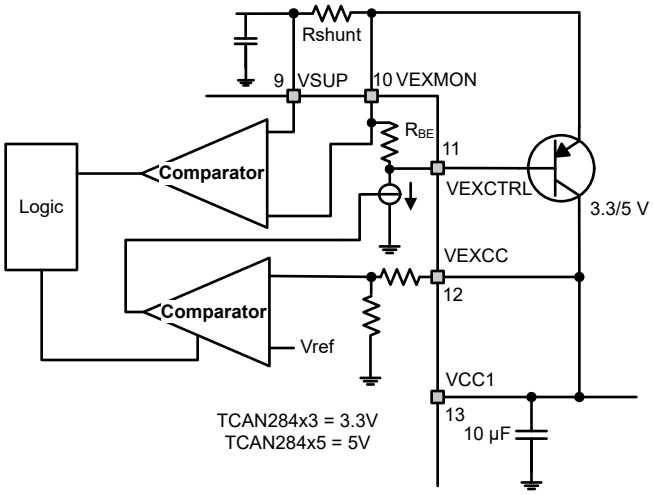


Figure 2-2. VCC1 + VEXCC Load Sharing

The other main power management feature of these devices comes in the form of 4 high side switches, labeled as HSS. The switches are high voltage tolerant and are commonly attached to the same voltage supply as VSUP through the VHSS pin. The switches can act as a simple load switch where each switch can carry up to 100mA. All HSS outputs 1 through 4 can be accessed at header block J2. The HSS outputs can be shorted to allow for larger currents, if all 4 outputs are shorted up to 400mA of current can be delivered to an off-board load. Easy access to short outputs is located on header block J2. Each switch has multiple modes of operation as the switch can be turned off and on, controlled by PWM1 through PWM4, controlled by Timer1 or Timer2, or direct drive through WAKE3 pin with a fast or slow slew rate setting. HSS1 and HSS2 can be configured at register address 1Eh. HSS3 and HSS4 can be configured at register address 4Dh with additional configuration options for both located at 4Fh.

2.2.2 Transceiver Options

One of the most important aspects of the TCAN284XX/TCAN285XX line of SBCs is the ability to act as a communication node for multiple different standards depending on direct device variant. The families of devices can be thought of as CAN SBCs with options for CAN-SIC and LIN. The TCAN284XEVM is set up for all device variants and can support testing with all communication modes.

All devices in the TCAN284XX family are CAN and CAN-FD capable. The main configuration registers associated with the CAN bus are Ch (SBC configuration), 10h (CAN Control), and 44h (CAN/CAN-FD data rate). The CAN transceiver cannot be on in any other mode than normal mode. The suggestion is to either force the CAN transceiver to follow SBC mode in register 10h or switch the SBC to normal mode before turning on the CAN transceiver.

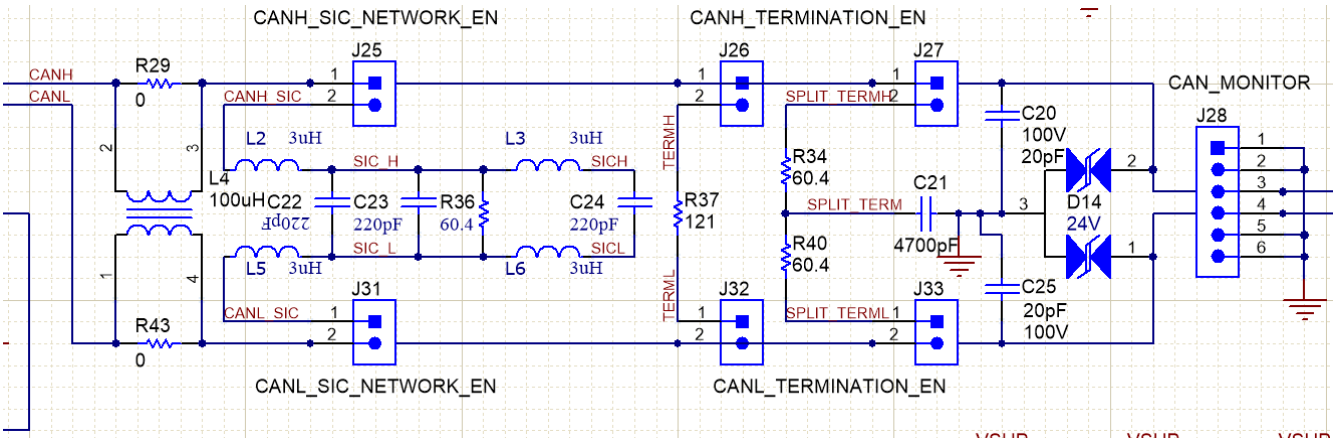


Figure 2-3. CAN Termination Styles Available on Board

The CAN bus on the TCAN284XEVM contains a common mode choke, pads for protection diodes and filtering caps, a CAN monitor, and three different termination styles. A standard resistive load, a split termination, and a SIC termination (only used on TCAN285XX devices). The split termination is employed to help mitigate issues from emissions by creating a low pass filter. To enable a standard termination on the CAN bus, J26 and J32 are shunted. For a split termination setup J27 and J33 are shunted instead. The CANL and CANH lines can be router externally through the CAN monitor header pins located at J28 or the CANH and CANL lines can be brought off-board through the DSUB-9 connector at J29. Single ended data for CAN is based on the CTXD and CRXD signals and are referenced to the ICs VCC1 level. The CTXD (transmit) and CRXD (receive) pins can be accessed through header block J30. While basic testing of the CAN bus can occur with a simple signal generator on these pins, for full scale CAN testing an external CAN controller must control the CTXD and CRXD pins.

For devices in the TCAN285XX family, most of the information remains the same as above. Except that the TCAN285XX family is CAN-SIC, which means that the recessive edge is driven unlike standard CAN. This can help mitigate issues due to ringing on the differential bus. The main difference when using the TCAN285XX family is that the termination style on the board is specific to SIC testing, so while the standard and split options are still available a specific SIC load can be applied by shunting J25 and J31.

In addition to CAN device, variants with the product number pattern of TCAN2847X/TCAN2857X are also LIN capable and the TCAN284XEVM allows for easy LIN usage in both responder and commander applications. The LIN transceiver can be configured at address 1Dh, similar to the CAN functionality the SBC must be in normal mode for the LIN bus to operate normally. LIN can be tied to SBC mode control similar to CAN functionality. The LIN bus contains a 220pF filter capacitor and a protection diode. The LIN bus can be access at the LIN monitor at J20, the external LIN header at J21, or through the DSUB-9 connector at J24. If the LIN node is a commander header J14 needs to be shunted to pull-up the node to battery supply voltage. Indicator LED D10 lights up when LIN bus drives low. The single ended pins are LTXD and LRXD and are referenced to devices VCC1 voltage level. These pins can be accessed through header block J30.

2.2.3 Special Use Pin Options

There are multiple special use pins on the TCAN284XX/TCAN285XX lines of devices that go beyond communication and power management. The pins are: the WAKEx pins, GFO pin, SW pin, LIMP Pin, nRST pin, and nINT pin.

The WAKEx pins (WAKE1, WAKE2, and WAKE3) are high voltage capable local wake-up pins. The pins can be configured to wake the device up from both rising and falling edge trigger. The pins can also be configured to wake up due to a pulse signal. By default, all the wake signals are active and set to watch for either rising or falling edge triggers. There are four primary registers to alter configurations of the WAKEx pins. These are the WAKE_PIN_CONFIG registers (1-4) - 11h, 12h, 2Ah, and 2Bh. These registers are where wake level, status, wake signal selection, and special features are accessed. The TCAN284XEVM allows for easy testing of Local Wake Ups (LWU) using the WAKEx pins. All three WAKEx signals are routed to J39 for easy access to connect the WAKEx signal to external sensor or other WAKEx signal source. The WAKEx signals can also be pulled up to either HSS4, VSUP, or VCC1 through J36 (WAKE1), J37 (WAKE2), J38 (WAKE3). When the WAKEx pins are pulled up to a supply voltage and S3, S4, or S5 are pushed, a high to low transition takes place on the WAKEx pin associated with the switch pressed. The last example shows static wake, but the WAKEx pins can also be used for cyclic sensing wake which minimizes current in sleep, In this mode, HSS4 periodically turns on, and the WAKEx with cyclic sensing wake selected and compares WAKEx state to previous state. If the states are different the SBC wakes up.

The WAKEx pins can also have some special features that go beyond a LWU, with WAKE1 and WAKE2 aiding battery monitoring applications and WAKE3 acting a direct drive source for controlling any of the HSS blocks available. For using WAKE1 and WAKE2 in aid of battery monitoring applications please see section *Potential Modifications* for more information as while this board does support Vbat monitoring. A few components must be added. For direct drive the HSSx pin that is to be controlled by WAKE3 needs to be configured for direct drive mode and then WAKE3 acts as an enable switch for the configured HSSx block.

The next special use pin is the GFO. This pin is truly a generic general-purpose output pin. To configure the pin, functionality can be accessed in register 29h. By default, the GFO pin is a simple output pin that can have the state modified through bit 4 in register 29h. The pin can also be used a specific interrupt flag including LDO

Error, WD error, LWU, Bus Wakeup Request (WUP), Restart Counter Exceeded, or a CAN bus fault flag. This pin can be accessed on header block J29.

Another special use pin is the SW pin, which has already been touched on in this document. This pin can be thought of as a prototyping/debug pin. During initial development is strongly suggested to hold SW pin in the active state until testing with the Watchdog (WD) begins. In the default state, holding the pin high disables watchdog actions. Meaning that the watchdog timer is still functioning but WD timer events do not cause related WD actions such as putting the device into a different functional mode. The pins active state can be changed to low. Another use of the SW pin is to work as a digital wake-up pin for the SBC while the SBC mode is in sleep mode. This offers a way at a system level to potentially wake the SBC from sleep by using SW as a digital wake up. The SW pin behavior can be modified at register address Eh. The SW pin, if not used for debug/development mode, can be accessed through header block J23.

The next special use pin is LIMP, the LIMP pin is for the limp home function and is an open-drain, active low, output. The pin is used for a limp home mode if the watchdog has timed out causing a reset. The pin is pulled up with an external resistor connected to the battery supply, VSUP. For the LIMP pin to be turned off, the watchdog error counter must reach zero from correct input triggers. If programmed any event that triggers the fail-safe mode also turns on the LIMP pin. The state of this pin can be read back by setting DEVICE_CONFIG register 8'h1A[6] LIMP_RD_EN to 1b. The state of the LIMP pin active (on) or inactive (off) can be read back from LIMP_STATE at 8'h1A[5]. The LIMP pin can be accessed through J15, and J15 can also be used to enable the LIMP indicator LED.

Next, the nRST pin. Which is a bi-directional open drain reset pin for the SBC. The pull-up resistor is integrated and pulled to VCC1. This pin watches for a high to low transition on the input when the device is not in restart mode and VCC1 is present. If a long enough pulse is detected, the device enters restart mode, EEPROM is reloaded, and any default configurations is reimplemented. When the device enters restart mode, the nRST pin pulls low to indicate to downstream devices the SBC is in restart mode. The amount of time the nRST pin is low depends on the method of entry into restart mode and if the LDO (VCC1) is active when device enters restart mode. This pin can be accessed on EVM through J11, and can be configured at register address 29h. S1 can be pressed to initiate a reset on the SBC.

Finally, the nINT pin. The pin flags the controller, or whatever device is connected to nINT pin, if there is an interrupt is generated by device operation. This signal can be accessed through J29 and is an active low flag.

2.2.4 Potential Board Modifications

The TCAN284XEVM provides a solid base to test most use cases without the need for modifying the board; however, there are 2 tests that can require some additional modifications which are Vbat monitoring and sleep current measurements.

As mentioned in the explanation of the WAKEx pins, WAKE1 and WAKE2 can be configured to support Vbat monitoring

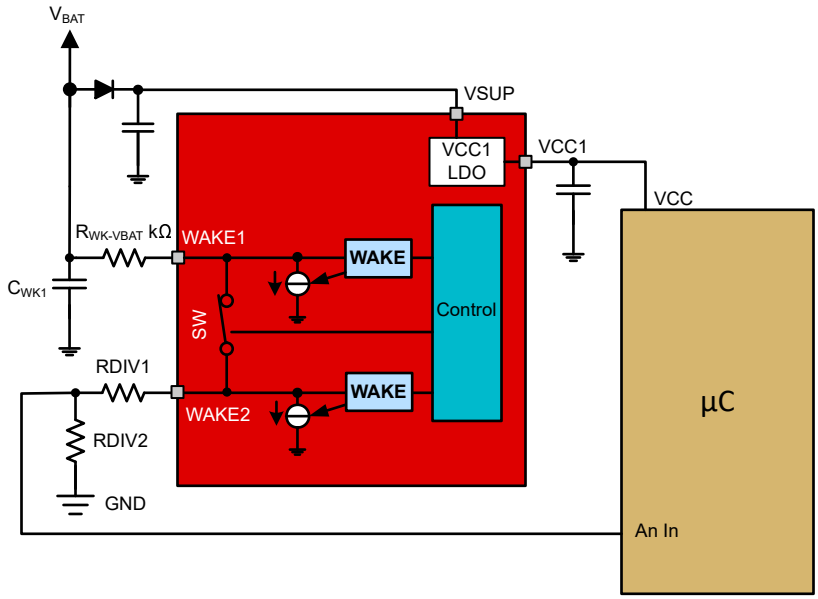


Figure 2-4. Vbat Monitoring Using WAKE1 and WAKE2

However, the default setup of the board does not include a properly sized R_WK-VBAT resistor (5.1k) or an RDIV2 resistor by default. However, by removing R67 and adding R14 the R_WK-VBAT resistor is situated correct and by adding R16 the RDIV2 voltage divider can be connected. If during testing, Vbat must never be reversed polarity, D25 can be shorted across; otherwise, D25 must be added as the WAKE1 pin is not capable of handling negative battery voltages.

The other potential modification is due to accurately measuring sleep current. If trying to accurately approximate the sleep current used by the specific SBC IC installed on board there are a few current sources that must be removed for most accurate results for SBC. U3 is used to power the LEDs on the circuit board as well as a few ICs. The EVM does not require U3 to be installed. To minimize current the end user can disable U3 by floating J12, but to completely remove U3s leakage from the system U3 must be removed and J12 must be left floating. Beyond the IC the MOSFETS Q2, Q3, and Q4 are all be removed (acting as LED drivers), but can draw small currents from SBC. In addition to the MOSFETS, R68 and R69 are also be removed. VHSS is left floating for VSUP sleep measurements unless VHSS is used in end application. If VHSS is used in end application remove R2, R3, R4, and R5. Removing these components minimizes non-SBC sleep current. While this can change in actual application, the individual result is more accurate if the above modifications are made.

2.3 Header, Jumper, and other Interface Information

Jumper ID	Function	Package	Comment	Installed?
J1	VSUP Diode Bypass	1x2 Header	Shunt to Bypass VSUP Diode	Yes
J2	HSS Outputs Header	2x4 Header	Output Connection point for HSS outputs	Yes
J3	Power Input Jack	Barrel Jack	Power Input	Yes
J4	Power Input Header	1x2 Header	Power input Header	Yes
J5	External VSUP Header	1x2 Header	Power input that skips diode and EMI filter	Yes
J6	VHSS Source Input	1x3 Header	Can Short VHSS to VSUP or GND and apply separate VHSS	Yes
J7	VCC1 External Output	1x2 Header	Can use to route VCC1 off board	Yes
J8	External 5V Connection point	1x2 Header	Can apply separate 5V signal when LDO (U3) is disabled	Yes
J9	VCAN Supply Input	1x3 Header	Can short to 5V LDO, VCC2 or external supply can be added	Yes

Jumper ID	Function	Package	Comment	Installed?
J10	VCAN External Input	1x2 Header	If using something other than 5V LDO or VCC2 to power VCAN apply signal to this header.	Yes
J11	nRST Shunt	1x2 Header	Shunt J11 to pull nRST low	Yes
J12	U3 LDO Enable Header	1x3 Header	Can Enable LDO from VSUP or VCC2 otherwise LDO is disabled	Yes
J13	VEXCC Output Header	1x2 Header	VEXCC Output Header can be used to bring VEXCC voltage off board	Yes
J14	LIN Commander Header	1x2 Header	Shunt when configured LIN node is a commander node – can ignore if LIN is responder node or unused	Yes
J15	LIMP Output Header	1x4 Header	Shunt pins J15-1 and J15-2 to enable LIMP LED and use pin J15-3 as external Output Header for LIMP signal	Yes
J16	HSS Load Sharing Header	2x4 Header	HSS(1-4) can be shorted to any other HSS, or multiple other HSS for load sharing applications.	Yes
J19	VEXCC +VCC1 Load Sharing Header	1x2 Header	For load sharing applications between VCC1 and VEXCC shunt J19	Yes
J20	LIN Monitor Header	1x3 Header	Can monitor LIN bus through pin J20-3 other pins are grounded	Yes
J21	LIN External Header	1x2 Header	External Header Output for LIN signal + GND	Yes
J22	VBAT to DSUB9 Header	1x2 Header	Shunt to allow VBAT (input at J3) to go to pin 9 of DSUB Connector (J24)	Yes
J23	SW Pin PU/PD Selector	1x3 Header	Shunt J12-1 to J12-2 to pull up SW pin and shunt J12-2 to J12-3 to pull down SW pin.	Yes
J24	DSUB-9 Connector	DSUB-9	DSUB port is used to transmit CANH, CANL, LIN, VBAT, and GND off board.	Yes
J25	CANH SIC Network Enable	1x2 Header	Shunt to implement a CAN-SIC load on CANH line – for use with TCAN285XX devices (CAN-SIC Capable). If Shunted J31 must also be shunted	Yes
J26	CANH Standard Termination Enable	1x2 Header	Shunt to Connect CANH to one side of standard 121 Ohm resistor (R37). If shunted J32 must also be shunted	Yes
J27	CANH Split Termination Enable	1x2 Header	Shunt to Connect CANH to one side of a split termination network. If shunted, J33 must also be shunted.	Yes
J28	CAN Monitor	1x6 Header	CAN Header pins J28-3 is CANH and J28-4 is CANL – the rest of the pins are GND	Yes
J29	External MCU Connection Point	2x7 Header	External Connection points for SW, GFO, nINT, and SPI pins (SDI, SDO, SCK, nCS)	Yes

Jumper ID	Function	Package	Comment	Installed?
J30	LIN/CAN Controller Connection Point	2x4 Header	Input Headers for CRXD, CTXD, LTXD, and LRXD – which are logic I/O for CAN and LIN respectively.	Yes
J31	CANL SIC Network Enable	1x2 Header	Shunt to Implement a CAN SIC load on CANL Line – for use with TCAN285XX devices (CAN-SIC Capable). If Shunted J25 must also be shunted.	Yes
J32	CANL Standard Termination Enable	1x2 Header	Shunt to Connect CANL to one side of standard 121 Ohm resistor (R37). If shunted J26 must also be shunted	Yes
J33	CANL Split Termination Enable	1x2 Header	Shunt to Connect CANL to one side of a split termination network. If shunted, J27 must also be shunted.	Yes
J34	VCC2 External Output Header	1x2 Header	Can be used to route VCC2 off board.	Yes
J35	Channel Expansion Interface	2x8 2.54mm Receptacle	Can be used to route power and wake signals off board.	Yes
J36	WAKE1 Pull-Up Source Selection	2x3 Header	Pull-Up Source: Shunt J36-1 to J36-2: HSS4 Shunt J36-3 to J36-4: VSUP Shunt J36-5 to J36-6: VCC1	Yes
J37	WAKE2 Pull-Up Source Selection	2x3 Header	Pull-Up Source: Shunt J37-1 to J37-2: HSS4 Shunt J37-3 to J37-4: VSUP Shunt J37-5 to J37-6: VCC1	Yes
J38	WAKE3 Pull-Up Source Selection	2x3 Header	Pull-Up Source: Shunt J38-1 to J38-2: HSS4 Shunt J38-3 to J38-4: VSUP Shunt J38-5 to J38-6: VCC1	Yes
J39	WAKE Output Header	2x3 Header	Can be used to route WAKE1, WAKE2, or WAKE3 signal path off board.	Yes
J40	VUSB to PUR Header	1x2 Header	Shunt J40 to have U2 perform a PUR.	Yes
J41	Mini-USB-B Input Jack	Mini USB-B	For MSP430 – not relevant to most Board Functions	Yes
J42	JTAG Output Header	2x7 Header	For MSP430 – not relevant to most Board Functions	Yes
J43	5V USB LDO (U9) Output Header	1x2 Header	Can be used to bring 5V USB Output off board	Yes
J44	3.3V USB LDO (U10) Output Header	1x2 Header	Can be used to bring 3.3V USB Output off board	Yes

2.4 Switch Information

Switch ID	Purpose	Type	Comment	Installed
S1	SBC Reset Switch	Push Button	Push to Cause Reset on SBC	Yes
S2	MCU to SPI Bus Switch	Dip Switch Array	Close all switches to connect to MCU. Open all switches for external control.	Yes
S3	WAKE1 Switch	Push Button	If J36 is shunted to pull-up source pushing button will create a high to low transition on WAKE1	Yes
S4	WAKE2 Switch	Push Button	If J37 is shunted to pull-up source pushing button will create a high to low transition on WAKE2	Yes
S5	WAKE3 Switch	Push Button	If J38 is shunted to pull-up source pushing button will create a high to low transition on WAKE3	Yes
S6	MCU Reset Switch	Push Button	Push to Reset MSP430 (U2)	Yes

2.5 Resistor Information

Resistor ID	Purpose	Comment	Installed
R1	LED Current Limiting Resistor	N/A	Yes
R2	LED Current Limiting Resistor	N/A	Yes
R3	LED Current Limiting Resistor	N/A	Yes
R4	LED Current Limiting Resistor	N/A	Yes
R5	LED Current Limiting Resistor	N/A	Yes
R6	U3 Enable Pull-up resistor for VCC2	N/A	Yes
R7	U3 Enable Pull-up resistor for VSUP	N/A	Yes
R8	LED Current Limiting Resistor	N/A	Yes
R9	Input Resistance for nRST LED Buffer	N/A	Yes
R10	Weak (100k) Pull-down on U3 Enable	If J12 is left floating R10 prevents U3-2 (EN) from floating	Yes
R11	LIN Commander Pull-up	Only Connects to LIN bus if J14 is shunted	Yes
R12	0 Ohm Resistor on VEXCC Path	N/A	Yes
R13	LIMP bus Pull-up to VSUP	N/A	Yes
R14	VBAT to Wake One Input Resistance	Used for VBAT monitoring applications	No
R15	0 Ohm Resistor on LIMP Path	N/A	Yes
R16	Pull-down Resistor on WAKE2	N/A	No
R18	0 Ohm Resistor between VEXCTRL and base pin of PNP Q1	N/A	Yes
R19	0 Ohm resistor on HSS1	N/A	Yes
R20	0 Ohm Resistor on HSS2	N/A	Yes
R22	VSUP to VEXMON Shunt Resistor	N/A	Yes
R23	0 Ohm resistor on HSS3	N/A	Yes
R24	0 Ohm Resistor on HSS4	N/A	Yes
R25	0 Ohm Resistor between VEXMON and Collector of PNP Q1	N/A	Yes

Resistor ID	Purpose	Comment	Installed
R26	0 Ohm Resistor between LIN bus and DB-9 Connector	N/A	Yes
R28	SW Pull-up Resistor	N/A	Yes
R29	CMC Bypass on CANH 0 Ohm resistor	N/A	No
R30	SW Pull-down Resistor	N/A	Yes
R31	0 Ohm Series Resistor on SCK Pin	N/A	Yes
R32	0 Ohm Series Resistor on SDI Pin	N/A	Yes
R33	0 Ohm Series Resistor on SDO Pin	N/A	Yes
R34	CANH Split Termination Resistor	N/A	Yes
R35	0 Ohm Series Resistor on nCS Pin	N/A	Yes
R36	Resistor in CAN-SIC Load	For TCAN285XX Devices	Yes
R37	Standard CAN Termination Resistor	N/A	Yes
R38	0 Ohm Series Resistor on LTXD Pin	N/A	Yes
R39	0 Ohm Series Resistor on LRXD Pin	N/A	Yes
R40	CANL Split Termination Resistor	N/A	Yes
R41	0 Ohm Series Resistor on CTXD Pin	N/A	Yes
R42	0 Ohm Series Resistor on CRXD Pin	N/A	Yes
R43	CMC Bypass for CANL 0 Ohm resistor	N/A	No
R44	Resistive Connection between Earth and GND on DB-9 Connector	N/A	Yes
R45	LED Current Limiting Resistor	N/A	Yes
R46	LED Current Limiting Resistor	N/A	Yes
R47	LED Current Limiting Resistor	N/A	Yes
R48	LED Current Limiting Resistor	N/A	Yes
R49	LED Current Limiting Resistor	N/A	Yes
R50	LED Current Limiting Resistor	N/A	Yes
R51	HSS4 to WAKE1 Pull-Up Resistor	N/A	Yes
R52	VSUP to WAKE1 Pull-Up Resistor	N/A	Yes
R53	VCC1 to WAKE1 Pull-Up Resistor	N/A	Yes
R54	HSS4 to WAKE2 Pull-Up Resistor	N/A	Yes
R55	VSUP to WAKE2 Pull-Up Resistor	N/A	Yes
R56	VCC1 to WAKE2 Pull-Up Resistor	N/A	Yes
R57	HSS4 to WAKE3 Pull-Up Resistor	N/A	Yes
R58	VSUP to WAKE3 Pull-Up Resistor	N/A	Yes
R59	VCC1 to WAKE3 Pull-Up Resistor	N/A	Yes
R60	0 Ohm Series Resistor on WAKE2 for Channel Expansion	N/A	Yes
R61	0 Ohm Series Resistor on WAKE1 for Channel Expansion	N/A	Yes
R62	0 Ohm Series Resistor on HSS4 for Channel Expansion	N/A	Yes

Resistor ID	Purpose	Comment	Installed
R63	0 Ohm Series Resistor on WAKE3 for Channel Expansion	N/A	Yes
R64	0 Ohm Series Resistor on LIMP for Channel Expansion	N/A	Yes
R65	LED Current Limiting Resistor	N/A	Yes
R66	LED Current Limiting Resistor	N/A	Yes
R67	WAKE1 3.3k Series Resistance	N/A	Yes
R68	Voltage Divider Resistor for LED Control NFET	N/A	Yes
R69	Voltage Divider Resistor for LED Control NFET	N/A	Yes
R70	Additional Gate Input Resistance for LED Control NFET	N/A	Yes
R71	Additional Gate Input Resistance for LED Control NFET	N/A	Yes
R72	Additional Gate Input Resistance for LED Control NFET	N/A	Yes
R73	Additional Gate Input Resistance for LED Control NFET	N/A	Yes
R74	WAKE2 3.3k Series Resistance	N/A	Yes
R75	WAKE3 3.3k Series Resistance	N/A	Yes
R76	Voltage Divider Resistor for LED Control NFET	N/A	Yes
R77	Voltage Divider Resistor for LED Control NFET	N/A	Yes
R78	nINT LED Buffer Input Resistance	N/A	Yes
R79	GFO LED Buffer Input Resistance	N/A	Yes
R80	MSP430 (U2) PUR Pull-down Resistor	N/A	Yes
R81	D+ (J41) to MSP430 (U2) PUR Resistance	N/A	Yes
R82	D- (J41) series Damping Resistor	N/A	Yes
R83	D+ (J41) series Damping Resistor	N/A	Yes
R84	USB to Board Ground Resistance	N/A	Yes
R85	MSP430 (U2) RST Pull-Up Resistor	N/A	Yes
R86	Current Limit Setting Resistor	N/A	Yes
R87	U9 Enable Pull-Down Resistor	N/A	Yes
R88	Current Limit Setting Resistor	N/A	Yes
R89	U10 Enable Pull-Down Resistor	N/A	Yes
R94	MSP430 (U2) XIN 0 Ohm Series Resistor	N/A	Yes
R95	MSP430 (U2) XOUT 0 Ohm Series Resistor	N/A	Yes
R102	LDO (U3) Feedback Network Resistor	N/A	Yes
R103	LDO (U3) Feedback Network Resistor	N/A	Yes
R108	LED Current Limiting Resistor	N/A	Yes

2.6 Inductance Information

Inductance ID	Function	Comment	Installed
L1	VBAT EMI Filter Inductor	N/A	Yes
L2	CAN-SIC Load Inductance	TCAN285XX Devices Only	Yes
L3	CAN-SIC Load Inductance	TCAN285XX Devices Only	Yes
L4	CAN Bus Common Mode Choke (CMC)	N/A	Yes
L5	CAN-SIC Load Inductance	TCAN285XX Devices Only	Yes
L6	CAN-SIC Load Inductance	TCAN285XX Devices Only	Yes
L7	VBUS (USB) Ferrite Bead	N/A	Yes

2.7 Capacitor Information

Capacitor ID	Function	Comment	Installed
C1	VSUP Decoupling Capacitor	N/A	Yes
C2	VBAT EMI Filter Capacitor	Electrolytic	Yes
C3	VBAT EMI Filter Capacitor	N/A	Yes
C4	HSS1 Decoupling Capacitor	N/A	Yes
C5	HSS2 Decoupling Capacitor	N/A	Yes
C6	HSS3 Decoupling Capacitor	N/A	Yes
C7	HSS4 Decoupling Capacitor	N/A	Yes
C8	VHSS Decoupling Capacitor	N/A	Yes
C9	VHSS Decoupling Capacitor	N/A	Yes
C10	U4 VCC Decoupling Capacitor	N/A	Yes
C11	U3 Input Bulk Capacitance	N/A	Yes
C12	VCC1 Output Bulk Capacitance	N/A	Yes
C13	U3 Output Bulk Capacitance	N/A	Yes
C14	VCAN Decoupling Capacitance	N/A	Yes
C15	VCAN Decoupling Capacitance	N/A	Yes
C16	S1 Parallel Capacitance	N/A	Yes
C17	VEXCC Output Bulk Capacitance	N/A	Yes
C18	VBAT Monitoring Capacitance	Must Install for VBAT monitoring	No
C19	LIN Bus Filter Capacitor	N/A	Yes
C20	CANH Filter Capacitor	N/A	No
C21	CAN Split Termination Capacitor	N/A	Yes
C22	CAN-SIC Load Capacitor	TCAN285XX Devices Only	Yes
C23	CAN-SIC Load Capacitor	TCAN285XX Devices Only	Yes
C24	CAN-SIC Load Capacitor	TCAN285XX Devices Only	Yes
C25	CANL Filter Capacitor	N/A	No
C26	DSUB-9 (J24) GND Capacitance	N/A	Yes
C27	VCC2 Output Bulk Capacitance	N/A	Yes
C28	U5 Decoupling Capacitor	N/A	Yes
C29	U6 Decoupling Capacitor	N/A	Yes

Capacitor ID	Function	Comment	Installed
C30	WAKE1 Capacitor	N/A	Yes
C31	WAKE2 Capacitor	N/A	Yes
C32	WAKE3 Capacitor	N/A	Yes
C33	VUSB Decoupling Capacitor	N/A	Yes
C34	VBUS (USB) Decoupling Capacitor	N/A	Yes
C35	U2 VEREF+ Decoupling Capacitor	N/A	Yes
C36	Crystal Y1 Capacitance	N/A	Yes
C37	Crystal Y1 Capacitance	N/A	Yes
C38	U9 and U8 Input Bulk Capacitance	N/A	Yes
C39	U9 Output Bulk Capacitance	N/A	Yes
C40	VBUS Bulk Capacitance	Electrolytic	Yes
C41	U2 RST Timer Capacitance	N/A	Yes
C42	U2 V18 Decoupling Capacitance	N/A	Yes
C43	U2 VCORE Decoupling Capacitance	N/A	Yes
C44	U8 Output and U10 Input Bulk Capacitance	N/A	Yes
C45	U10 Output Bulk Capacitance	N/A	Yes
C46	U2 Supply Decoupling Capacitor	N/A	Yes
C47	U8 HF Bypass Capacitor	N/A	Yes
C52	U2 Supply Decoupling Capacitor	N/A	Yes
C53	U2 Supply Decoupling Capacitor	N/A	Yes

2.8 Diode Information

Diode ID	Function	Comment	Installed
D1	VBAT Input Protection Diode	N/A	Yes
D2	VSUP Reverse Polarity Protection Diode	N/A	Yes
D3	LED Indicator for nRST Signal	Super Red LED	Yes
D4	U3 Output Protection Diode	N/A	Yes
D5	HSS1 LED Indicator	Green LED	Yes
D6	HSS2 LED Indicator	Green LED	Yes
D7	HSS3 LED Indicator	Green LED	Yes
D8	HSS4 LED Indicator	Green LED	Yes
D9	VCC1 Output Protection Diode	N/A	Yes
D10	LIN Pull-Up Reverse Polarity Protection Diode	N/A	Yes
D11	LIMP LED Indicator	Super Red LED	Yes
D12	VEXCC Output Protection Diode	N/A	Yes
D13	LIN Bus Protection Diode	N/A	Yes
D14	CAN Bus Line Protection Diode Array	N/A	No
D15	VCC2 Output Protection Diode	N/A	Yes
D16	VSUP Indicator LED	Green LED	Yes
D17	VHSS Indicator LED	Green LED	Yes

Diode ID	Function	Comment	Installed
D18	VEXCC Indicator LED	Green LED	Yes
D19	VCC1 Indicator LED	Green LED	Yes
D20	VCAN Indicator LED	Green LED	Yes
D21	VCC2 Indicator LED	Green LED	Yes
D22	nINT Indicator LED	Super Red LED	Yes
D23	GFO Indicator LED	Green LED	Yes
D24	VBUS (USB) Protection Diode	N/A	Yes
D25	VBAT Monitoring Diode	Must Install for VBAT Monitoring Applications	No
D29	U3 Output Indicator LED	N/A	Yes

2.9 Transistor Information

Transistor ID	Function	Comment	Installed
Q1	External PNP BJT for VEXCC Applications	N/A	Yes
Q2	LED Indicator Driver Dual Channel N-MOSFET	Drives D16 + D17	Yes
Q3	LED Indicator Driver Dual Channel N-MOSFET	Drives D18 + D19	Yes
Q4	LED Indicator Driver Dual Channel N-MOSFET	Drives D20 + D21	Yes

2.10 IC and Misc. Component Information

Component ID	Component GPN	Function	Comment	Installed
U1	TCAN28475	Main EVM SBC	Footprint compatible with all other TCAN284XX and TCAN285XX IC's	Yes
U2	MSP430F5529	External MCU	Not Needed For TCAN28 testing	Yes
U3	TPS7B8650	Additional 5V LDO	Used to drive LEDs and provide pull-up voltage to SW pin	Yes
U4	SN74LVC1G07	Buffer for LED Driving	Only Used for Driving LEDs	Yes
U5	SN74LVC1G07	Buffer for LED Driving	Only Used for Driving LEDs	Yes
U6	SN74LVC1G07	Buffer for LED Driving	Only Used for Driving LEDs	Yes
U9	TPS2553	USB to 5V LDO	U2 Power Rail	Yes
U10	TPS2553	USB to 3.3V LDO	U2 Power Rail	Yes
Y1	ABM11-24.000MHZ-D2X-T3	25MHz clock for U2	N/A	Yes

3 Software

3.1 Software Description

This device or EVM does not need direct software. Software interaction with this device is limited to register configurations through external controller and SPI communication. Board is by default in SPI mode 0 with 4 wire SPI, one byte transactions, with no CRC byte. This can be changed in subsequent configurations, but first the configuration must be done according to devices initial conditions.

3.2 Software Installation

No software is needed to be installed for operating with this device. The only software needed is hosted on external controller interfacing through devices SPI bus pins, nCS, SDO, SDI, and SCK.

3.3 Software Development

For full testing it is advised to get a controller that can handle 4-wire SPI in mode 0. There are four pins that need to be accessed at a minimum for SPI on the TCAN284XEVM. These are SDO (serial data out), SDI (serial data in), SCK (Serial Clock), and nCS (active low chip select) this pins can be accessed through header block J29. To connect the EVM to a 4-wire SPI capable controller, SDO should connect to the controllers data input pin. SDI should connect to controllers data output pin. SCK should connect to SPI clock on controller. The suggestion is that a minimum of 1MHz is used for SPI speed, and nCS is connected to nCS. The TCAN284XX and TCAN285XX devices are by default in mode 0 for SPI. Meaning the clock polarity is default low, and data is sampled on the rising edge and shifted on the falling edge. The user can change the device to SPI modes 1, 2, or 3, but the initial configuration must be done in mode 0. By default, the TCAN284XX and TCAN285XX devices are in one byte transaction mode with no CRC. Meaning there are 16 clock pulses per SPI transaction. For read commands, both SDO and SDI act a bit differently. The SDI pin should be given a 7 bit address and a 0 bit to indicate a read followed by nothing else for the rest of the transaction. SDO immediately starts outputting the 8-bit global interrupt vector. The address is simultaneously sent to SDI pin. After the global interrupt data has been transmitted out of the SDO pin, the request register data follows. Data is transmitted MSB.

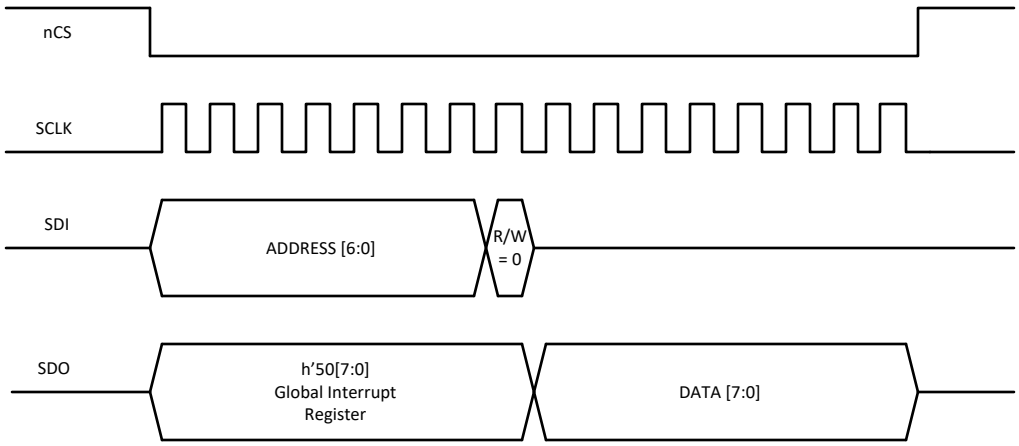


Figure 3-1. SPI Read - One Byte Mode

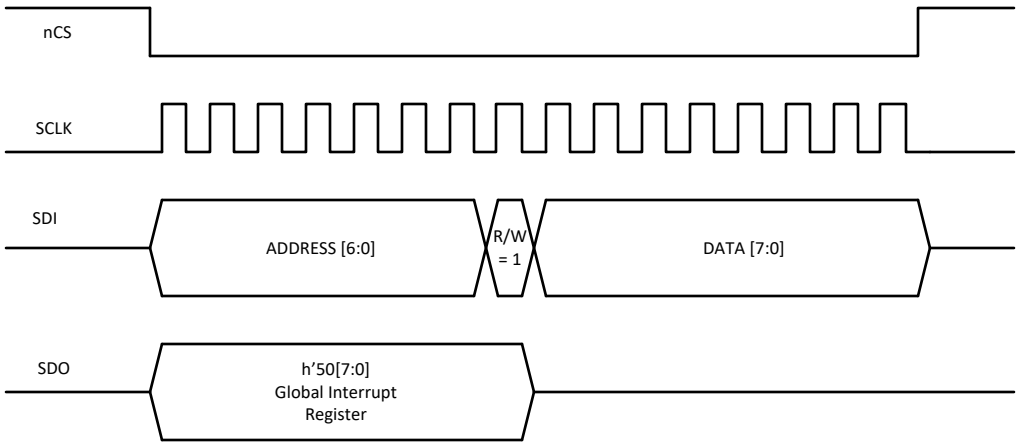


Figure 3-2. SPI Write - One Byte Mode

To verify a valid SPI connection there are two tests to perform, an ID validation test and a SPI Scratch Pad test. For prototyping and debugging purposes, the suggestion is holding SW high to prevent the watchdog from putting the device to sleep when prototyping. After the board powers up and reaches standby mode, the SPI tests can commence. The first test is reading the ID registers of the specific TCAN284XX/TCAN285XX device on board. There are 8 ID registers on these devices starting at address 0h and going through address 7h. The registers are read only so the data is constant and always known. For example, if validating the TCAN28475 the 8 registers reads back 0x54, 0x43, 0x41, 0x32, 0x38, 0x34, 0x37, 0x35 from ID registers 0h through 7h. For specific device ID, please see DEVICE_ID_y register table in respective devices data sheet. If the ID is valid after read, two things have been confirmed: SPI Read works and device is giving expected ID. The next test checks both the SPI read and write capabilities by using the Scratch_Pad_SPI register located at address Fh. This register has no other purpose than debugging SPI. The register is read/write accessible, and the register contents has no impact on any other device functionality. So, reading/writing does not change device in any way. To perform the second test, there are multiple read and write conditions that should be performed consecutively. The process is to read the scratch pad register, verify the value is as expected, then write a new value. This process repeats a few times. A suggested flow uses the following steps:

1. Read: Verify address Fh contains 0x00 (default condition)
2. Write: Write byte 0x55 to address Fh
3. Read: Verify address Fh contains 0x55
4. Write: Write byte 0xAA to address Fh
5. Read: Verify address Fh contains 0xAA
6. Write: Write byte 0xFF to address Fh
7. Read: Verify address Fh contains 0xFF
8. Write: Write byte 0x00 to address Fh
9. Read: Verify address Fh contains 0x00

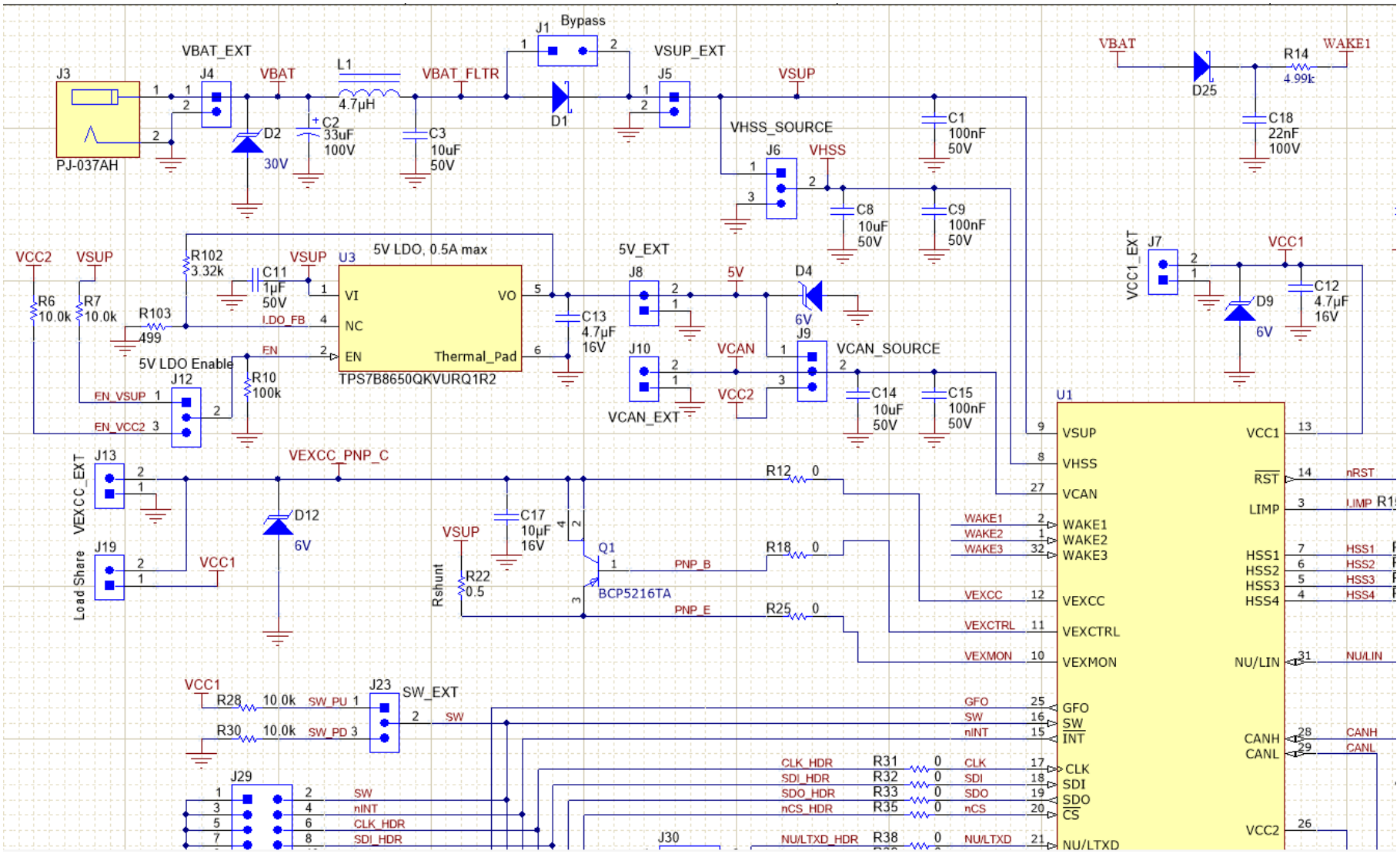
If this test is completed successfully, where success is accurate data reads and writes, then the SPI bus is ready for communication. Further configurations can be written to device if non-default operation is desired. Please refer to specific device data sheet for full register mapping.

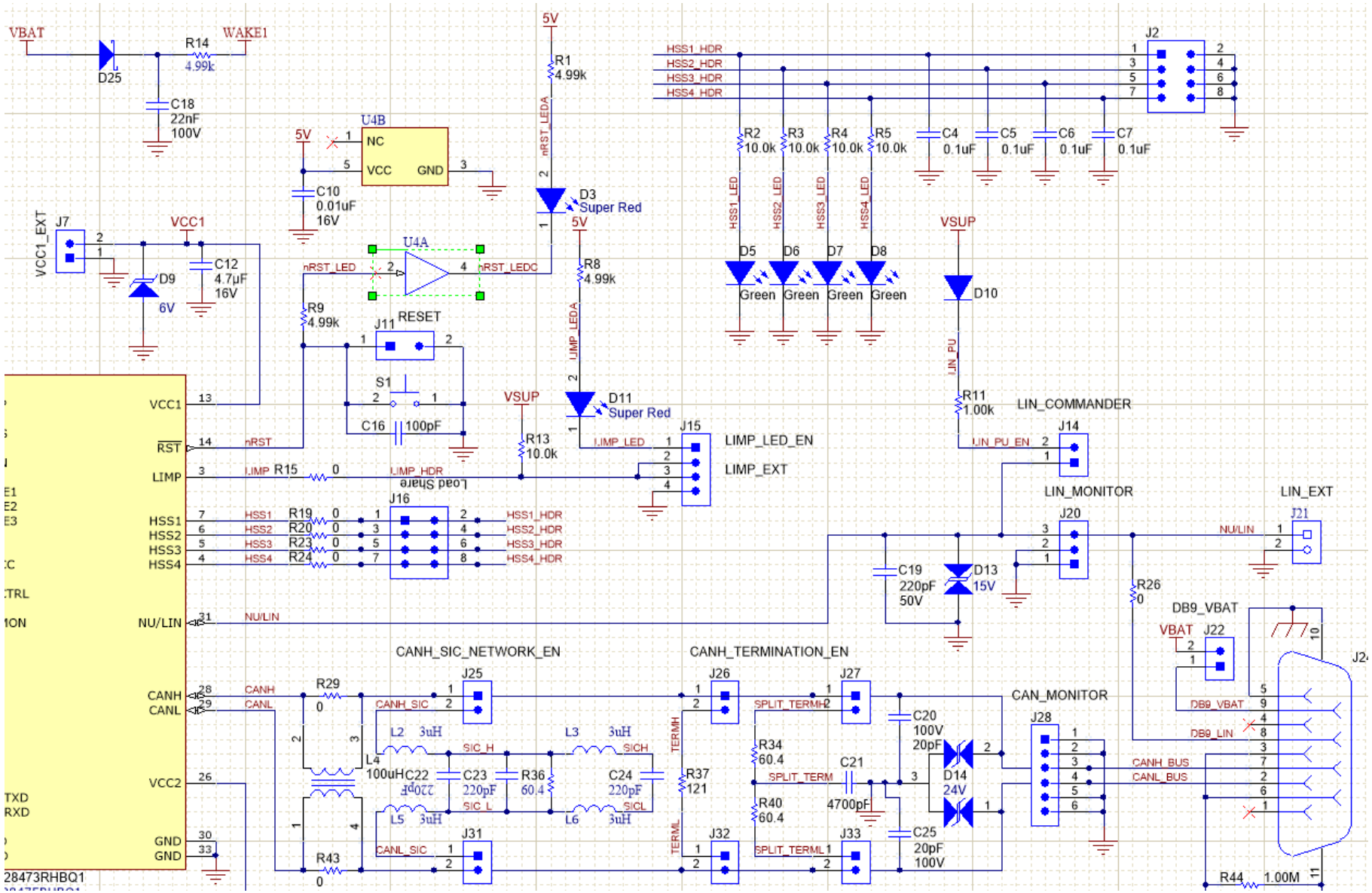
3.4 Programming Options

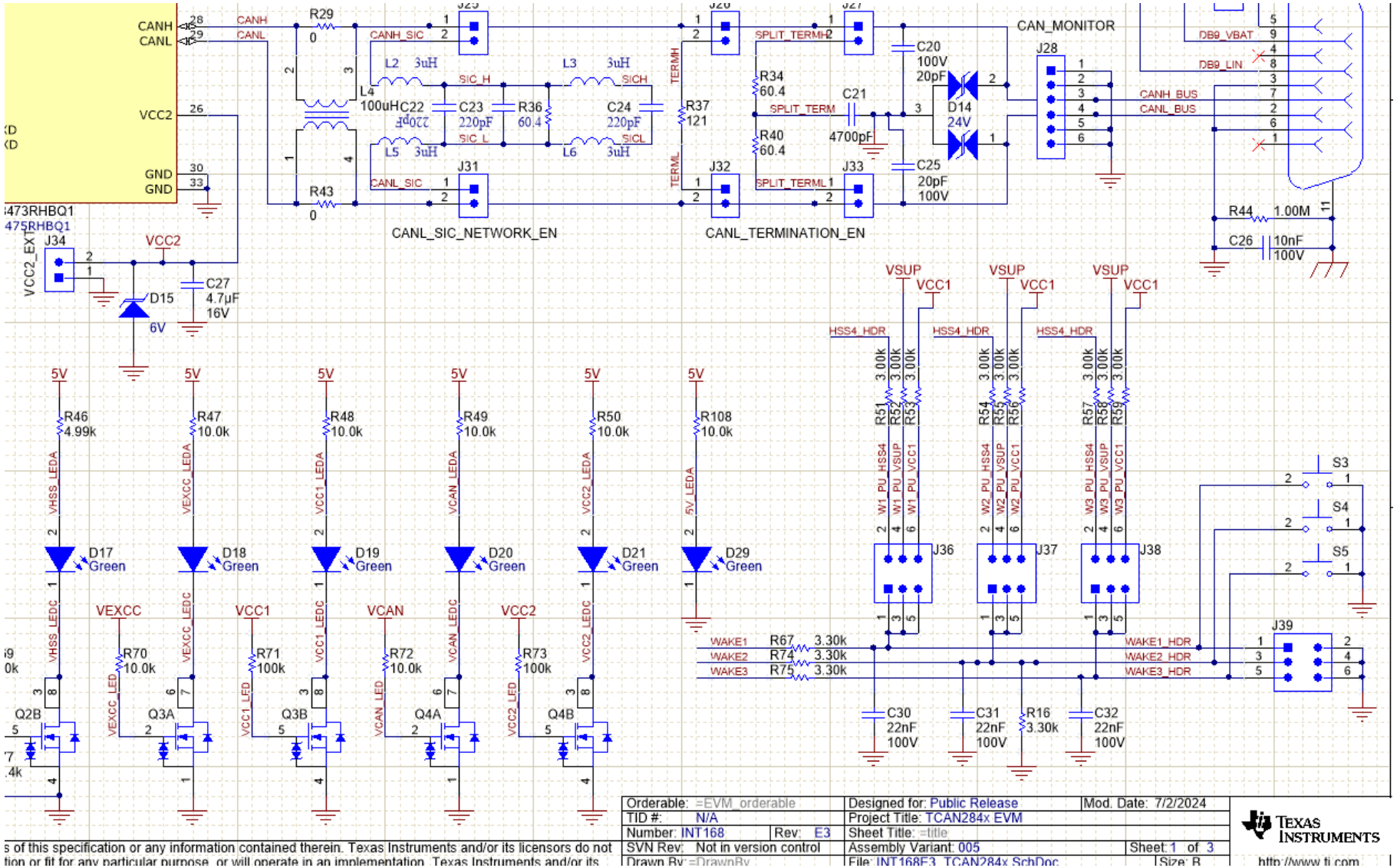
Program device through SPI bus interface (nCS, SDO, SDI, and SCK) accessed through header block J29.

4 Hardware Design Files

4.1 Schematics







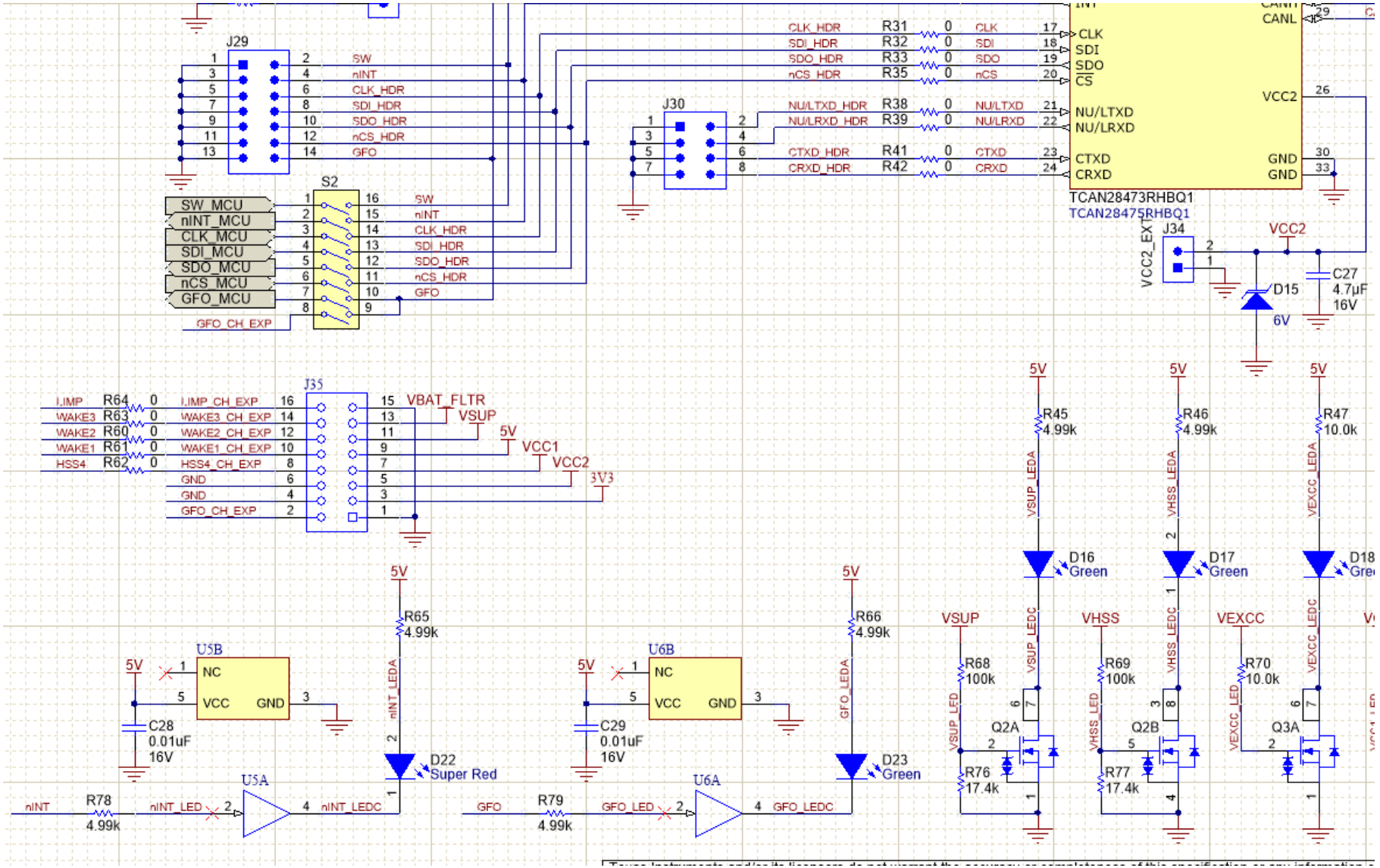
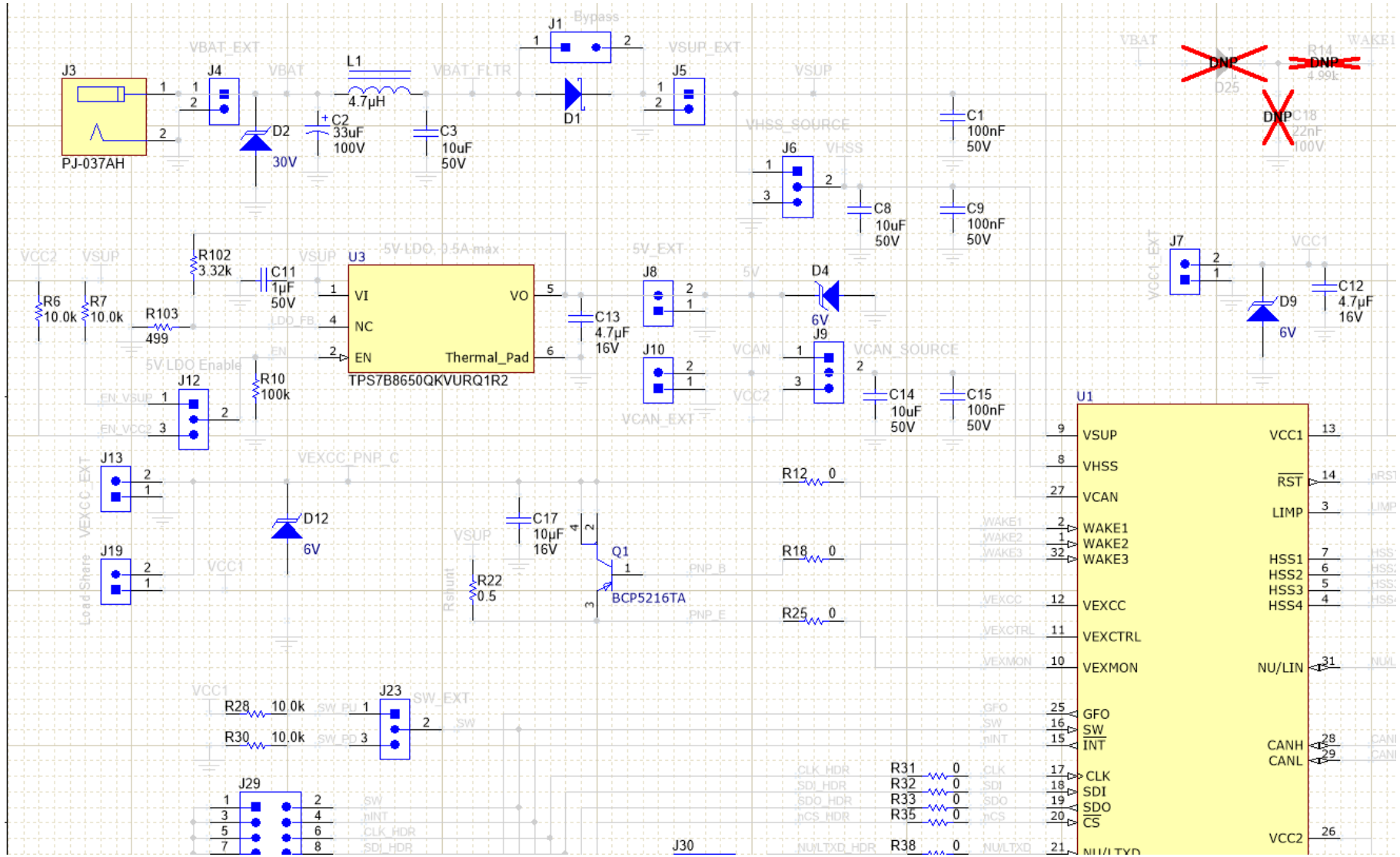
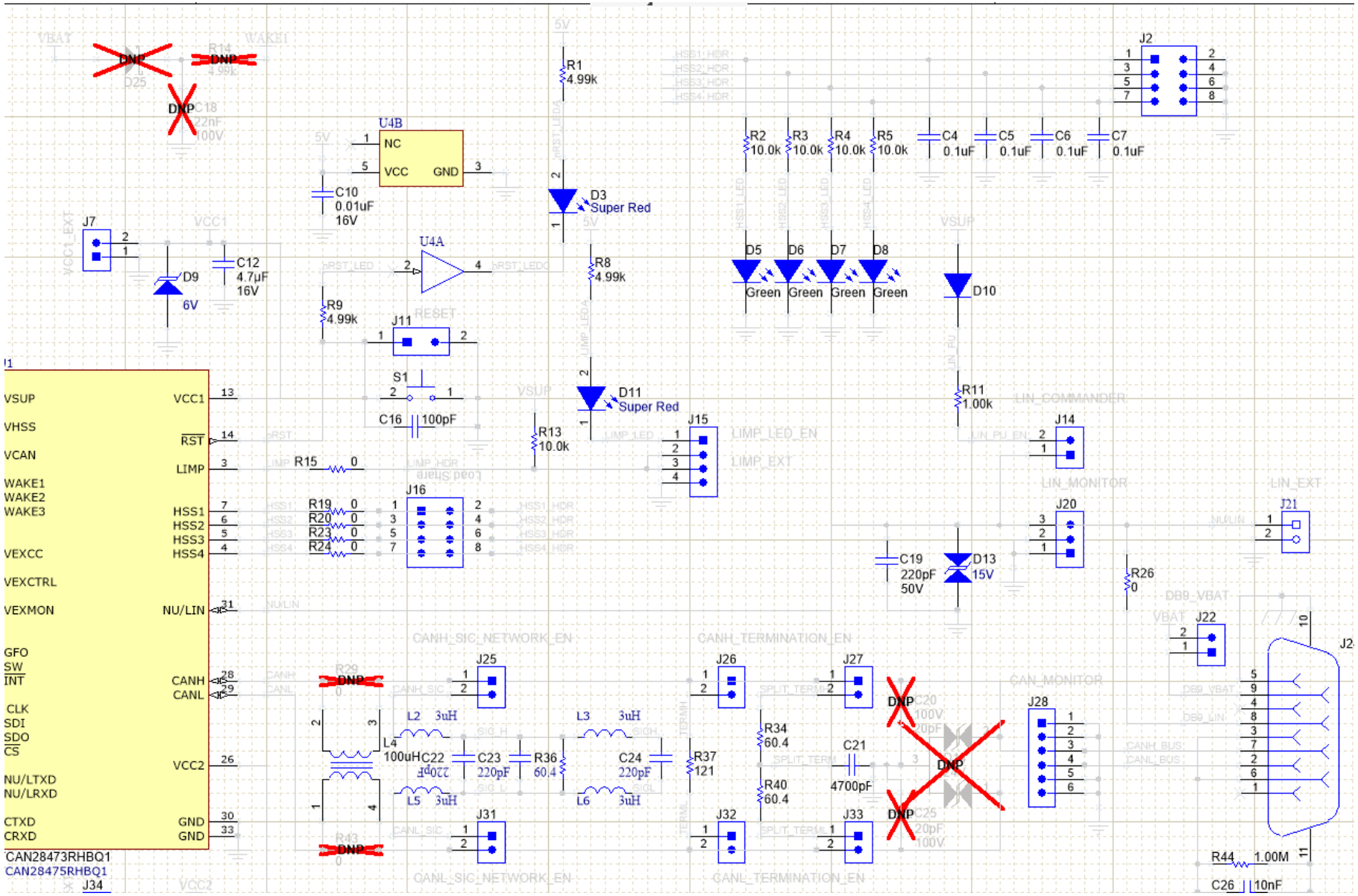
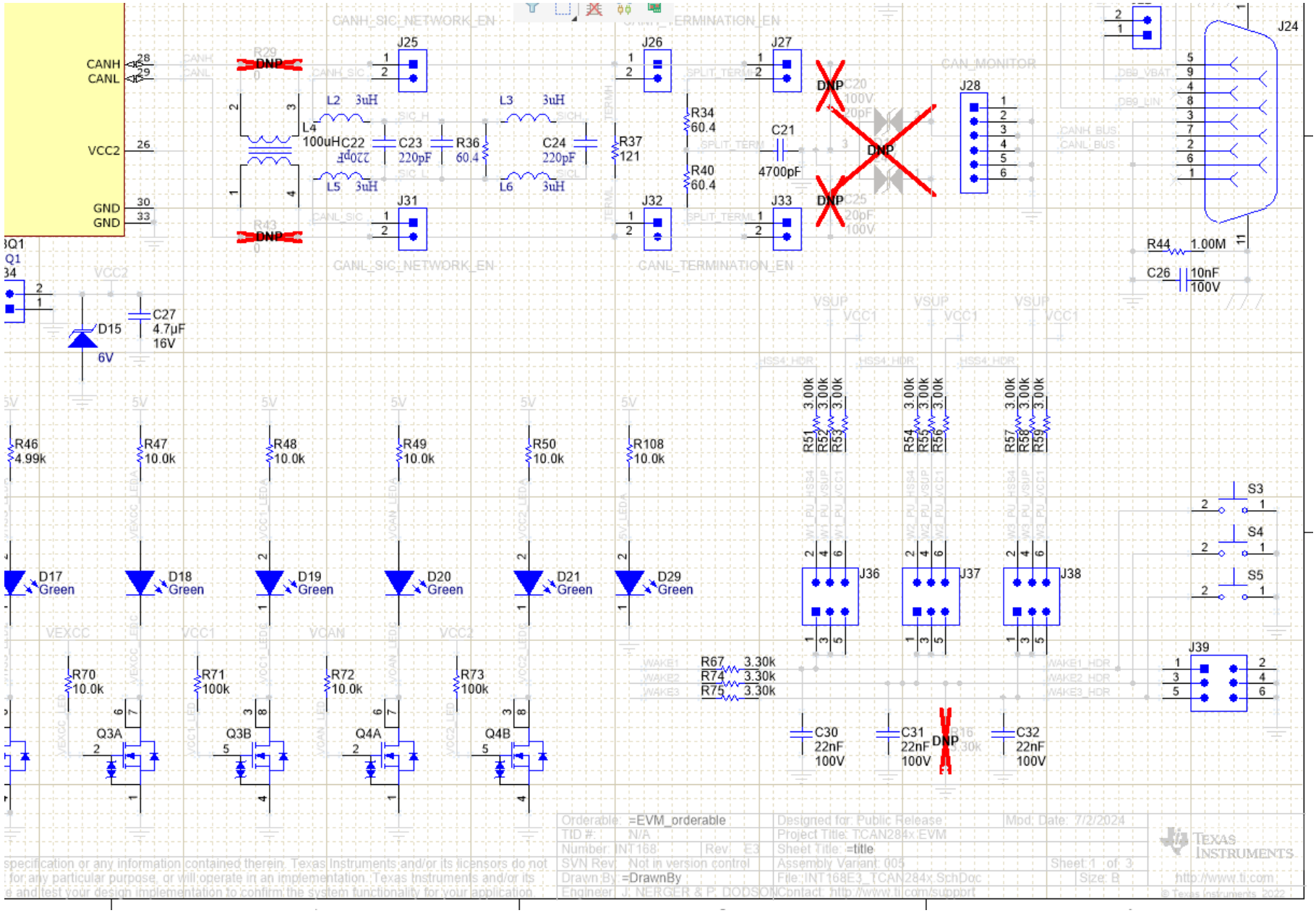


Figure 4-1. Generic Schematic - Showing all Components







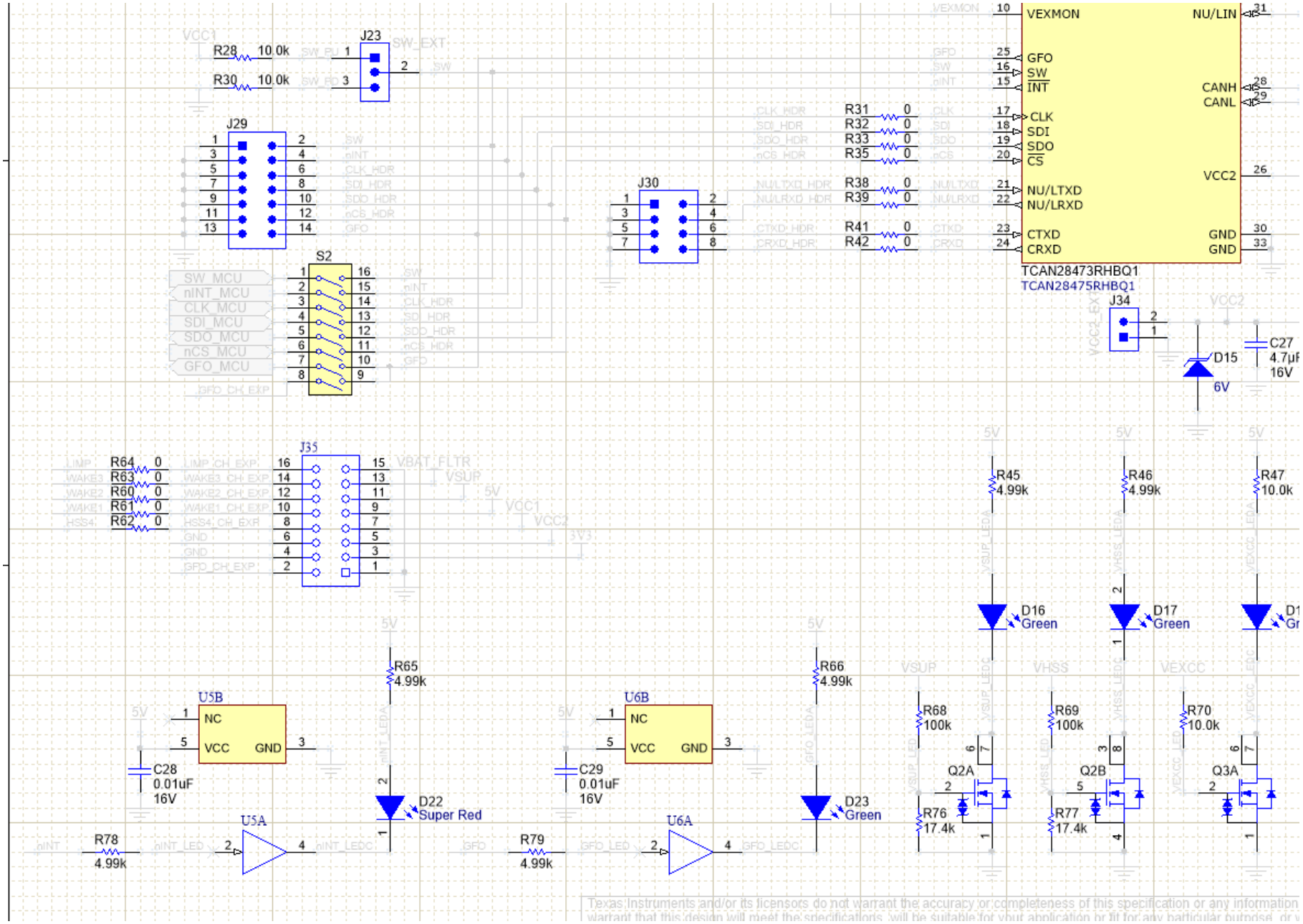


Figure 4-2. Out of Box Schematic - With DNI'd Components Crossed Out

4.2 PCB Layouts

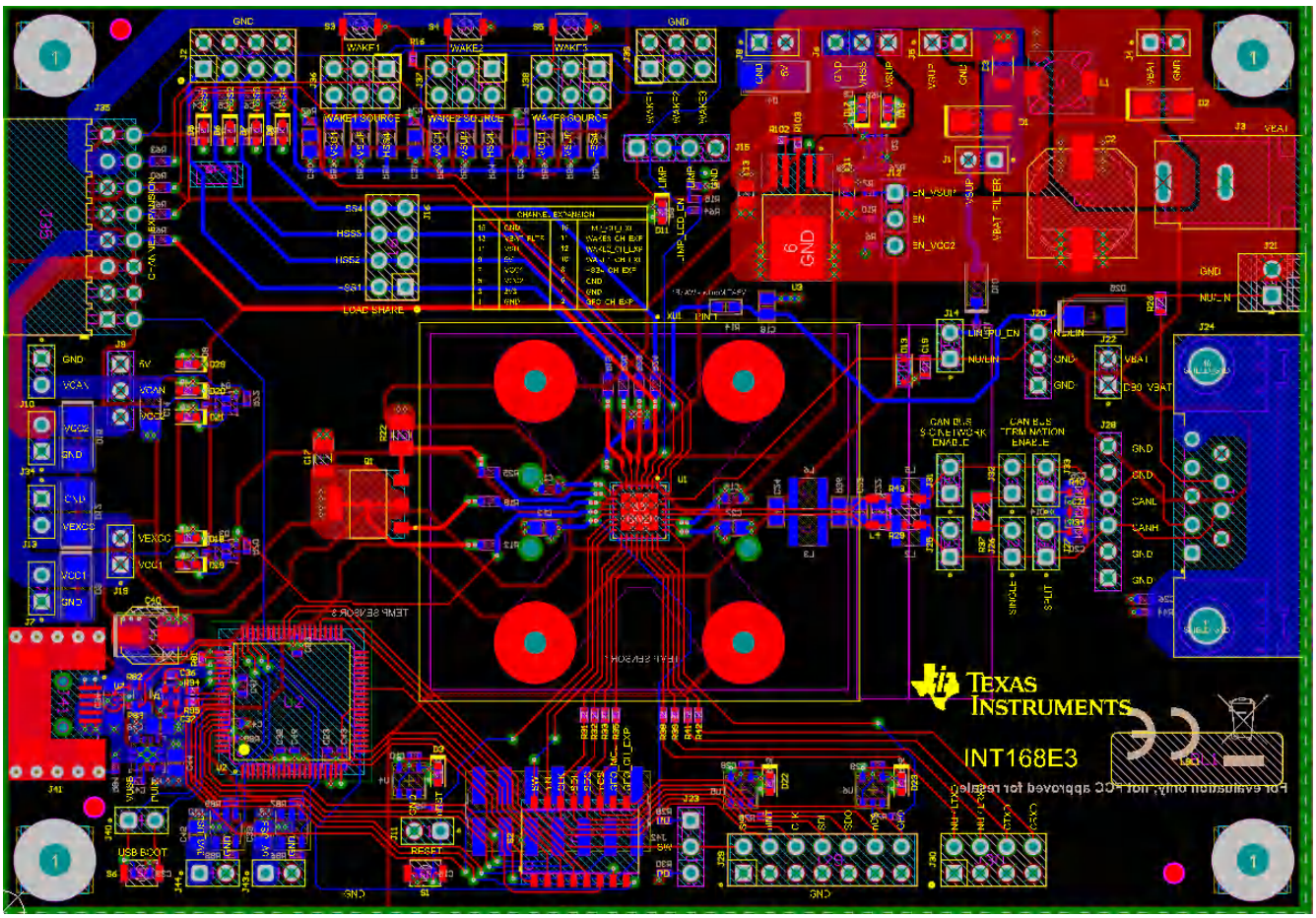


Figure 4-3. PCB Layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 High Tg	6.00mil	4.2	
5	Layer 2 GND	Copper	1.42mil		
6	Dielectric 2	FR-4 High Tg	44.00mil	4.2	
7	Layer 3 PWR	Copper	1.42mil		
8	Dielectric 3	FR-4 High Tg	6.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Figure 4-4. Layer Stack Information

4.3 Bill of Materials (BOM)

Manufacturer	PartNumber	Designator	Quantity
TDK	C1608X7R1H104K080AA	C1, C9, C15	3
Chemi-Con	EMVA101ADA330MJA0G	C2	1
Samsung	CL31B106KBHNNNE	C3, C8, C14, C34	4
TDK	CGA3E2X7R1H104K080AA	C4, C5, C6, C7	4
MuRata	GRM155R71C103KA01D	C10, C28, C29	3
Wurth Elektronik	885012207103	C11	1
TDK	CGA4J3X7R1C475K125AE	C12, C13, C27	3
AVX	06035A101JAT2A	C16	1
TDK	CGA5L1X7R1C106K160AC	C17	1
AVX	06035A221FAT2A	C19, C33, C42	3
AVX	06031C472KAT2A	C21	1
Kemet	C0805C221J1GACTU	C22, C23, C24	3
Kemet	C0603X103K1RACTU	C26	1
MuRata	GRM21BR72A223KA01L	C30, C31, C32	3
AVX	0603YC104JAT2A	C35, C46, C52, C53	4
MuRata	GRM1555C1H100JA01D	C36, C37	2
Kemet	C0805C105K4RACTU	C38	1
AVX	0805YD105KAT2A	C39, C45	2
Chemi-Con	EMVE100ADA220ME55G	C40	1
Kemet	C0603X222K5RACTU	C41	1
Kemet	C0603C474K8RACTU	C43	1
AVX	0805YD225KAT2A	C44	1
Samsung Electro-Mechanics	CL05B103KA5NNNC	C47	1
ON Semiconductor	MBRA140T3G	D1	1
Littelfuse	SMAJ30A	D2	1
Wurth Elektronik	150060SS75000	D3, D11, D22	3
Littelfuse	SMAJ6.0A	D4, D9, D12, D15	4
Wurth Elektronik	150060GS75000	D5, D6, D7, D8, D16, D17, D18, D19, D20, D21, D23, D29	12
Micro Commercial Components	1N4148W-TP	D10	1
NXP Semiconductor	PESD1LIN,115	D13	1
ON Semiconductor	1SMB5922BT3G	D24	1
B&F Fastener Supply	NY PMS 440 0025 PH	H1, H2, H3, H4	4
Keystone	1902C	H5, H6, H7, H8	4
Samtec	TSW-102-07-G-S	J1, J4, J5, J7, J8, J10, J11, J13, J14, J19, J22, J25, J26, J27, J31, J32, J33, J34, J40, J43, J44	21
Sullins Connector Solutions	PEC04DAAN	J2, J16, J30	3

Manufacturer	PartNumber	Designator	Quantity
CUI Inc.	PJ-037AH	J3	1
Samtec	TSW-103-07-G-S	J6, J9, J12, J20, J23	5
Wurth Elektronik	61300411121	J15	1
On-Shore Technology	OSTVN02A150	J21	1
TE Connectivity	5747840-5	J24	1
Samtec	TSW-106-07-G-S	J28	1
Samtec	TSW-107-07-G-D	J29	1
Samtec	SSW-108-02-G-D-RA	J35	1
Sullins Connector Solutions	PEC03DAAN	J36, J37, J38, J39	4
TE Connectivity	1734035-2	J41	1
Samtec	TSM-107-01-L-DV	J42	1
TDK	B82462A4472M000	L1	1
Abracon	AISC-1210-3R0J-T	L2, L3, L5, L6	4
TDK	ACT45B-101-2P-TL003	L4	1
Laird-Signal Integrity Products	MI1206K900R-10	L7	1
Brady	THT-14-423-10	LBL1	1
Diodes	BCP5216TA	Q1	1
Texas Instruments	CSD85301Q2	Q2, Q3, Q4	3
Yageo America	RC0402FR-074K99L	R1, R8, R45, R46, R65, R66	6
Yageo America	RC0402FR-0710KL	R2, R3, R4, R5, R6, R7, R13, R28, R30, R47, R48, R49, R50, R70, R72, R108	16
Vishay-Dale	CRCW04024K99FKED	R9, R78, R79	3
Vishay-Dale	CRCW0402100KFKED	R10	1
Vishay-Dale	CRCW04021K00FKED	R11	1
Vishay-Dale	RCS06030000Z0EA	R12, R18, R19, R20, R23, R24, R25, R26, R60, R61, R62, R63	12
Yageo America	RC0402JR-070RL	R15, R31, R32, R33, R35, R38, R39, R41, R42, R64, R94, R95	12
Susumu Co Ltd	RL1220S-R50-F	R22	1
Yageo	RC0603FR-0760R4L	R34, R40	2
Vishay-Dale	CRCW080560R4FKEA	R36	1
Vishay-Dale	CRCW1206121RFKEA	R37	1
Panasonic	ERJ-2RKF1004X	R44	1
Yageo America	RC1206FR-073KL	R51, R52, R53, R54, R55, R56, R57, R58, R59	9
Panasonic	ERJ-2RKF3301X	R67, R74, R75	3
Samsung Electro-Mechanics	RC1005F104CS	R68, R69, R71, R73	4
Vishay-Dale	CRCW040217K4FKED	R76, R77	2
Vishay-Dale	CRCW04021M00FKED	R80	1

Manufacturer	PartNumber	Designator	Quantity
Vishay-Dale	CRCW04021K50JNED	R81	1
Vishay-Dale	CRCW040233R0JNED	R82, R83	2
Vishay-Dale	CRCW040233K0JNED	R84, R85	2
Vishay-Dale	CRCW0402130KJNED	R86	1
Vishay-Dale	CRCW0402100KJNED	R87, R89	2
Vishay-Dale	CRCW0402160KJNED	R88	1
Vishay-Dale	CRCW04023K32FKED	R102	1
Vishay-Dale	CRCW0402499RFKED	R103	1
Omron Electronic Components	B3U-1000P	S1, S3, S4, S5, S6	5
TE Connectivity	1-1571983-1	S2	1
Wurth Elektronik	60900213421	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17	17
Texas Instruments	TCAN28475RHBQ1	U1	1
Texas Instruments	MSP430F5529IPNR	U2	1
Texas Instruments	TPS7B8650QKVURQ1R2	U3	1
Texas Instruments	SN74LVC1G07DBVT	U4, U5, U6	3
Texas Instruments	TPD4E004DRYR	U7	1
Texas Instruments	TPS73533DRBT	U8	1
Texas Instruments	TPS2553DBVT-1	U9, U10	2
Abracon Corporation	ABM11-24.000MHZ-D2X-T3	Y1	1

5 Additional Information

5.1 Trademarks

All trademarks are the property of their respective owners.

5.2 Related Documentation

Texas Instruments: TCAN284XX-Q1 Datasheet, SLLSFE8

Texas Instruments, TCAN285XX-Q1 Datasheet, SLLSFM2

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265