SNx5DP159RSB - TDP158RSB Transition Document

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1 Introduction

This document provides instruction on how to transition an application that is redriving or retiming an AC-coupled HDMI signal to transition-minimized differential signaling (TMDS) using the SNx5DP159RSB device, to an application that is redriving an AC-coupled HDMI signal to TMDS using the TDP158RSB device, and the other way around. The next sections describe the differences between the SNx5DP159RSB and TDP158RSB devices. To transition from one device to the other just requires following the changes in pins, registers, and the PCB.

2 Functional Changes

This section lists the functional changes.

- SNx5DP159RSB – Operates in Redriver mode up to 3 Gbps or Retimer Mode at all speeds. Capable of reporting a DP-HDMI adaptor ID
- TDP158RSB – Operates in Redriver Only mode – all speeds. No DP-HDMI adaptor ID reporting.

2.1 Power

Table 1 lists the power changes.

Table 1. Power Changes

Parameter	SNx5DP159RSB	TDP158RSB
Typical active power at 6 Gbps (mW)	435 mW (600 mW maximum)	200 mW (350 mW maximum)
Typical standby or low power (uW)	10000 uW	8000 uW

2.2 Pin Function Changes

Table 2 lists the pin function changes.

Table 2. Pin Function Changes

Pin	SNx5DP159RSB	TDP158RSB
Pin 13	SCL_CTL: I^2C clock signal **NOTE:** When I2C_EN/PIN = Low, pin strapping takes priority and those functions cannot be changed by I^2C.	SCL_CTL/SWAP: When I2C_EN = High: I^2C clock signal. When I2C_EN = Low: Lane SWAP (HDMI mode only) • SWAP = L: Normal operation • SWAP = H: Lane swap
Pin 14	SDA_CTL: I^2C data signal **NOTE:** When I2C_EN/PIN = Low, pin strapping takes priority and those functions cannot be changed by I^2C.	SDA_CTL/PRE: When I2C_EN = High: I^2C data signal When I2C_EN = Low: Pre-emphasis • DE = L: 0 dB • DE = H: 3.5 dB

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Table 2. Pin Function Changes (continued)

Pin	SNx5DP159RSB	TDP158RSB
Pin 16	PRE_SEL: I2C_EN/PIN = High: NA I2C_EN/PIN = Low: De-emphasis • PRE_SEL = L: –2 dB de-emphasis • PRE_SEL = No connect: 0 dB • PRE_SEL = H: Reserved	TERM: I2C_EN/PIN = High: NA I2C_EN/PIN = Low: Source termination control • TERM = H: 75 Ω to approximately 150 Ω • TERM = L: 150 Ω to approximately 300 Ω • TERM = NC: No transmit termination **NOTE:** When TMDS_CLOCK_RATIO_STATUS bit = 1, the TDP158 device automatically sets source termination from 75 Ω to approximately 150 Ω.
Pin 17	EQ_SEL/A0: When I2C_EN/PIN = High: I^2C address bit 1 When I2C_EN/PIN = Low: Equalization pin strap • EQ_SEL = L: Fixed EQ at 7.5 dB • EQ_SEL = No connect: Adaptive EQ • EQ_SEL = H: Fixed at 14 dB **NOTE:** 3 level for pin strap programming, but 2 level for I^2C address	A0/EQ1: When I2C_EN = High: I^2C address bit 1 When I2C_EN = Low: EQ1 pin setting Works in conjunction with A1/EQ2 See Main Link Inputs for settings
Pin 19	VDD	NC
Pin 23	HDMI_SEL/A1: When I2C_EN/PIN = High address bit 2 When I2C_EN/PIN = Low : HDMI_SEL • HDMI_SEL = High: Configured for DVI • HDMI_SEL = Low: Configured for HDMI (adaptor ID block is readable through I^2C or I^2C-over-AUX) **NOTE:** Internal weak pull down	A1/EQ2: When I2C_EN = High: I^2C address bit 2 When I2C_EN = Low: EQ2 pin setting Works in conjunction with A0/EQ1 See Main Link Inputs for settings

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3 Recommended PCB Changes

Table 3 lists the recommended PCB changes.

Table 3. Recommended PCB Changes

Pin	SNx5DP159RSB	TDP158RSB
Pin 19	Routed to VDD	No connect can be routed to VDD
VSADJ	Resistor value = 6.49 kΩ (application dependent)	Resistor value = 6.49 kΩ (application dependent)
Pin strapping resistors	3-level input pins • Pull up: 65 kΩ ±10% • Pull down: 0 to 65 kΩ +10% 2-level input pins • Pull up: 0 to 65 kΩ +10% • Pull down: 0 to 65 kΩ +10%	Pull up or pull down: 1 kΩ to 0 Ω ±10%
VCC	VCC nom: 3.3 V VCC min: 3.0 V VCC max: 3.6 V	VCC nom: 3.3 V VCC min: 3.13 V VCC max: 3.47 V

4 Register Changes

Table 4 lists the register changes.

Table 4. Register Changes

Parameter	SNx5DP159RSB	TDP158RSB
ID register (0x00h to 0x07h)	DP159 (ASCII Characters)	TDP158 (ASCII characters)
Revision ID (0x08)	Device revision	Device revision
Misc control (0x09)	[7] SWAP_EN [6] LANE_POLARITY [5:4] Reserved [3] PD_EN [2] HPD_AUTO_PWRDWN_DISABLE [1:0] I2C_DR_CTL	[7] LANE_SWAP [6] LANE_CONTROL [5] DP mode [4] SIG_EN [3] PD_EN [2] HPD_AUTO_PWRDWN_DISABLE [1:0] I2C_DR_CTL
Misc control (0x0A)	[7] Application Mode(Source/Sink) [6] HPDSNK_GATE_EN [5] EQ_ADA_EN [4] EQ_EN [3] AUX_BRG_EN [2] APPLY_RXTX_CHANGES [1:0] DEV_FUNC_MODE	[7] Reserved [6] HPDSNK_GATE_EN [5:2] Reserved [1:0] SLEW_CTL_DATA
Misc control (0x0B)	[7:6] SLEW_CTL [6] HDMI_SEL? [4:3] TX_TERM_CTL [2] Reserved [1] TMDS_CLOCK_RATIO_STATUS [0] DDC_TRAIN_SET	[7:6] SLEW_CTL_CLK [5] Reserved [4:3] TERM [2] DDC_DR_SEL [1] TMDS_CLOCK_RATIO_STATUS [0] DDC_TRAIN_SETDISABLE
Misc control (0x0C)	[7:5] VSWING_DATA [4:2] VSWING_CLK [1:0] HDMI_TWPST1	[7:5] VSWING_DATA [4:2] VSWING_CLK [1:0] HDMI_TWPST1
EQ control (0x0D)	[7:6] Reserved [5:3] Data Lane fixed EQ [2:1] Clock Lane EQ [0] Clock VOD control(Low active)	[7] Reserved [6:3] Data Lane fixed EQ [2:1] Clock EQ Values [0] Clock VOD control(High active)

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Table 4. Register Changes (continued)

Parameter	SNx5DP159RSB	TDP158RSB
EyeScan (0x0E to 0x1F)	Miscellaneous	NA
Aux channel and Power mode status (0x20)	[7:4] Reserved [3] AUX_TX_SR [2:0] AUX_SWING	[7] Power Down [6] Standby [5] Loss of signal [4:0] Reserved
DP-Mode individual lane control (0x30)	NA	[7:6] Data rate select [5] Clock lane enable [4] Lane D0 enable [3] Lane D1 enable [2] Lane D2 enable
DP-Mode individual lane control register per lane (0x31 – 0x34)	NA	[7:5] VOD swing Adjust [4:3] Pre-emphasis Adjust [2:0] Reserved
DP-Mode fixed EQ D1 and D2 (0x4E)	NA	[7:4] D1 Fixed EQ [3:0] D2 Fixed EQ
DP-Mode fixed EQ CLK and D0 (0x4F)	NA	[7:4] CLK Fixed EQ [3:0] D0 Fixed EQ

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2018) to A Revision **Page**

- Changed *Recommended PCB Changes* table 4

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