ISOW1044 Isolated CAN FD Transceiver with Integrated Low-Emissions, Low-Noise, High-Efficiency DC-DC Converter

1 Features

- Meets the requirements of ISO 11898-2:2016 physical layer standards
  - Support of Classical CAN: 1 Mbps
  - Optimized for CAN FD: 2 and 5 Mbps
- Integrated DC-DC converter with low-emissions, low-noise
  - Meets CISPR 32 and EN 55032 Class B with greater than 6 dB margin on a two-layer PCB
  - Low frequency power converter at 25 MHz enabling low noise performance
- Additional 10 Mbps GPIO channel
- High efficiency output power
  - Typical efficiency: 47%
  - Isolated output voltage accuracy: ± 5%
  - Additional output current: 20 mA
- Independent power supply for CAN & DC-DC
  - Logic supply (V_{IO}): 1.71 V to 5.5 V
  - Power converter supply (V_{DD}): 4.5 V to 5.5 V
- Fault-Protected CAN FD Transceiver
  - DC Bus fault protection voltage: ± 58V
  - Receiver common mode input voltage: ±12 V
  - Remote wakeup via BUS wake-up pattern
- Typical loop delay: 167 ns
- Reinforced and Basic isolation options
- High CMTI: 100-kV/µs (typical)
- High ESD bus protection w.r.t GND2
  - HBM ESD: ±12 kV
  - IEC 61000-4-2 contact discharge: ±8 kV
- Operating temperature range: -40°C to 125°C
- Current limit and thermal shutdown
- 20-pin wide SOIC package
- Safety-Related Certifications planned:
  - VDE Reinforced and Basic insulation per DIN VDE V 0884-11:2017-01
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications

2 Applications

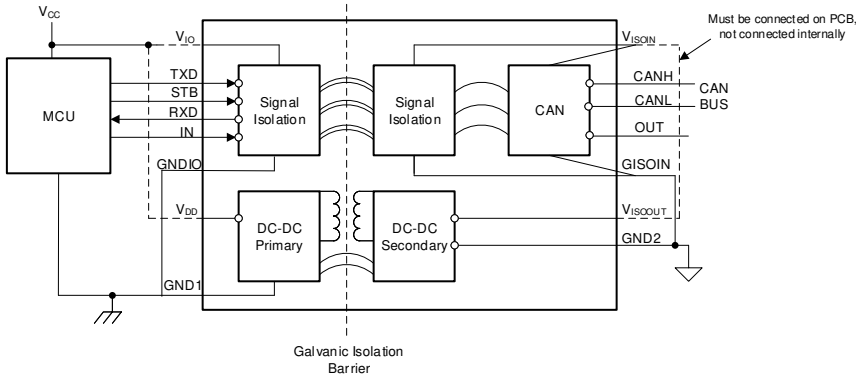
- Factory Automation
- Building Automation
- Industrial Transport
- Solar Inverters, Protection Relay
- Motor Drives

3 Description

The ISOW1044 device is a galvanically-isolated controller area network (CAN) transceiver with a built-in isolated DC-DC converter that eliminates the need for a separate isolated power supply in space-constrained isolated designs. The low-emissions, isolated DC-DC meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20 mA output current can be used to power other circuits on the board. An integrated 10 Mbps GPIO channel is available and can help remove an additional digital isolator or optocoupler for diagnotstics, LED indication or supply monitoring.

Device Information

FEATURE	ISOW1044	ISOW1044B
Protection Level	Reinforced	Basic
Surge Test Voltage	10 kV_{PK}	7.8 kV_{PK}
Isolation Rating	5000 V_{RMS}	5000 V_{RMS}
Working Voltage	1000 V_{RMS}/1500 V_{PK}	1000 V_{RMS}/1500 V_{PK}
Package	DFM (20)	DFM (20)
Body Size (Nom)	12.83mm × 7.5 mm	12.83mm × 7.5 mm



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (December 2021)	Page
• Updated device status to Production status	1

5 Description Continued

The device supports both classical CAN and CAN FD networks up to 5 Megabits per second (Mbps) data rate. It offers ±58-V DC bus fault protection and ±12-V common-mode voltage range. Both signal and power paths are 5-kV_{RMS} isolated per UL1577 and are qualified for reinforced and basic isolation per VDE, CSA, TUV and CQC. The bus pins of these devices can endure up to 8 kV of IEC 61000-4-2 electrostatic discharge (ESD),.

The ISOW1044 device can operate from a single supply voltage of 4.5 V to 5.5 V by connecting V_{IO} and V_{DD} together on PCB. If lower logic levels are required, these devices support 1.71 V to 5.5 V logic supply (V_{IO}) that can be independent from the power converter supply (V_{DD}) of 4.5 V to 5.5 V. This device supports a wide operating ambient temperature range from –40°C to +125°C and are available in 20-pin DFM (SOIC-20 footprint compatible package) offering a minimum of 8-mm creepage and clearance.

The ISOW1044 supports a standby mode and wake over CAN compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP). The device also includes protection and diagnostic features supporting thermal-shutdown (TSD), TXD dominant time-out (DTO) and supply undervoltage detection.

6 Device Comparison Table

PART NUMBER	ISOLATION	PACKAGE	BODY SIZE (NOM)
ISOW1044	Reinforced	20-DFM (SOIC)	12.83 mm x 7.5 mm
ISOW1044B	Basic	20-DFM (SOIC)	12.83 mm x 7.5 mm

7 Pin Configuration and Functions

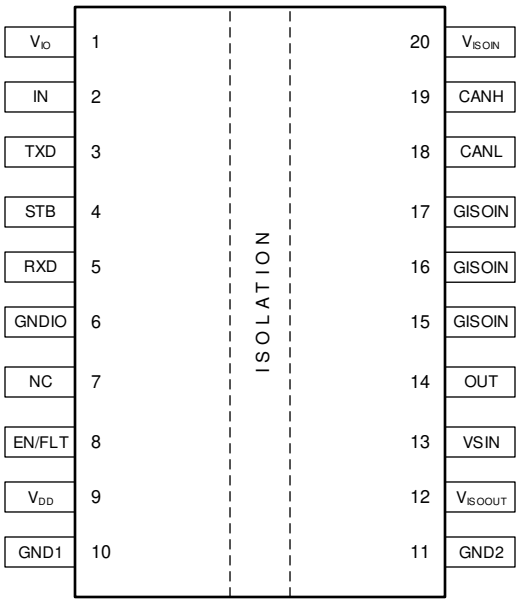


Figure 7-1. ISOW1044 20-pin DFM Top View

Table 7-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
V_{IO}	1	--	Side 1 Logic supply
IN	2	I	General purpose logic (GPIO) input (internal pull-down)
TXD	3	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
STB	4	I	Standby enable. Connect this pin to GNDIO in normal mode. If this pin is floating or logic high, driver is in standby mode.
RXD	5	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
GNDIO	6	--	Ground connection on side 1 for V_{IO}. GNDIO and GND1 are not internally connected and need be shorted on PCB.
NC	7	--	Not connected internally
EN/FLT	8	I/O	Multi-function power converter enable input pin or fault output pin. Can only be used as either an input pin or an output pin. • If it's used as Power converter enable input pin, the EN/FLT pin enables and disables the integrated DC-DC power converter. Connect directly to microcontroller or through a series current limiting resistor to use as an enable input pin. DC-DC power converted is enabled when EN is high (connected to V_{IO}) and disabled when low (connected to GND1). If EN is floating, DC-DC converter is enabled (internal pull-up resistor) • If it's used as Fault output pin, the EN/FLT pin gives an alert signal if power converter is not operating properly. This pin is active low. Connect to microcontroller through a 5 kΩ or greater pull-up resistor to use as a fault outpin pin.
V_{DD}	9	--	Side 1 DC-DC converter power supply
GND1	10	--	Ground connections on side for V_{DD} . GNDIO and GND1 are not internally connected and need be shorted on PCB.
GND2	11	--	Ground connections on side for V_{ISOOUT} . GND2 and GISOIN are not internally connected and need be shorted direclty on PCB, or connected through a ferrite bead.
V_{ISOOUT}	12	--	Isolated power converter output voltage. V_{ISOOUT} and V_{ISOIN} need be shorted directly on PCB, or connected through a ferrite bead.
V_{SIN}	13	I	Power converter input . Pin 12 and pin 13 need be shorted directly on PCB.

Table 7-1. Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
OUT	14	O	General purpose logic (GPIO) output (default output is low)
GISOIN	15, 16, 17	--	Ground connections for V_{ISOIN}. GND2 and GISOIN need be shorted direclty on PCB, or connected through a ferrite bead.
CANL	18	I/O	Low-level CAN bus line
CANH	19	I/O	High-level CAN bus line
V_{ISOIN}	20	--	Power supply input for CAN tranceiver. V_{ISOIN} and V_{ISOOUT} need be shorted direclty on PCB, or connected through a ferrite bead.

(1) I = Input, O = Output

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	–0.5	6	V
V_{ISOIN}	Isolated supply voltage, input supply for CAN transceiver	–0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output	–0.5	6	V
V_{IO}	Logic supply voltage	–0.5	6	V
V_{BUS}	Voltage on bus pins (CANH, CANL with respect to GND2)	-58	58	V
V_{BUS_DIFF}	Max Differential voltage on bus pins (CANH-CANL)	-45	45	V
V_{logic_IO}	Logic I/O voltage level (RXD, TXD, STB, EN, IN)	–0.5	V_{IO} + 0.5(3)	V
	OUT	-0.5	V_{ISOIN} + 0.5	V
I_O	Output current on RXD, OUT pins	–15	15	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the deviceat these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.
(3) The maximum voltage must not be greater than 6 V.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except bus pins	±2000	V
			CANH, CANL Bus pins w.r.t GND2(pin15/16/17)	±12000	
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	V
$V_{(ESD)}$	Electrostatic discharge	per IEC61000-4-2 contact discharge, CANH and CANL w.r.t. GND2		±8000	V
$V_{(ESD)}$	Electrostatic discharge	per IEC61000-4-2 contact discharge, CANH and CANL w.r.t. GND1 (across Isolation barrier)		±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD controlprocess.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD controlprocess.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Logic supply voltage	1.8-V operation	1.71		1.89	V
		2.5-V, 3.3-V, and 5.5-V operation	2.25		5.5	
V_{DD}	Power converter supply voltage		4.5		5.5	V
$V_{DD(UVLO+)}$	Supply threshold when Power converter supply is rising			2.7	2.95	V
$V_{DD(UVLO-)}$	Supply threshold when Power converter supply is falling		2.40	2.55		V
$V_{HYS1(UVLO)}$	Power converter supply voltage hysteresis		0.15	0.24		V
$V_{IO(UVLO+)}$	Rising threshold of Logic supply voltage				1.7	V
$V_{IO(UVLO-)}$	Falling threshold of Logic supply voltage		1			V
$V_{HYS2(UVLO)}$	Logic supply voltage hysteresis		75	125		mV

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage (TXD, STB, EN, and IN inputs)		0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (TXD, STB, EN, and IN inputs)		0		0.3 × V_{IO}	V
I_{OH}	High-level output current RXD	V_{IO} = 5V	-4			mA
		V_{IO} = 3.3V	-2			mA
		V_{IO} = 1.8 or 2.5V	-1			mA
I_{OL}	Low-level output current RXD	V_{IO} = 5V			4	mA
		V_{IO} = 3.3V			2	mA
		V_{IO} = 1.8 or 2.5V			1	mA
I_{OH}	High-level output current OUT	V_{DD}=4.5 to 5.5V	-4			mA
I_{OL}	Low-level output current OUT	V_{DD}=4.5 to 5.5V			4	mA
$1/t_{UI}$	Signaling rate	CAN			5	Mbps
DR	Data rate for extra GPIO channel	GPIO			10	Mbps
Tpwrup	Power up time after applying input supply(Isolated output supply reaches 90% of setpoint and data transmission can start after this)			5		ms
T_A	Ambient operating temperature	≤ 50% of bits are dominant	–40		125	°C
			–40		105	°C

8.4 ThermalInformation

THERMAL METRIC(1)		ISOW1044 DFM 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	°C/W

(1) For more informationabout traditional and new thermal metrics, see the*Semiconductor andIC Package Thermal Metrics* application report.

8.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{IO} = V_{DD} = 5.5 V, STB= GND1, CAN Bus load R_L= 60 Ω, TXD=repetitive pattern of 1 ms time period with 990 µs LOW time, 10 µs HIGH time, Extra load on V_{ISOOUT}= 20 mA			1060	mW
P_{D1}	Maximum power dissipation (side-1)				490	mW
P_{D2}	Maximum power dissipation by (side-2)				570	mW

8.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	>17	um
DTI	Distance through the insulation	Minimum internal gap (internal clearance- transformer power isolation)	>120	um
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage Category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1500	
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW1044(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW1044B(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7800\ V_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; ISOW1044: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s. ISOW1044B: $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; ISOW1044: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s. ISOW1044B: $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied accordingto the specific equipment isolation standards of an application. Care should be taken to maintainthe creepage and clearance distance of a board design to ensure that the mounting pads of theisolator on the printed-circuit board do not reduce this distance. Creepage and clearance on aprinted-circuit board become equal in certain cases. Techniques such as inserting grooves and/orribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation (ISOW1044) and basic electrical insulation (ISOW1044B)* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsicsurge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partialdischarge (pd).
(5) All pins on each side of the barrier tied together creating atwo-terminal device

8.7 Safety-Related Certifications

VDE	CSA	UL	TUV	CQC
Plan to certifiy according to DIN VDE V 0884-11 :2017-01	Plan to certifiy according to IEC 62368-1, IEC 61010-1 and IEC 60601-1	Plan to certifiy under UL 1577 Component Recognition Program	Plan to certifiy according to GB4943.1-2011	Plan to certifiy ccording to EN 61010-1:2010/ A1:2019 and EN 62368-1:2014
Maximum transient isolation voltage 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1500 V_{PK}; Maximum surge isolation voltage, ISOW1044: 6250 V_{PK} (Reinforced), ISOW1044B: 6000 V_{PK} (Basic)	Per CSA62368-1:19, IEC 62368-1:2018 Ed. 3, CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed., ISOW1044 (Reinforced): 600 V_{RMS}, ISOW1044B (Basic): 1000 V_{RMS} maximum working voltage (pollution degree 2, material group I, ambient temperature 90 ℃), 1 MOPP (Means of Patient Protection) per CSA 60601- 1:14 . IEC 60601-1 (ISOW1044 only) Ed.3+A1, 250 V_{RMS} maximum working voltage	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage.	ISOW1044 (Reinforced): 5000 V_{RMS} reinforced insulation per EN 61010-1:2010/A1:2019 and EN 62368-1:2014 up to working voltage of 600 V_{RMS} . ISOW1044B (Basic): 1000 V_{RMS}
Certification planned	Certification planned	Certification planned	Certification planned	Certification planned

8.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier uponfailure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 68.5 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C, See Figure 8-1			332	mA
		$R_{\theta JA}$ = 68.5 °C/W, V_I = 3.6 V, T_J = 150 °C, T_A = 25 °C, See Figure 8-1			507	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 68.5 °C/W, T_J = 150 °C, T_A = 25 °C, See Figure 8-2			1826	mA
T_S	Safety temperature(1)				150	℃

(1) The maximum safety temperature,T_S, has the same value as the maximum junction temperature,T_J, specified for the device. The I_S andP_S parameters represent the safety current and safety power respectively.The maximum limits of I_S and P_S should not beexceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board forleaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$,where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ isthe maximum allowed junction temperature.
$P_S = I_S \times V_I$, whereV_I is the maximum input voltage.

8.9 Electrical Characteristics

over recommended operating conditions, typical values are at V_{DD} = 5V, GND1 = GNDIO, GND2 = GISOIN, V_{IO} = 3.3 V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device						
V_{ISOOUT}	Isolated Output supply voltage	EN=V_{DD}, STB, TXD, IN floating	4.75	5	5.25	V
Iout	Extra current available on Visoout	V_{DD} = 4.5 to 5.5 V, CAN full loaded 60 Ω, TXD toggling 5 Mbps, IN toggling 10 Mbps		20		mA
V_{OH}	Output high voltage on OUT pin	V_{DD} = 5 V ± 10%, I_{OH} = –4 mA, IN = V_{IO}	V_{ISOIN} – 0.4			V
V_{OL}	Output low voltage on OUT pin	V_{DD} = 5 V ± 10%, I_{OL} = 4 mA, IN = GND2			0.4	V
I_I	Input current, IN	IN at GND1 or V_{IO}	–25		25	µA
I_I	Input current, EN	EN at GND1 or V_{IO}	–25		25	µA
TXD TERMINAL						
I_I	Input leakage current	TXD = V_{IO} or GND1	–25		25	uA
C_I	Input capacitance	VIN = 0.4 x sin(2 x π x 1E+6 x t) + 1.65 V, V_{IO} = 3.3 V		2		pF
RXD TERMINAL						
V_{OH}	High level output voltage	I_O = -4 mA for 4.5 V ≤ V_{IO} ≤ 5.5 V, See Figure 9-4	V_{IO} – 0.4	V_{IO} – 0.2		V
		I_O = -2 mA for 3.0 V ≤ V_{IO} ≤ 3.6 V, See Figure 9-4	V_{IO} – 0.2	V_{IO} – 0.06		V
		I_O = -1 mA for 2.25 V ≤ V_{IO} ≤ 2.75 V, See Figure 9-4	V_{IO} – 0.1	V_{IO} – 0.04		V
		I_O = -1 mA for 1.71 V ≤ V_{IO} ≤ 1.89 V, See Figure 9-4	V_{IO} – 0.1	V_{IO} – 0.04		V
V_{OL}	Low level output voltage	I_O = 4 mA for 4.5 V ≤ V_{IO} ≤ 5.5 V, See Figure 9-4		0.2	0.4	V
		I_O = 2 mA for 3.0 V ≤ V_{IO} ≤ 3.6 V, See Figure 9-4		0.07	0.2	V
		I_O = 1 mA for 2.25 V ≤ V_{IO} ≤ 2.75 V, See Figure 9-4		0.035	0.1	V
		I_O = 1 mA for 1.71 V ≤ V_{IO} ≤ 1.89 V, See Figure 9-4		0.04	0.1	V
STB Terminal						
I_I	Input leakage current	STB = V_{IO} or GND1	-25		25	uA
C_I	Input capacitance	VIN = 0.4 x sin(2 x π x 1E+6 x t) + 1.65 V, V_{IO} = 3.3 V		2		pF
DRIVER ELECTRICAL CHARACTERISTICS						
$V_{O(DOM)}$	Bus output voltage(Dominant), CANH	STB=GND1, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	2.75		4.5	V
	Bus output voltage(Dominant), CANL	STB=GND1, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	0.5		2.25	V
$V_{O(REC)}$	Bus output voltage(recessive), CANH and CANL	STB=GND1, TXD = V_{IO} and R_L = open, See Figure 9-1 and Figure 9-2	2.0	0.5 x V_{ISOIN}	3.0	V

over recommended operating conditions, typical values are at V_{DD} = 5V, GND1 = GNDIO, GND2 = GISOIN, V_{IO} = 3.3 V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(DOM)}$	Differential output voltage(dominant)	STB=GND1, TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	1.4		3.3	V
	Differential output voltage(dominant)	STB=GND1, TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	1.5		3.0	V
	Differential output voltage(dominant)	STB=GND1, TXD = 0 V, R_L = 2240 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	1.5		5.0	V
$V_{OD(REC)}$	Differential output voltage(recessive)	TXD = VIO, R_L = 60 Ω, and C_L = open, See Figure 9-1 and Figure 9-2	–120.0		12.0	mV
	Differential output voltage(recessive)	TXD = VIO, R_L = open, and C_L = open, See Figure 9-1 and Figure 9-2	–50.0		50.0	mV
$V_{O(STB)}$	Bus Output Voltage, CANH, Standby mode	STB = V_{IO}, R_L = open, See Figure 9-1 and Figure 9-2	–100		100	mV
$V_{O(STB)}$	Bus Output Voltage, CANL, Standby mode	STB = V_{IO}, RL = open, See Figure 9-1 and Figure 9-2	–100		100	mV
$V_{OD(STB)}$	Bus Output Voltage, CANH-CANL, Standby mode	STB=V_{IO}, RL = open, See Figure 9-1 and Figure 9-2	-200		200	mV
V_{SYM_DC}	Output symmetry (V_{ISOIN} - $V_{O(CANH)}$ - $V_{O(CANL)}$)	R_L = 60 Ω and C_L = open, TXD = V_{IO} or GND1, See Figure 9-1 and Figure 9-2	–400.0		400.0	mV
$I_{OS(SS\_DOM)}$	Short circuit current steady state output current, dominant	-15 V < CANH < 40 V, CANL = open, and TXD = 0 V, See Figure 9-8	–115.0			mA
		-15 V < CANL < 40 V, CANH = open, and TXD = 0 V, See Figure 9-8			115.0	mA
$I_{OS(SS\_REC)}$	Short circuit current steady state output current, recessive	-27 V < VBUS < 32 V, VBUS = CANH = CANL, and TXD = V_{IO} , See Figure 9-8	–5.0		5.0	mA
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{CM}	Input common mode range	See Figure 9-4 and Table 9-1	–12		12	V
V_{IT}	Differential input threshold voltage, normal mode	-12 V ≤ V_{CM} ≤ 12 V, STB = GND1, See Figure 9-4 and Table 9-1	500.0		900.0	mV
$V_{IT(STB)}$	Differential input threshold voltage, standby mode	-12 V ≤ V_{CM} ≤ 12 V, STB = V_{IO}	400		1150	mV
V_{HYS}	Hysteresis voltage for differential input threshold, normal mode	-12 V ≤ V_{CM} ≤ 12 V, STB = GND1		100		mV
$V_{DIFF(DOM)}$	Dominant state differential input voltage range, normal mode	-12 V ≤ V_{CM} ≤ 12 V, STB = GND1, See Figure 9-4 and Table 9-1	0.9		9	V
$V_{DIFF(DOM)}$	Dominant state differential input voltage range, standby mode	-12 V ≤ V_{CM} ≤ 12 V, STB = V_{IO}, See Figure 9-4 and Table 9-1	1.15		9	V
$V_{DIFF(REC)}$	Recessive state differential input voltage range, normal mode	-12 V ≤ V_{CM} ≤ 12 V, STB = GND1, See Figure 9-4 and Table 9-1	–4		0.5	V
$V_{DIFF(REC)}$	Recessive state differential input voltage range, standby mode	-12 V ≤ V_{CM} ≤ 12 V, STB = V_{IO}, See Figure 9-4 and Table 9-1	–4		0.4	V
$I_{OFF(LKG)}$	power-off bus input leakage current	CANH = CANL = 5 V, V_{DD} = V_{IO} = GND1			5	uA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance	TXD = V_{IO}			10	pF
R_{ID}	Differential input resistance	TXD = V_{IO} ; -12 V ≤ VCM ≤ +12 V	40		90	kΩ

over recommended operating conditions, typical values are at V_{DD} = 5V, GND1 = GNDIO, GND2 = GISOIN, V_{IO} = 3.3 V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{IN}	Input resistance (CANH or CANL)	TXD = V_{IO} ; -12 V ≤ VCM ≤ +12 V	20		45	kΩ
$R_{IN(M)}$	Input resistance matching: (1 - $R_{IN(CANH)}/R_{IN(CANL)}$) x 100%	V_{CANH} = V_{CANL} = 5 V	–1		1	%

8.10 Supply Current Characteristics

Typical values are at V_{DD}=5V, V_{IO}=3.3V, Min/Max over recommended operating conditions, GND1 = GNDIO, GND2 = GISOIN, V_{DD} = 4.5 V to 5.5 V(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter disabled						
I_{DD}	Power converter supply current	EN = GND1, STB, TXD, IN floating		0.23	0.27	mA
I_{IO}	Logic supply current	EN = GND1, STB, TXD, IN floating		0.34	0.70	mA
Supply current: Normal Mode						
I_{DD}	Power converter supply current	TXD = GND1, Bus dominant, R_L= 60 Ω		124	211	mA
I_{DD}	Power converter supply current	TXD = V_{IO}, Bus recessive, R_L = 60 Ω		26	46	mA
I_{DD}	Power converter supply current	TXD = 1Mbps 50% duty square wave, R_L = 60 Ω		76	123	mA
I_{DD}	Power converter supply current	TXD = 5 Mbps 50% duty square wave, R_L= 60 Ω		78	136	mA
I_{IO}	Logic supply current	TXD = GND1, Bus dominant, V_{IO} = 1.71 to 1.89 V		4.3	5.5	mA
I_{IO}	Logic supply current	TXD = GND1, Bus dominant, V_{IO} = 2.25 to 5.5 V		4.9	6.0	mA
I_{IO}	Logic supply current	TXD = V_{IO}, Bus recessive, V_{IO} = 1.71 to 1.89 V		3.3	5.4	mA
I_{IO}	Logic supply current	TXD = V_{IO}, Bus recessive, V_{IO} = 2.25 to 5.5 V		3.8	5.5	mA
I_{IO}	Logic supply current	TXD = 1 Mbps square wave 50% duty, V_{IO} = 3 to 3.6V		4.4	5.3	mA
I_{IO}	Logic supply current	TXD = 5 Mbps square wave 50% duty, V_{IO} = 3 to 3.6V		4.5	6.2	mA
Supply current: Standby mode						
I_{DD}	Power converter supply current	STB = V_{IO} , R_L = 60 Ω		16	23	mA
I_{IO}	Logic supply current	STB = V_{IO} , V_{IO} = 3 to 3.6 V		2.7	3.5	mA

8.11 Switching Characteristics

Typical specifications are at V_{IO} = 3.3V, V_{DD} = 5V, GND1 = GNDIO, GND2 = GISOIN, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 1.71 V < V_{IO} < 5.5 V, See Figure 9-3		140	205	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; 1.71 V < V_{IO} <5.5 V, See Figure 9-3		167	222	ns
t_{MODE}	Mode change time, from Normal to Standby or from Standby to Normal				20	us
t_{WK_FILTER}	Filter time for a valid wake-up pattern		0.5		1.8	us
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value		0.8		5	ms
CMTI	Common mode transient immunity	TXD = V_{IO} or GND1, V_{CM} = 1200 V_{PK}, See Figure 9-9	85	100		kV/µs
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, LOW to HIGH TXD edge to driver recessive (dominant to recessive)	R_L = 60 Ω and C_L = 100 pF; input rise/fall time (10% to 90%) on TXD =1 ns, See Figure 9-3		87	110	ns
t_{pLD}	Propagation delay time, HIGH TO LOW TXD edge to driver dominant (recessive to dominant)			78	105	
$t_{sk(p)}$	pulse skew (|tpHR - tpLD|)			15		
t_R	Differential output signal rise time			27		
t_F	Differential output signal fall time			48		
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}	R_{TERM} = 60 Ω, C_L = open, C_{SPLIT} = 4.7nF, TXD = Dominant or receissive or toggling at 250khz, 1Mhz See Figure 9-3	0.9		1.1	V/V
t_{TXD_DTO}	Dominant time out	R_L = 60 Ω and C_L = open, See GUID-20200710-SS0I-JPX8-LTFT-RNRQCRR6XDXR	1.2		3.8	ms
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, bus dominant to recessive transition to RXD high output (dominant to recessive)	$C_{L(RXD)}$ = 15 pF, See Figure 9-5		90	115	ns
t_{pDL}	Propogation delay time, bus recessive to dominant transition to RXD low output (recessive to dominant)			80	105	ns
t_R	Output signal rise time(RXD)			1		ns
t_F	Output signal fall time(RXD)			1		ns
FD TIMING PARAMETERS						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns, See Figure 9-6	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns, See Figure 9-6	155		210	ns

Typical specifications are at V_{IO} = 3.3V, V_{DD} = 5V, GND1 = GNDIO, GND2 = GISOIN, Min/Max are over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BIT(RXD)}$	Bit time on RXD bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns, See Figure 9-6	400		550	ns
	Bit time on RXD bus output pins with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns, See Figure 9-6	120		220	ns
ΔtREC	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, See Figure 9-6	-65		40	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; input rise/fall time (10% to 90%) on TXD =1 ns; ΔtREC = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$, See Figure 9-6	-45		15	ns
GPIO Channel						
t_{PLH}, t_{PHL}	Propagation delay time			11	25	ns
PWD	Pulse Width distortion, $\lvert t_{PLH} - t_{PHL} \rvert$			3.5	10	ns
t_r	Output signal rise time			2.2	5	ns
t_f	Output signal fall time			2.2	5	ns

8.12 Insulation Characteristics Curves

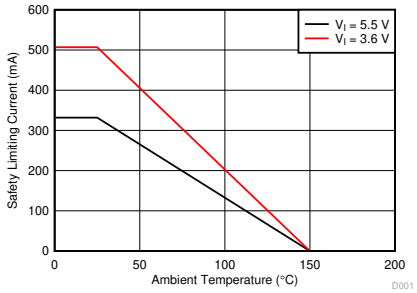


Figure 8-1. Thermal Derating Curve for Limiting Current per VDE

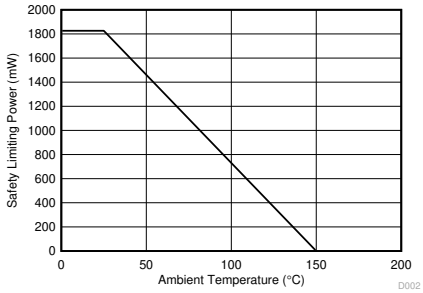
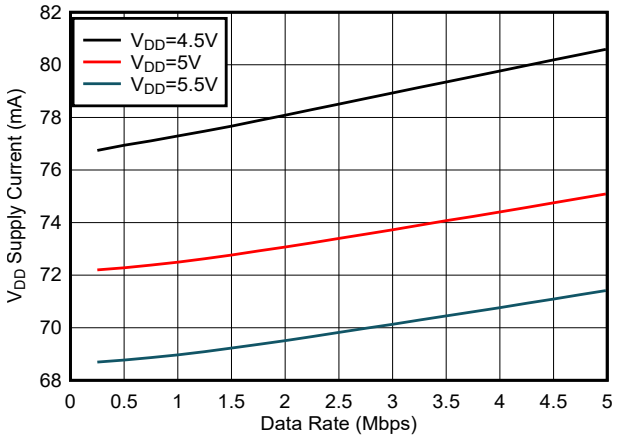


Figure 8-2. Thermal Derating Curve for Limiting Power per VDE

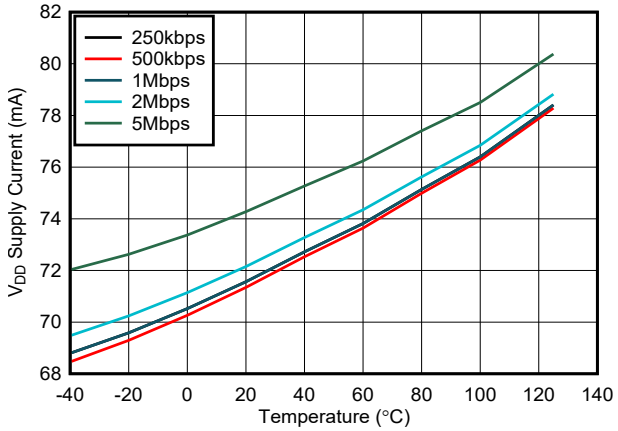
8.13 Typical Characteristics

V_{DD} = V_{IO} , V_{ISOIN} = V_{ISOOUT}, $C_{L(RXD)}$ = 15 pF , R_L = 60 Ω, T_A = 25°C unless otherwise noted.



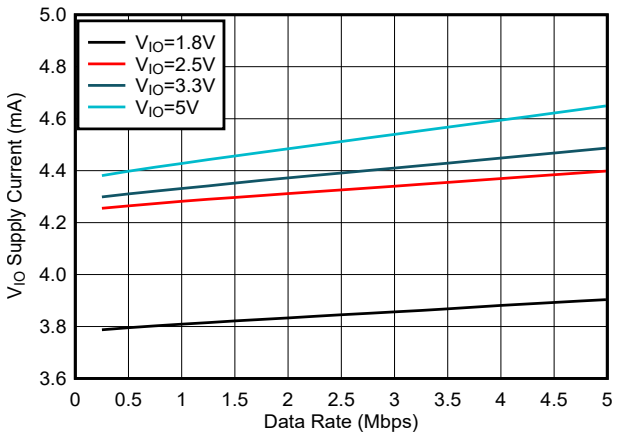
V_{ISOOUT} = 5 V STB = Low

Figure 8-3. V_{DD} Supply Current vs Datarate



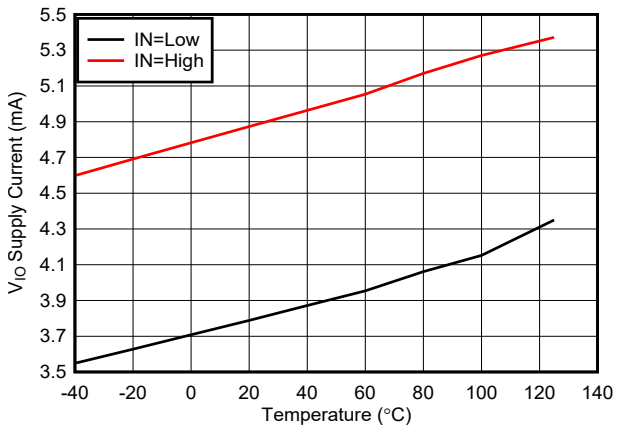
V_{DD} = 5 V STB = Low V_{ISOOUT} = 5 V

Figure 8-4. V_{DD} Supply Current vs Temperature



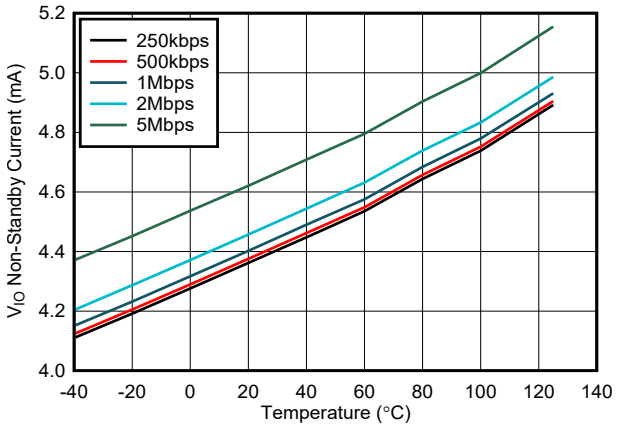
V_{ISOOUT} = 5 V STB = Low

Figure 8-5. V_{IO} Supply Current vs Datarate



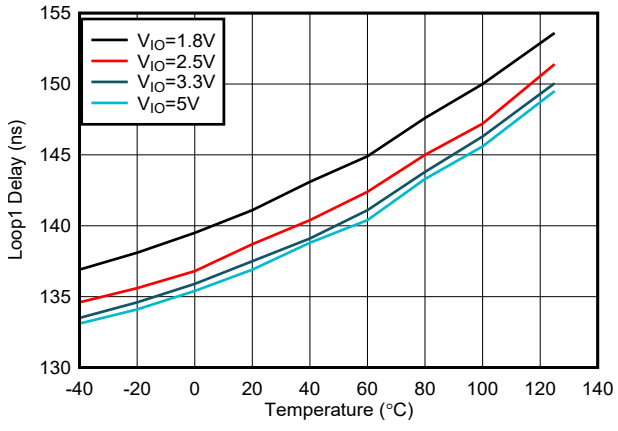
V_{DD} = 5 V STB = High V_{ISOOUT} = 5 V

Figure 8-6. V_{IO} Standby Current vs Temerature



V_{DD} = 5 V STB = Low V_{ISOOUT} = 5 V

Figure 8-7. V_{IOI} Non-standby Current vs Temperature

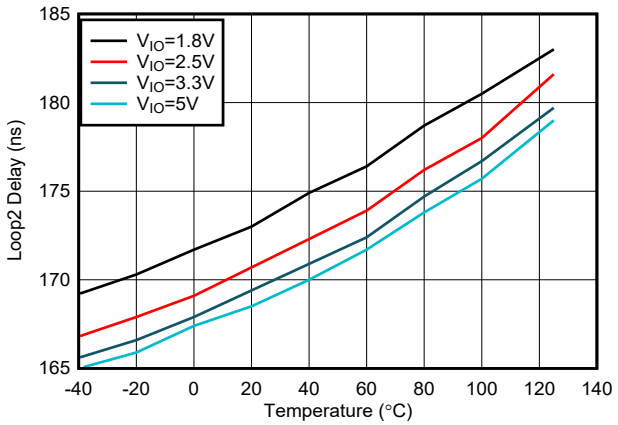


V_{DD} = 5 V STB = Low V_{ISOOUT} = 5 V
C_L = 100 pF

Figure 8-8. Loop Delay (Recessive to Dominant) vs Temperature

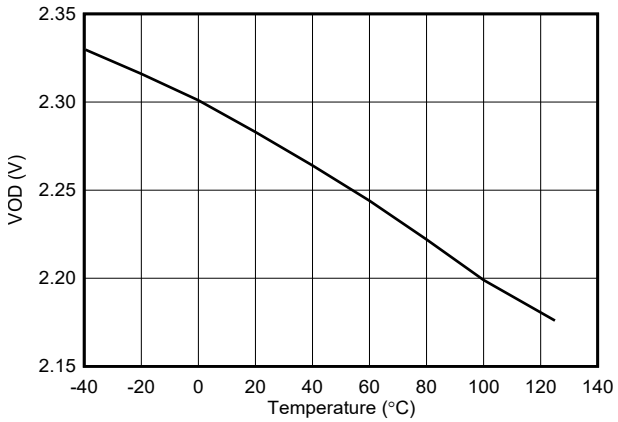
8.13 Typical Characteristics (continued)

V_{DD} = V_{IO} , V_{ISOIN} = V_{ISOOUT}, $C_{L(RXD)}$ = 15 pF , R_L = 60 Ω, T_A = 25°C unless otherwise noted.



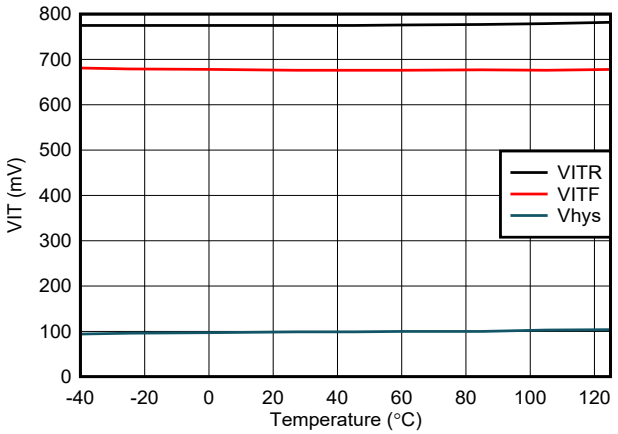
V_{DD} = 5 V STB = Low V_{ISOOUT} = 5 V
C_L = 100 pF

Figure 8-9. Loop Delay (Dominant to Recessive) vs Temperature



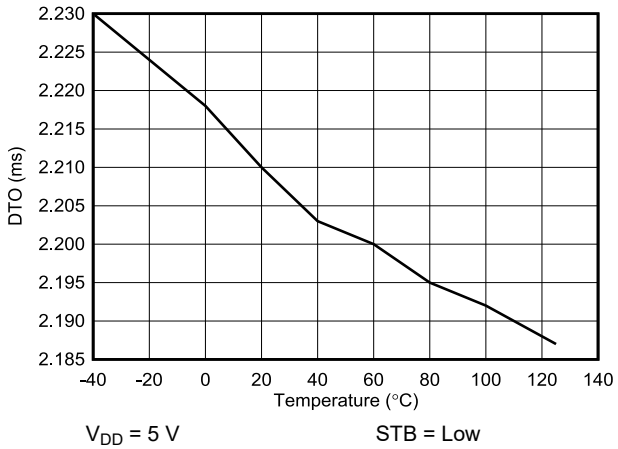
V_{DD} = 5 V STB = Low

Figure 8-10. Dominant state differential output voltage vs Temperature



V_{DD} = 5 V STB = Low

Figure 8-11. Receiver differential threshold voltage vs Temperature



V_{DD} = 5 V STB = Low

Figure 8-12. Dominant Timeout vs Temperature

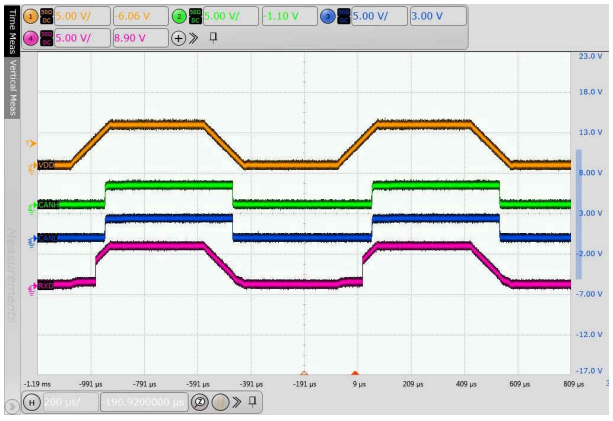


Figure 8-13. Glitch Free Power Up on VDD

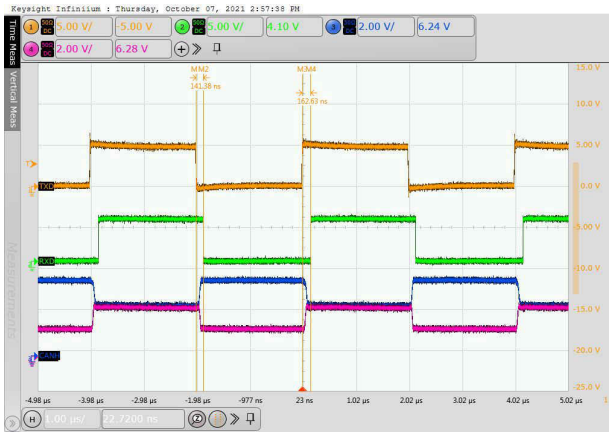


Figure 8-14. Typical TXD, RXD, CANH and CANL Waveforms at 500 kbps

8.13 Typical Characteristics (continued)

V_{DD} = V_{IO} , V_{ISOIN} = V_{ISOOUT}, $C_{L(RXD)}$ = 15 pF , R_L = 60 Ω, T_A = 25°C unless otherwise noted.

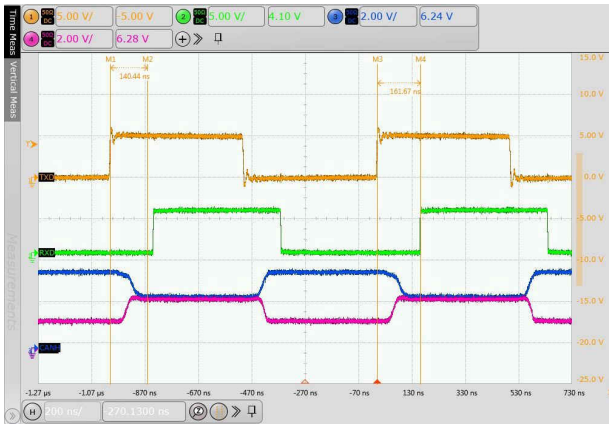


Figure 8-15. Typical TXD, RXD, CANH and CANL Waveforms at 2 Mbps

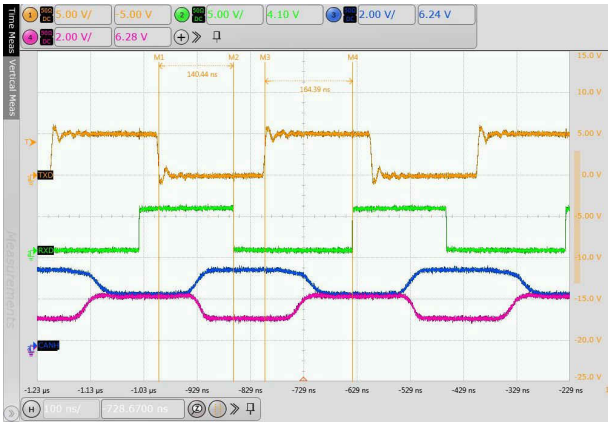


Figure 8-16. Typical TXD, RXD, CANH and CANL Waveforms at 5 Mbps

9 Parameter Measurement Information

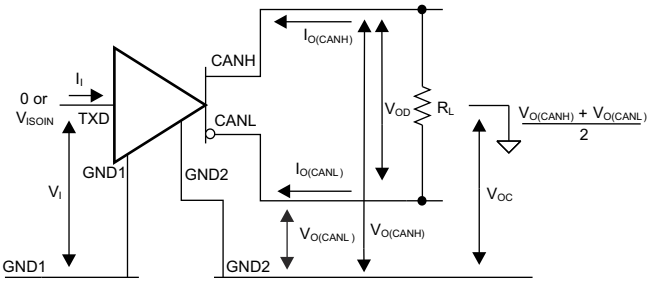


Figure 9-1. Driver Voltage, Current and Test Definitions

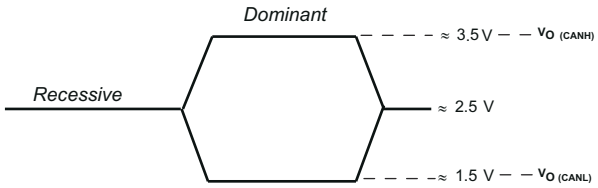
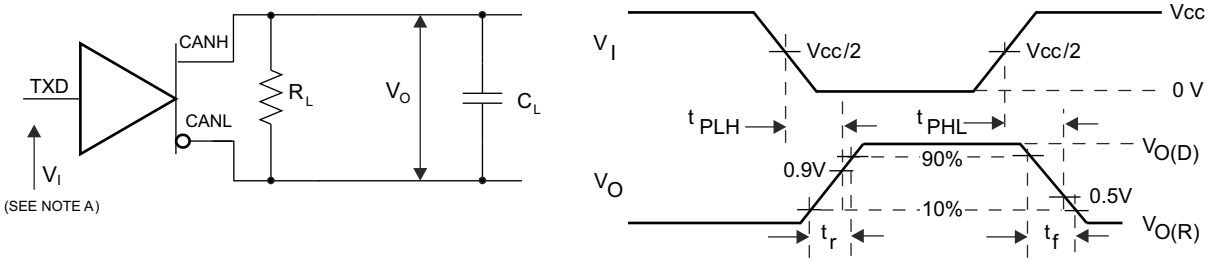


Figure 9-2. Bus Logic State Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6 ns, ZO = 50 Ω.

Figure 9-3. Driver Test Circuit and Voltage Waveforms

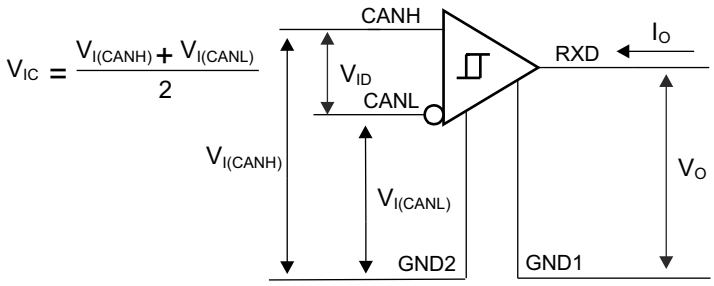
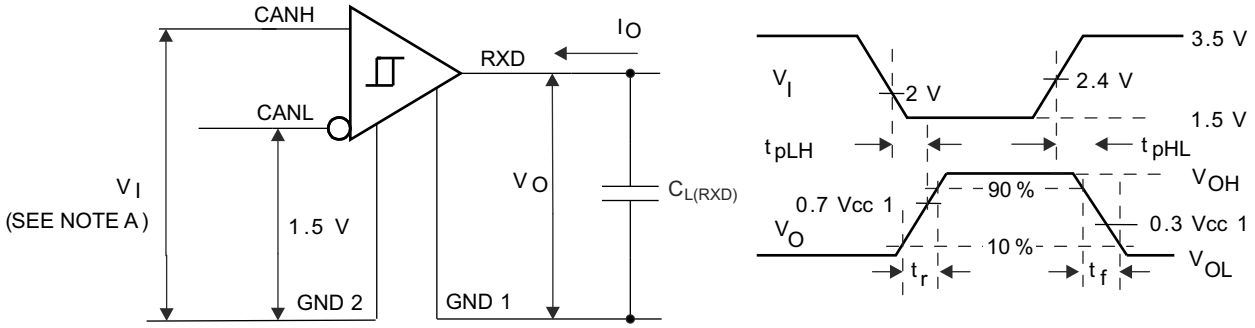


Figure 9-4. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 9-5. Receiver Test Circuit and Voltage Waveforms

Table 9-1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	RXD	
-11.5 V	-12.5 V	1000 mV	L	V_{OL}
12.5 V	11.5 V	1000 mV	L	
-8.55 V	-9.45 V	900 mV	L	
9.45 V	8.55 V	900 mV	L	
-8.75 V	-9.25 V	500 mV	H	V_{OH}
9.25 V	8.75 V	500 mV	H	
-11.8 V	-12.2 V	400 mV	H	
12.2 V	11.8 V	400 mV	H	
Open	Open	X	H	

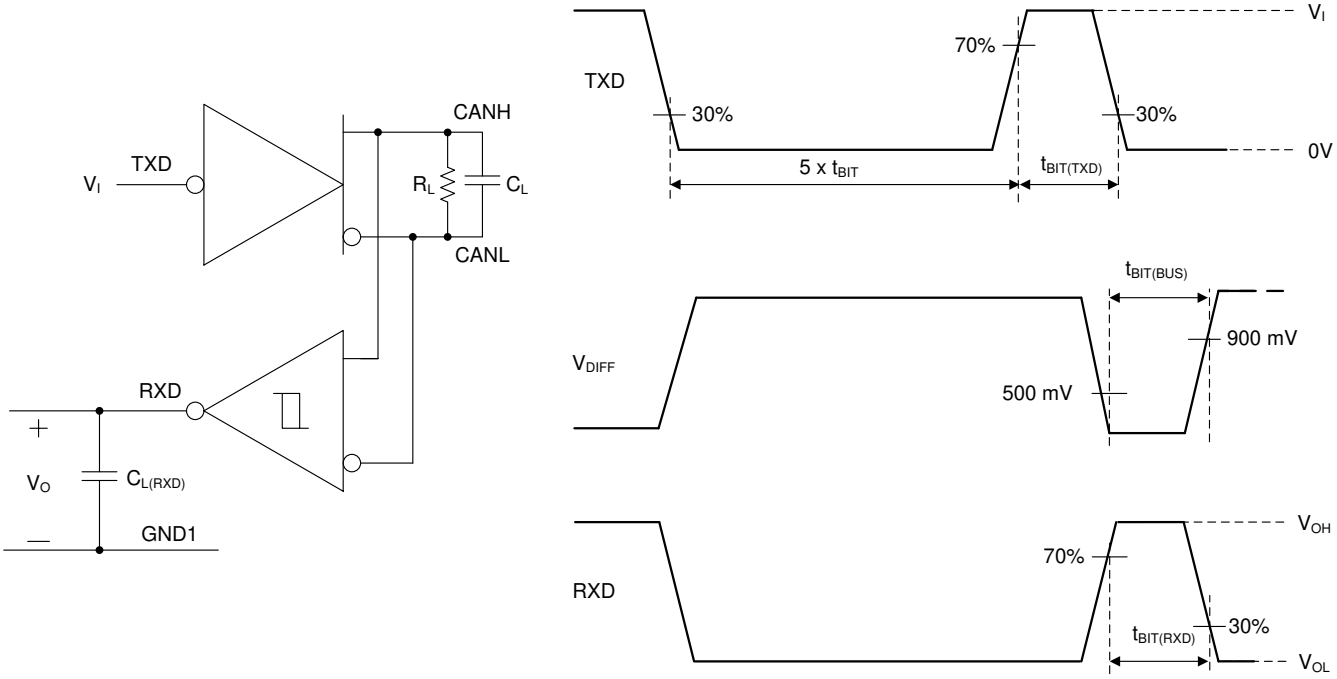
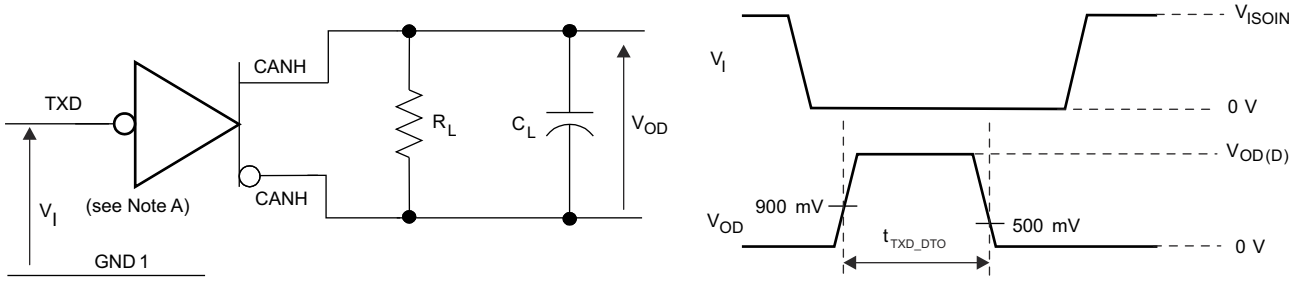


Figure 9-6. t_{LOOP} and CAN FD Timing Parameter Measurement



A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 9-7. Dominant Time-out Test Circuit and Voltage Waveforms

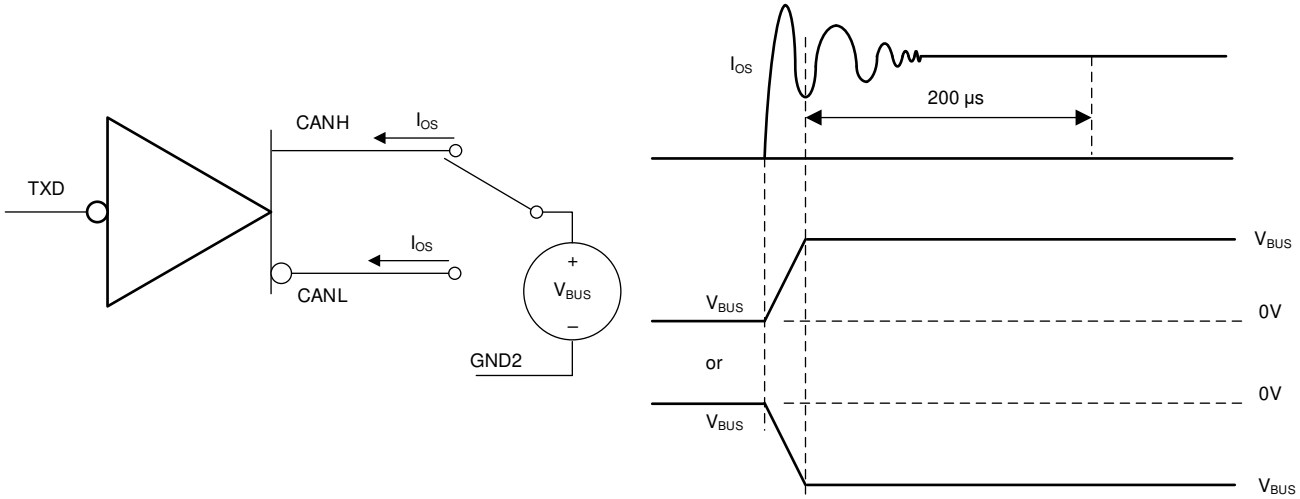


Figure 9-8. Driver Short-Circuit Current Test Circuit and Waveforms

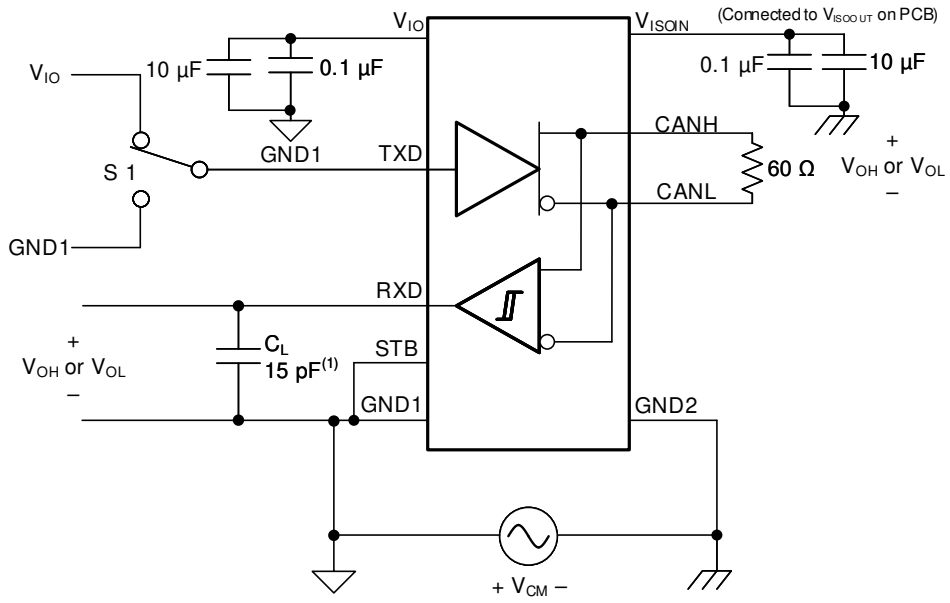
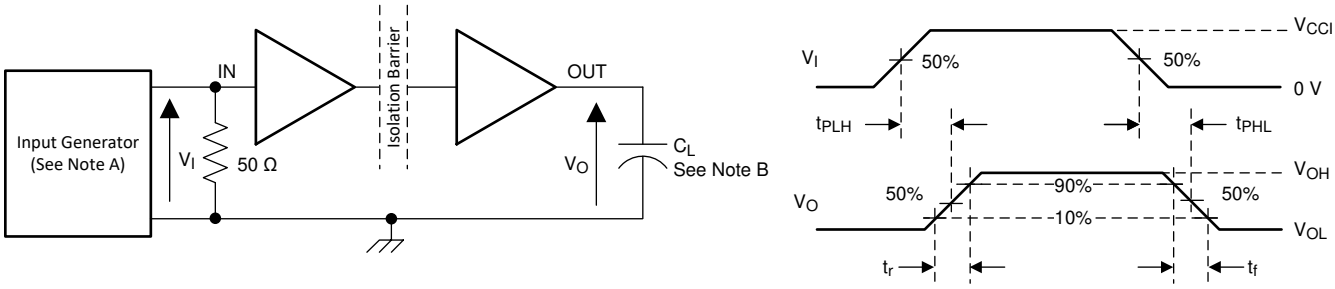


Figure 9-9. Common-Mode Transient Immunity Test Circuit



A. V_{CCI} and V_{CCO} refers to the power supplies V_{IO} and V_{ISOIN}, respectively. C_L = 15 pF and The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9-10. Switching Characteristics Test Circuit and Voltage Waveforms

10 Detailed Description

10.1 Overview

The ISOW1044 has signal isolation channels, power isolation with integrated transformer and CAN transceiver all integrated in one package. ISOW1044 supports maximum signaling rate up to 1Mbps for CAN, and 5 Mbps for CAN FD. Functional Block Diagram shows functional block diagram of ISOW1044.

10.2 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve upto 47% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. In case bus communication is not needed, the DC-DC converter can be switched off using EN pin to save power. The output voltage, V_{ISOOUT}, is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{IO}, V_{DD} and V_{ISOOUT} supplies which ensures robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

10.3 Signal Isolation

The integrated signal isolation channels for CAN tranceiver and GPIIO employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 10-3 shows a functional block diagram of a typical signal isolation channel.

In order to keep any noise coupling from power converter away from signal path, power supplies on side1 for power converter (V_{DD}) and signal path(V_{IO}) are kept separate. Similarly on side2, power converter output (V_{ISOOUT}) needs to be connected to power supply for CAN (V_{ISOIN}) externally on PCB. For more details, refer to Layout guidelines section.

10.4 CAN Transceiver

The ISOW1044 device includes a digitally isolated CAN transceiver that offers ±58-V DC bus fault protection and ±12-V common-mode voltage range. The device supports up to 5-Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. The power converter operates from a 5-V supply on side 1 (V_{DD}) and a 5-V supply on side 2 (V_{ISOOUT}). The logic supply V_{IO} on side 1 can operate from 1.71-V up to 5.5-V. This wide V_{IO} supply range is of particular advantage for applications operating in harsh industrial environments because the low voltage on side 1 enables the connection to low voltage microcontrollers for power conservation, whereas the 5 V on side 2 maintains a high signal-to-noise ratio of the bus signals.

The ISOW1044 supports a standby mode and remote BUS Wake-UP (WUP). The STB pin can be supplied from either the system processor or from a static system voltage source. In standby mode, the CAN driver and main receiver are switched off and bidirectional CAN communication is not possible. The DC-DC converter, low-power receiver, and bus monitor circuits are still enabled to allow for RXD wake-up requests via the CAN bus. The CAN bus pins are weakly pulled to GND in this mode. If normal mode is the only intended mode of operation than the STB pin can be tied directly to GND.

10.4.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The ISOW1044 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the ISOW1044.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 10-1 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 10-1 for the timing diagram of the wake-up pattern with wake timeout feature.

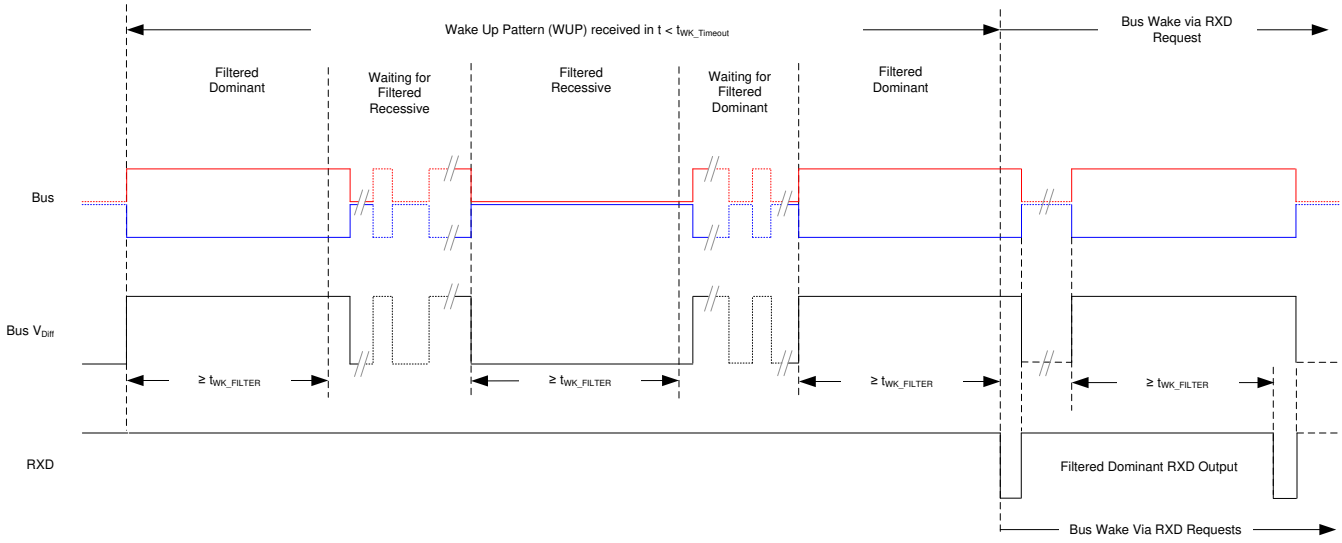


Figure 10-1. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

10.5 Functional Block Diagram

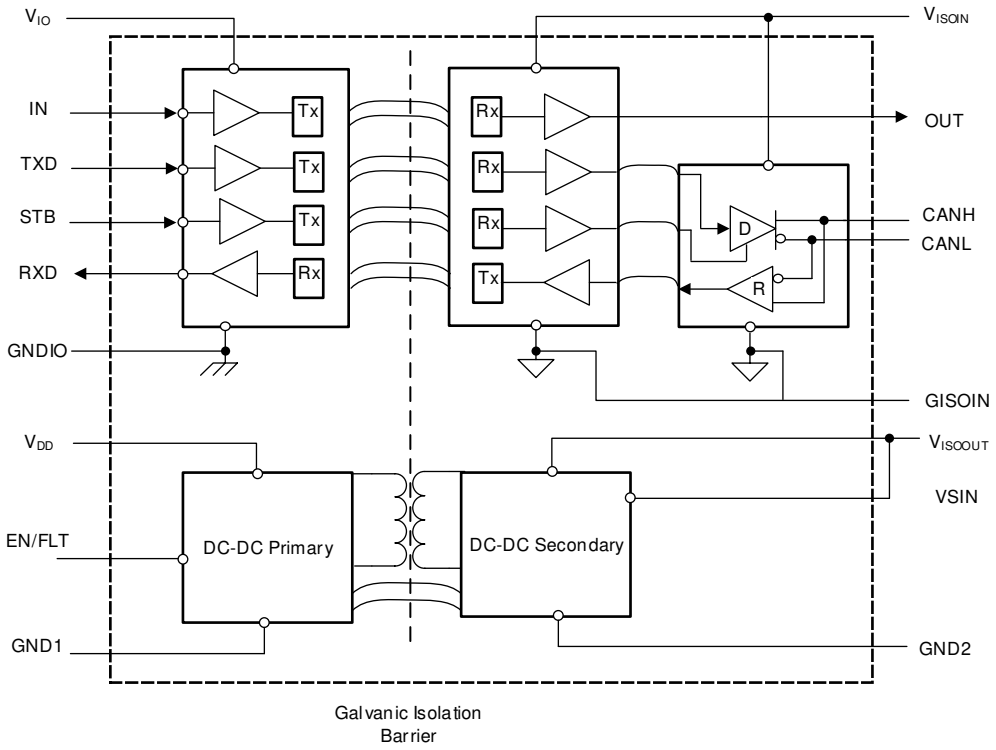


Figure 10-2. Block Diagram

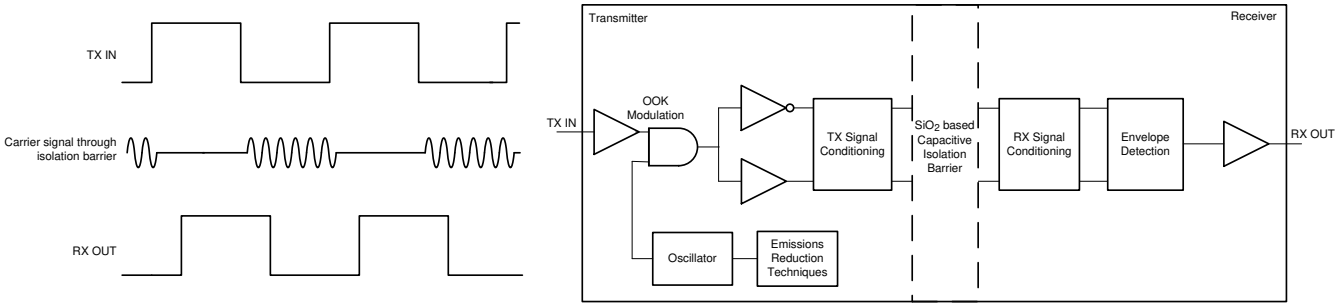


Figure 10-3. Signal Isolation channel

10.6 Feature Description

10.6.1 CAN Bus States

The CAN bus has two logical states during operation: *recessive* and *dominant*. A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The ISOW1044 transceiver implements a standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver.

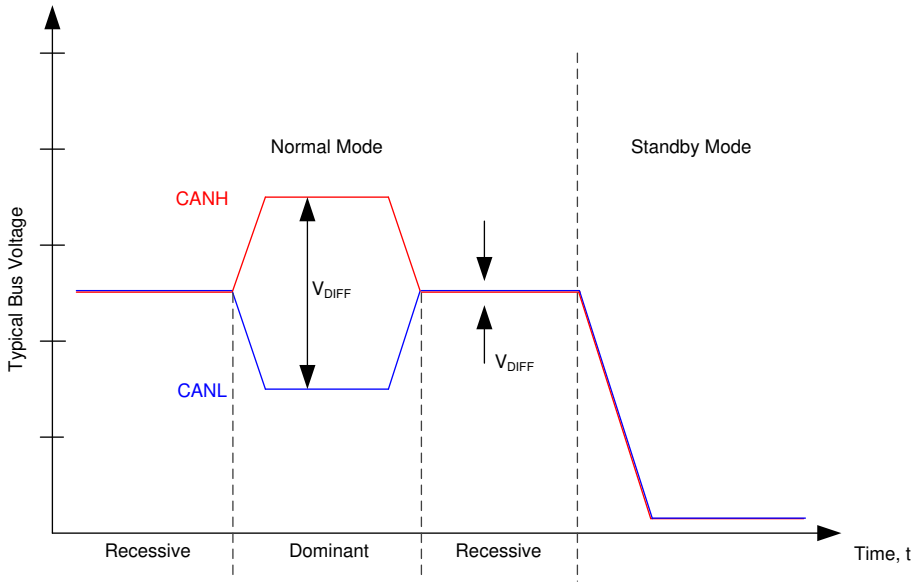


Figure 10-4. Bus States (Physical Bit Representation)

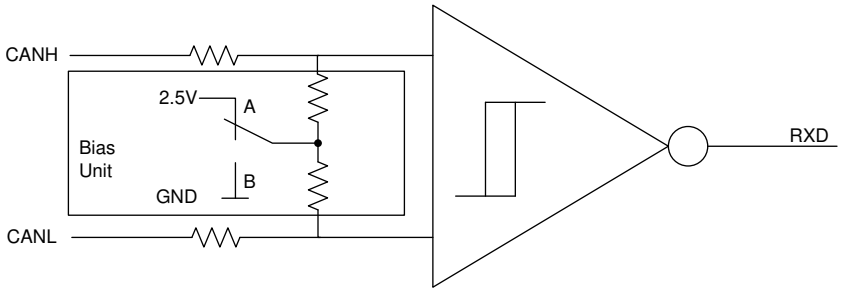


Figure 10-5. Simplified Recessive Common Mode Bias and Receiver

A. A - Normal Mode B - Standby Mode

10.6.2 Digital Inputs and Outputs: TXD (Input) and RXD (Output)

The V_{IO} supply for the isolated digital input and output side of the device can be supplied by 1.8-V, 2.5-V, 3.3-V, and 5-V supplies and therefore the digital inputs and outputs are 1.8-V, 2.5-V, 3.3-V, and 5-V compatible.

10.6.3 TXD Dominant Timeout (DTO)

The TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where the TXD pin is held dominant longer than the timeout period, t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on the TXD pin. The DTO circuit disables the CAN bus driver if no rising edge occurs before the timeout period expires, which frees the bus for communication between other nodes on the network. The CAN driver is activated again when a recessive signal occurs on the TXD pin, clearing the TXD DTO condition. The receiver and RXD pin still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

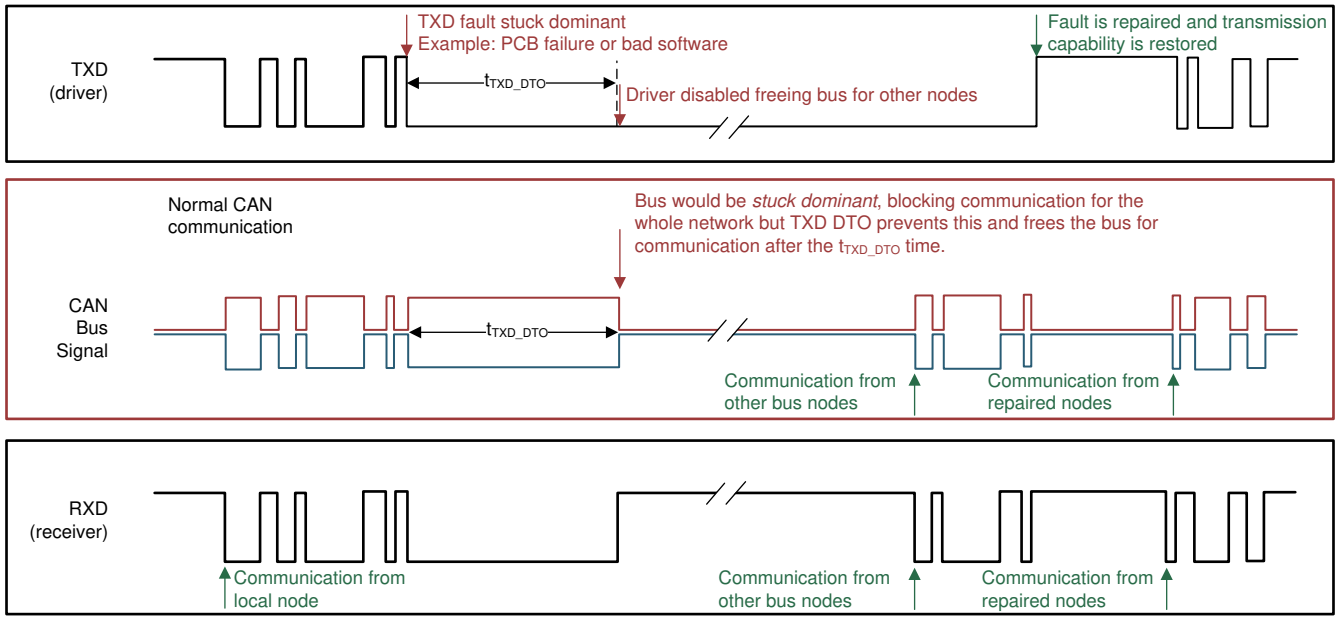


Figure 10-6. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time (t_{TXD_DTO}) allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate with Equation 1.

$$\text{Minimum Data Rate} = 11 / t_{TXD\_DTO} \quad (1)$$

10.6.4 *Power-Up and Power-Down Behavior*

The ISOW1044 has built-in under-voltage lockout (UVLO) on all supplies (V_{DD}, V_{IO} and V_{ISOOUT}) with positive-going and negative-going thresholds and hysteresis. Both the power converter supply (V_{DD}) and Logic supply (V_{IO}) need to be present for the device to work. If either of them is below its UVLO, both the signal path and the power converter are disabled.

Assuming V_{IO} is above its UVLO+, when the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. CAN BUS is in high impedance state in this duration. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, the feedback channel starts providing feedback to the primary controller. The regulation loop takes over and CAN drive output, Received data output (RXD) and gneral purpose logic channel (OUT) take their respective states defined by the inputs to the device i.e. Standby (STB), Driver data to be transmitted TXD, and general purpose logic input IN respectively. Designers should consider a sufficient time margin (typically 5 ms with 10-µF load capacitance) to allow this power up sequence before any usable system functionality.

When either of V_{DD} or V_{IO} is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the isolation channels and BUS load.

10.6.5 *Protection Features*

The ISOW1044 device has multiple protection features to create a robust system level solution.

- The first feature is an Enable/Fault protection feature. This EN/FLT pin can be used as either an input pin to enable or disable the integrated DC-DC power converter or as an output pin which works as an alert signal if the power converter is not operating properly. In the /Fault use case, a fault is reported if V_{DD} > 7 V, V_{DD} < 2.5 V, or if the junction temperature >170°C. When a fault is detected, this pin will go low, disabling the DC-DC converter to prevent any damage.

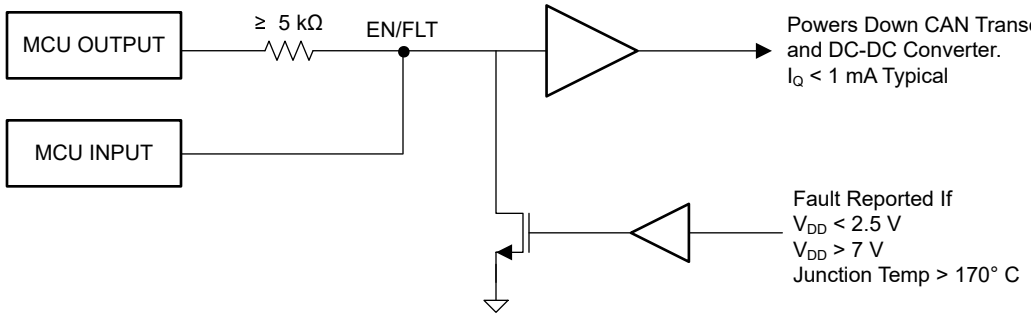


Figure 10-7. EN Fault Pin Diagram

- An over-voltage clamp feature is present on V_{ISOOUT} which will clamp the voltage at 6 V if there is an increase in voltage seen. For device reliability, it is recommended that V_{ISOOUT} stays lower than the over-clamp voltage for device reliability.
- Over-Voltage Lock Out (OVLO) on V_{DD} will occur when a voltage higher than 7 V on V_{DD} is seen. At OVLO, the device will go into a low power state and the EN/FLT pin will go low.
- In cases of overload or short on power converter output V_{ISOOUT}, maximum duty cycle of power converter is limited. In cases of driver bus short circuit due to the external power supply cable shorting to the bus cable, short circuit current protection on CAN chip restricts the bus current to ±115 mA maximum.
- Thermal protection is also integrated to help prevent the device from getting damaged under such scenarios. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 165 ℃ (typical), thus disabling the short condition. The device is re-enabled when the junction temperature becomes 155 ℃ (typical). If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the system design to prevent repeated or prolonged exposure to bus shorts as this exposes the device to high junction temperatures for extreme amounts of time affecting device reliability.

10.6.6 *Floating Pins, Unpowered Device*

The ISOW1044 is designed to be ideal passive or no load to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus which is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The device has internal pull-ups on critical pins (TXD and STB) which places the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature. When a CAN controller supporting open drain outputs is used, an adequate external pull-up resistor must be used to ensure that the TXD output of the CAN controller maintains adequate bit timing to the input of the CAN transceiver. See Table 10-3 for more details.

10.6.7 *Glitch-Free Power Up and Power Down*

Communication on the bus that already exist between a master node and slave node in a CAN network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus should occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and recessive state
- Powered up or powered down in a recessive state when already connected to the bus

The ISOW1044 device meets above criteria and does not cause any false data toggling on the bus when powered up or powered down in a recessive state with supply ramp rates >= 50 us.

10.7 Device Functional Modes

Table 10-1 lists the supply configuration for these devices:

Table 10-1. Supply configuration Function Table

INPUTS			OUTPUTS		
V_{DD}	V_{IO}	EN/FLT	BUS OUTPUT (CANH/ CANL)	RXD	V_{ISOOUT} (2)
< $V_{DD(UVLO+)}$	>$V_{IO(UVLO+)}$	X	High-Z	Recessive (Default High)	OFF
>$V_{DD(UVLO+)}$	<$V_{IO(UVLO+)}$	X	High-Z	Recessive (Default High)	Invalid Operation
5 V	1.71 V to 5.5 V	H or Open	Per Device Mode (1) and TXD	Mirrors Bus	5 V
5 V	1.71 V to 5.5 V	L	High-Z	Recessive (Default High)	OFF

(1) At Normal mode (STB = L), BUS OUTPUT follows TXD. Otherwise if at Standby mode (STB = H or Open), BUS OUTPUT is High-Z.
(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GND2 and GISOIN pins are shorted together and EN/FLT = High.

Table 10-2 shows the different driver functional modes:

Table 10-2. Driver Functional Table

INPUTS					OUTPUTS		
V_{DD} (1)	V_{IO}	EN/FLT	STB	INPUT TXD	CANH (3)	CANL (3)	DRIVEN BUS STATE
PU	PU	H or Open	L	L	H	L	Dominant
				H or Open	Z	Z	Recessive
			H or Open	X	Hi-Z	Hi-Z	Weak pull-down to ground
		L	X	X	Hi-Z	Hi-Z	Weak pull-down to ground
PD	PU	X	X	X	Hi-Z	Hi-Z	Weak pull-down to ground
PU	PD(2)	X	X	X	Invalid Operation		

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Z = common-mode (recessive) biased to V_{ISOIN}/2 , Hi-Z=High impedance state
(2) A strongly driven input signal on TXD can weakly power the floating V_{IO} through an internal protection diode and cause an undetermined output.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and GND2 and GISOIN pins are shorted together and EN/FLT = High

At Normal mode (STB = L), the CAN outputs follow the logic states at data input, TXD. A logic low at the TXD input causes the CAN output to go dominant. Therefore the differential output voltage defined by Equation 2 is positive. A logic high at the TXD input causes the CAN BUS to go recessive. Therefore the differential output voltage defined by Equation 2 is negative.

$$V_{OD} = V_{CANH} - V_{CANL} \quad (2)$$

At Standby mode (STB = H or Open), both outputs go to the high-impedance (Hi-Z) state. The logic state at the TXD pin is irrelevant when this mode. The driver is disabled (bus outputs are in the Hi-Z) by default when the STB pin is left open. The TXD pin has an internal pullup resistor.

Table 10-3 shows the different receiver functional modes:

Table 10-3. Receiver Functional Table

INPUTS						OUTPUT
V_{DD} (1)	V_{IO}	EN/FLT	STB	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH}$-V_{CANL}	BUS STATE	RXD (3)
PU	PU	H or Open	L	V_{ID} > 0.9 V	Dominant	L
				0.5 V< V_{ID} < 0.9 V	Undefined	Undefined
				V_{ID} < 0.5 V	Recessive	H
			H or Open	V_{ID} > 1.15 V	Dominant	H (L if a remote wake event occurred)
				0.4 V< V_{ID} < 1.15 V	Undefined	
				V_{ID} < 0.4 V	Recessive	
			X	Open (V_{ID} = 0 V)	Open	H
		L	X	X	X	Hi-Z
PD	PU	X	X	X	X	Hi-Z
PU	PD(2)	X	X	X	X	Invalid Operation

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) A strongly driven input signal on TXD can weakly power the floating VIO through an internal protection diode and cause an undetermined output.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GND2 and GISOIN pins are shorted together and EN/FLT = High

At Normal mode (STB = L), the receiver output, RXD, goes low when the differential input voltage defined by Equation 3 is greater than the positive input threshold, V_{IT+}. The receiver output, RXD, goes high when the differential input voltage defined by Equation 3 is less than the negative input threshold, V_{IT-} . If the V_{ID} voltage is between the V_{IT+} and V_{IT-} thresholds, the output is indeterminate.

$$V_{ID} = V_{CANH} - V_{CANL} \quad (3)$$

At Standby mode (STB = H or Open), RXD output goes high and if a remote wake-up event occurs, it goes low.

Other device feature functional states are shown inTable 10-4 and Table 10-5 below:

Table 10-4. DC-DC Converter Enable/Disable

INPUTS			OUTPUT
V_{DD}	V_{IO}	EN/FLT	V_{ISOOUT}
PU	PU	H or Open	5 V
PU	PU	L	OFF

Table 10-5. General Purpose Logic Input/Output

INPUTS				OUTPUT	CommentsComments
V_{DD} (1) (2)	V_{IO}	EN/FLT	IN	OUT	
PU	PU	H or Open	H	H	Output channel assumes logic state governed by IN
			L	L	
			Open	L	Default state
		L	X	Hi-Z	Device is in disabled state when either of V_{DD} or V_{IO} is missing
PD	PU	X	X	Hi-Z	
PU	PD	X	X	Invalid Operation	

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state
(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GND2 and GISOIN pins are shorted together and EN=High

10.8 Device I/O Schematics

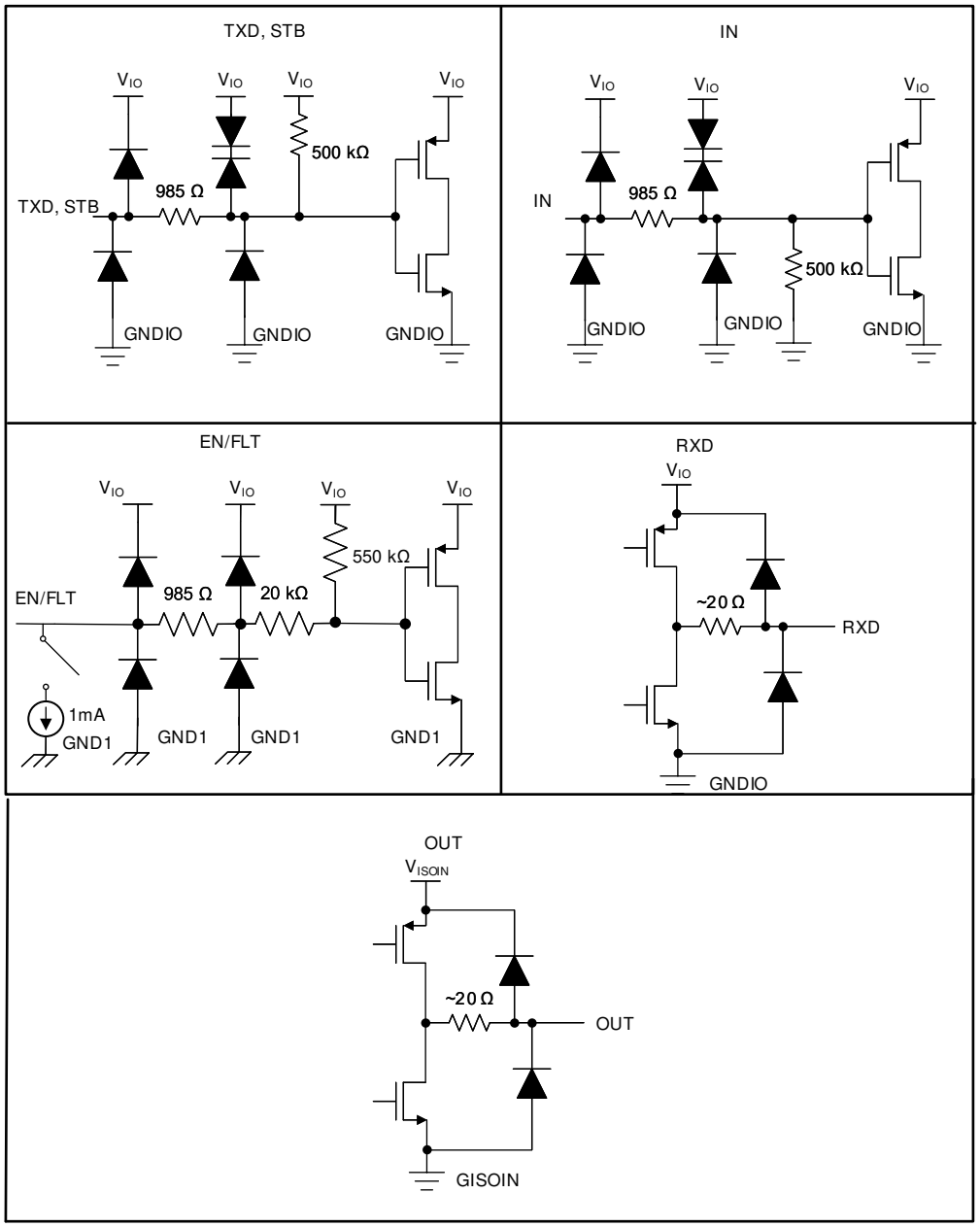


Figure 10-8. Device I/O schematics

11 Application and Implementation

Note

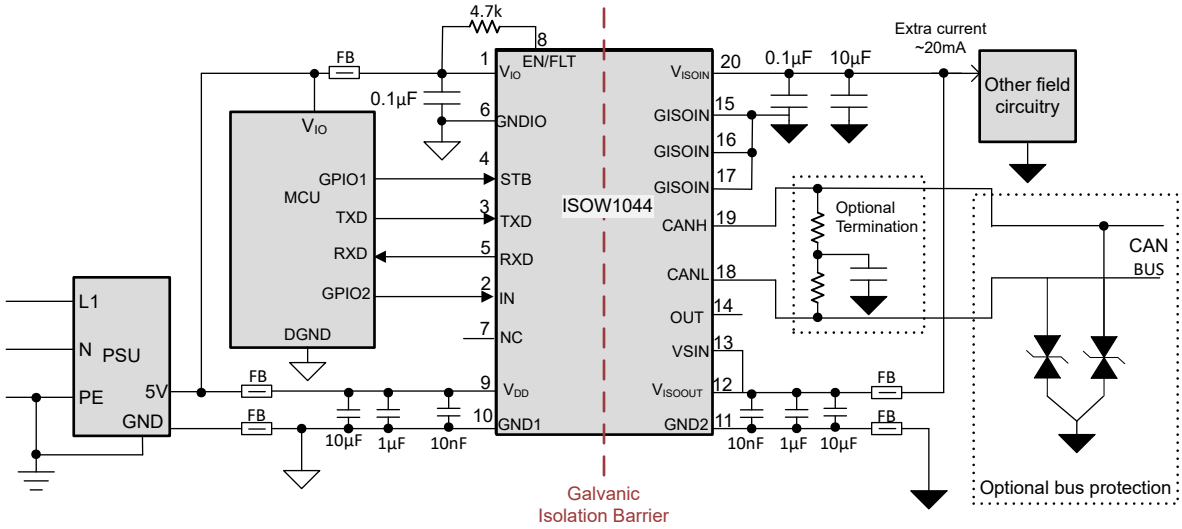
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The ISOW1044 device can be used with other components from Texas Instruments such as a microcontroller and a linear voltage regulator to form a fully isolated CAN interface. Typically two power supplies isolated from each other are needed to power up both sides of Isolated CAN device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the CAN device and peripherals on isolated side, thus saving board space.

11.2 Typical Application

The ISOW1044 device is suitable for applications that have limited board space and desire more integration. It is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The device can be used in applications with a host micro-controller or FPGA that includes the link layer portion of the CAN protocol. Figure 11-1 shows a typical application configuration for 5 V controller applications. The bus termination is shown for illustrative purposes. The ISOW1044 device meets 8 kV contact ESD (Electrostatic discharge) per IEC 61000-4-2 standalone with no external components on bus. If the application requires the usage of Common mode choke (CMC) , then use of Transient voltage suppressor (TVS) is a must to achieve 8kV IEC ESD.



Notes:
1. Keep 10 nF bypass capacitors close to V_{DD} and V_{ISOOUT} pins (< 1 mm) for optimum Radiated emissions performance
2. GND1 and GNDIO need be shorted directcly. GND2 and GISOIN need be shorted directly, or through ferrite beads.
3. All GISOIN pins (pin 15, 16, 17) need be shorted on PCB for optimum IEC-ESD performance.
4. V_{SIN} and V_{ISOOUT} must be shorted on PCB.

Figure 11-1. Application circuit for ISOW1044

11.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISOW1044 device only requires external bypass capacitors to operate as shown in above application diagram.

Because of very-high current flowing through the device V_{DD} and V_{ISOOUT} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10-µF capacitor is adequate, higher decoupling capacitors (such as 47 µF) on both the V_{DD} and V_{ISOOUT} pins to the respective grounds are strongly recommended to achieve the best performance.

11.2.2 Detailed Design Procedure

11.2.2.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the ISOW1044 transceiver.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 Standard. These organizations and standards have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

The ISOW1044 device is specified to meet the 1.5-V requirement with a 50-Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the device is a minimum of 30 kΩ. If 100 ISOW1044 transceivers are in parallel on a bus, this requirement is equivalent to a 300-Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60 Ω gives an equivalent loading of 50 Ω. Therefore, the ISOW1044 device theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity, therefore a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data-rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes, and a significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. Using this flexibility requires the responsibility of good network design and balancing these tradeoffs.

11.2.2.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes are removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

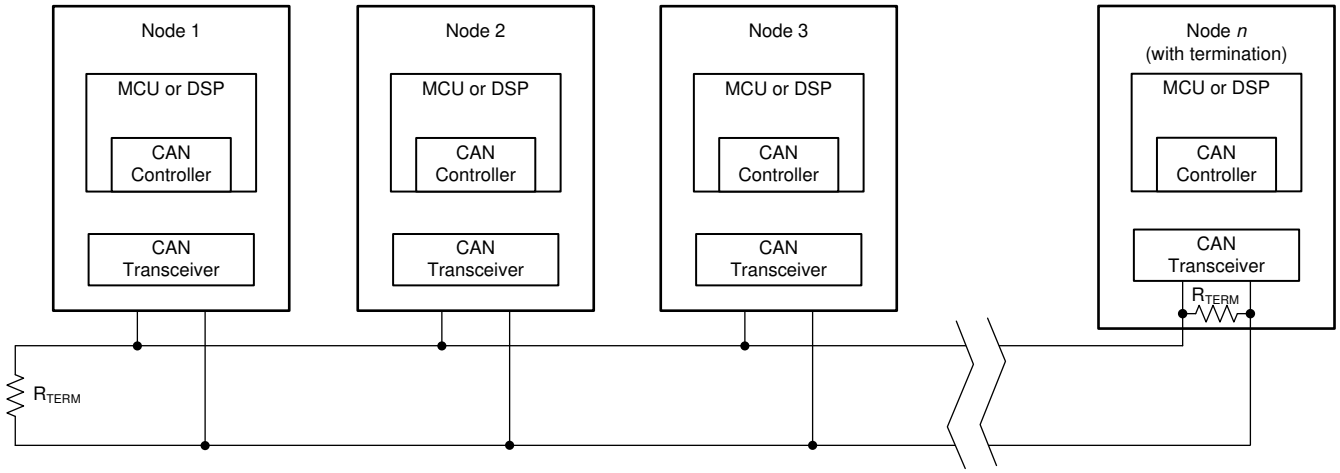


Figure 11-2. Typical CAN Bus

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used as below termination concepts. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

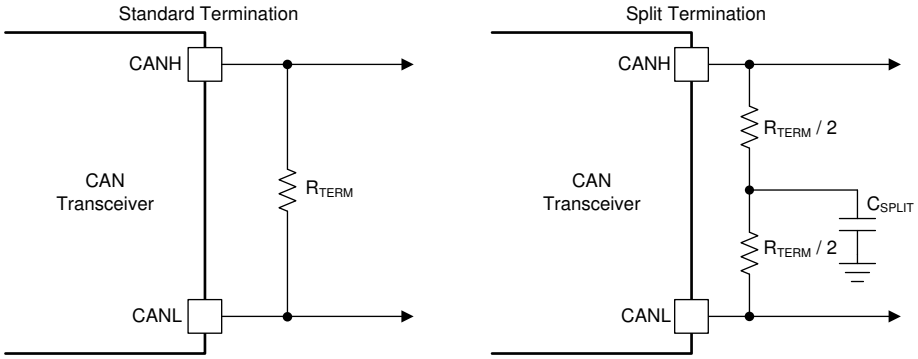
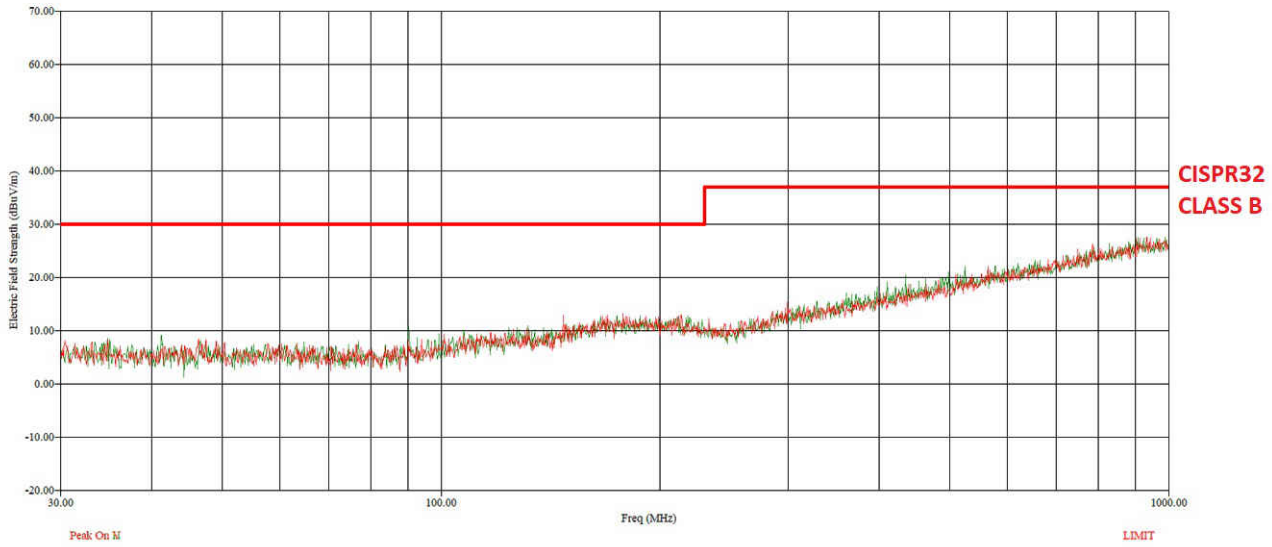


Figure 11-3. CAN Bus Termination Concepts

11.2.3 Application Curve



Red: Peak vertical scan. Green: Peak horizontal scan

V_{DD} = 5 V V_{ISOOUT} = 5 V Data rate = 1 Mbps

Figure 11-4. ISOW1044 Radiated Emissions versus CISPR32B line

11.2.4 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 11-5 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value. Figure 11-6 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime of 1184 years.

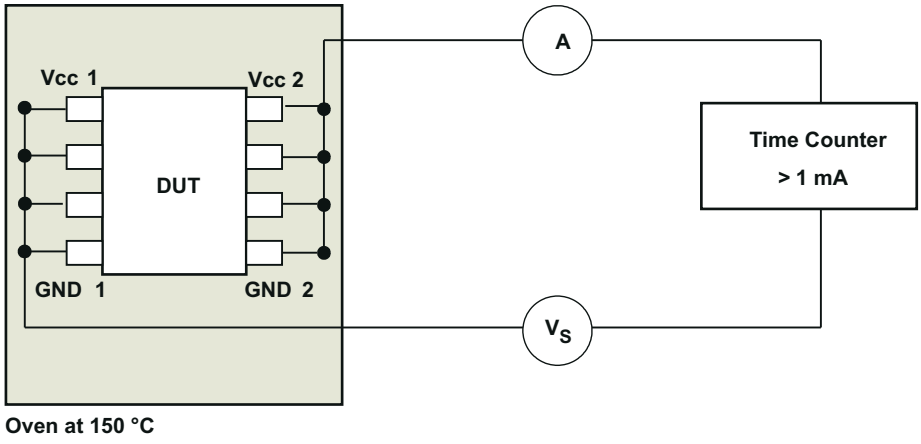


Figure 11-5. Test Setup for Insulation Lifetime Measurement

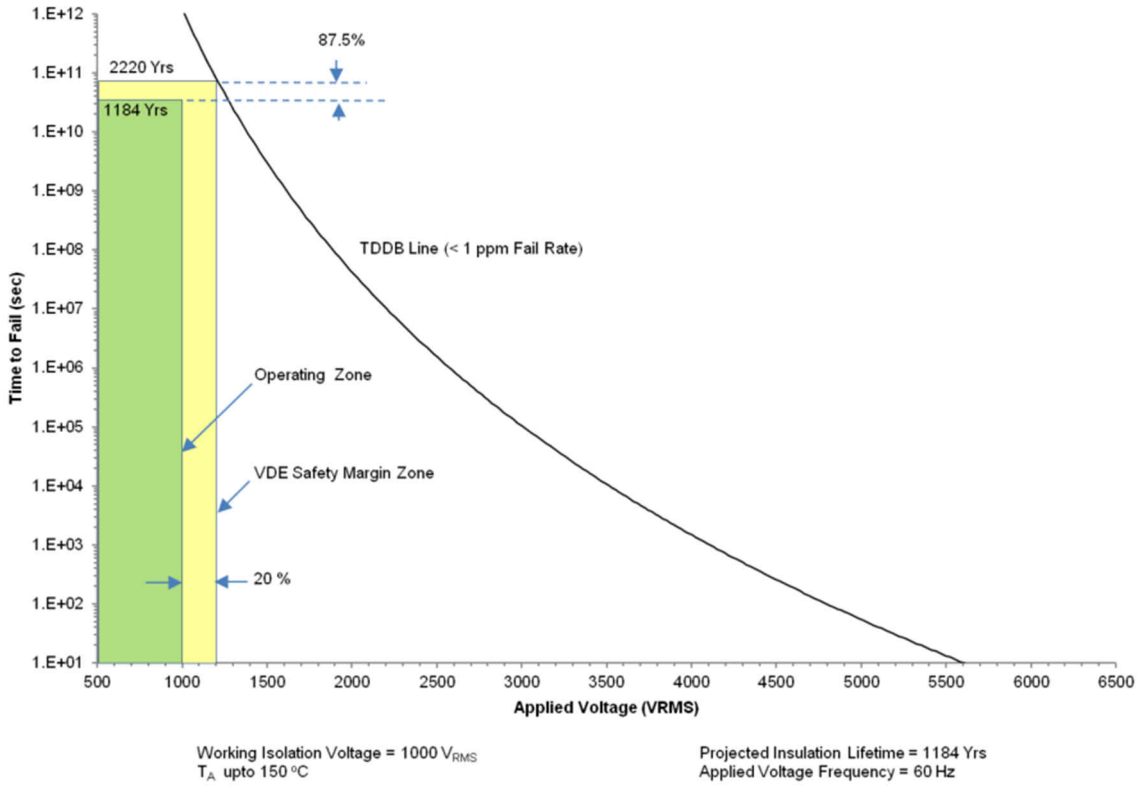


Figure 11-6. Insulation Lifetime Projection Data

12 Power Supply Recommendations

To make sure that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input V_{DD} and output V_{ISOOUT} supply pins should have high frequency ceramic capacitors 10 nF and bulk capacitors 10 µF atleast close to the pins. Signal path supply pins, V_{IO} and V_{ISOIN} , should have 100 nF or higher value ceramic bypass capacitors close to device pins. ISOW10144 can consume typical peak pulse currents of upto 250mA under fully loaded conditions for short durations (10s of µs) from the power source that is powering V_{DD} of ISOW1044. Please make sure the current limit of upstream power device is atleast 300mA typical.

13 Layout

13.1 Layout Guidelines

Figure 11-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to achieve low emissions design:

1. High frequency bypass capacitors 10 nF must be placed close to V_{DD} and V_{ISOOUT} pins, within 1 mm distance away from device pins. This is very essential for optimised radiated emissions performance. Ensure that these capacitors are 0402 size so that they offer least inductance (ESL).
2. Bulk capacitors of atleast 10 µF must be placed on power converter input (V_{DD}) and output (V_{ISOOUT}) supply pins after the 10 nF capacitor with a distance of 2 - 4 mm, as shown in Layout Example.
3. Traces on V_{DD} and GND1 must be symmetric till bypass capacitors. Similarly traces on V_{ISOOUT} and GND2 must be symmetric.
4. Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on power supply pins, one between V_{ISOOUT} and V_{ISOIN} and the other between GND2 (pin 11) and GND2(pin 15), as shown in example PCB layout, so that any high frequency noise from power converter output sees a high impedance before it goes to other components on PCB.
5. Do not have any metal traces or ground pour within 4 mm of power converter output terminals V_{ISOOUT} (pin12) and GND2 (pin11).
6. Place the CAN BUS protection and filtering circuitry close to the bus connector to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows two optional 68pF bus filter capacitors
7. Common mode choke or ferrite beads on bus terminals (CANH/CANL) can minimise any high frequency noise that can couple of CAN bus cable which can act as antenna and amplify that noise. This will improve Radiated emissions performance on a system level.
8. Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design. EVM Link is available in Related Documentation.

13.2 Layout Example

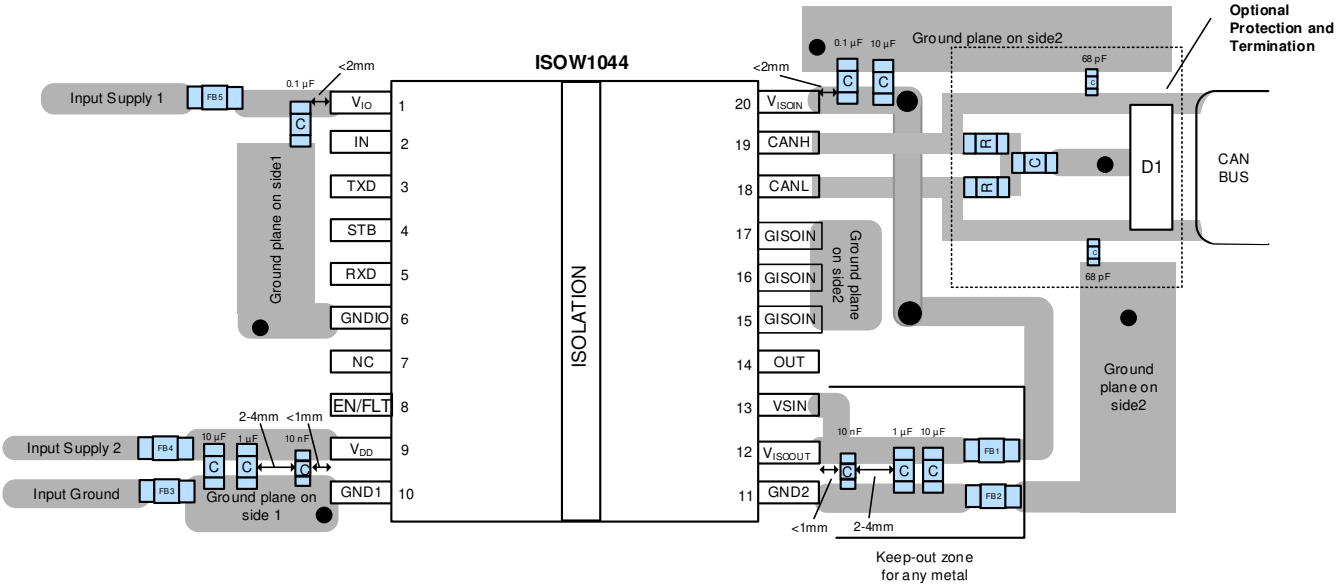


Figure 13-1. Layout example

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- **ISOW1044DFM** Evaluation board

14.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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14.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

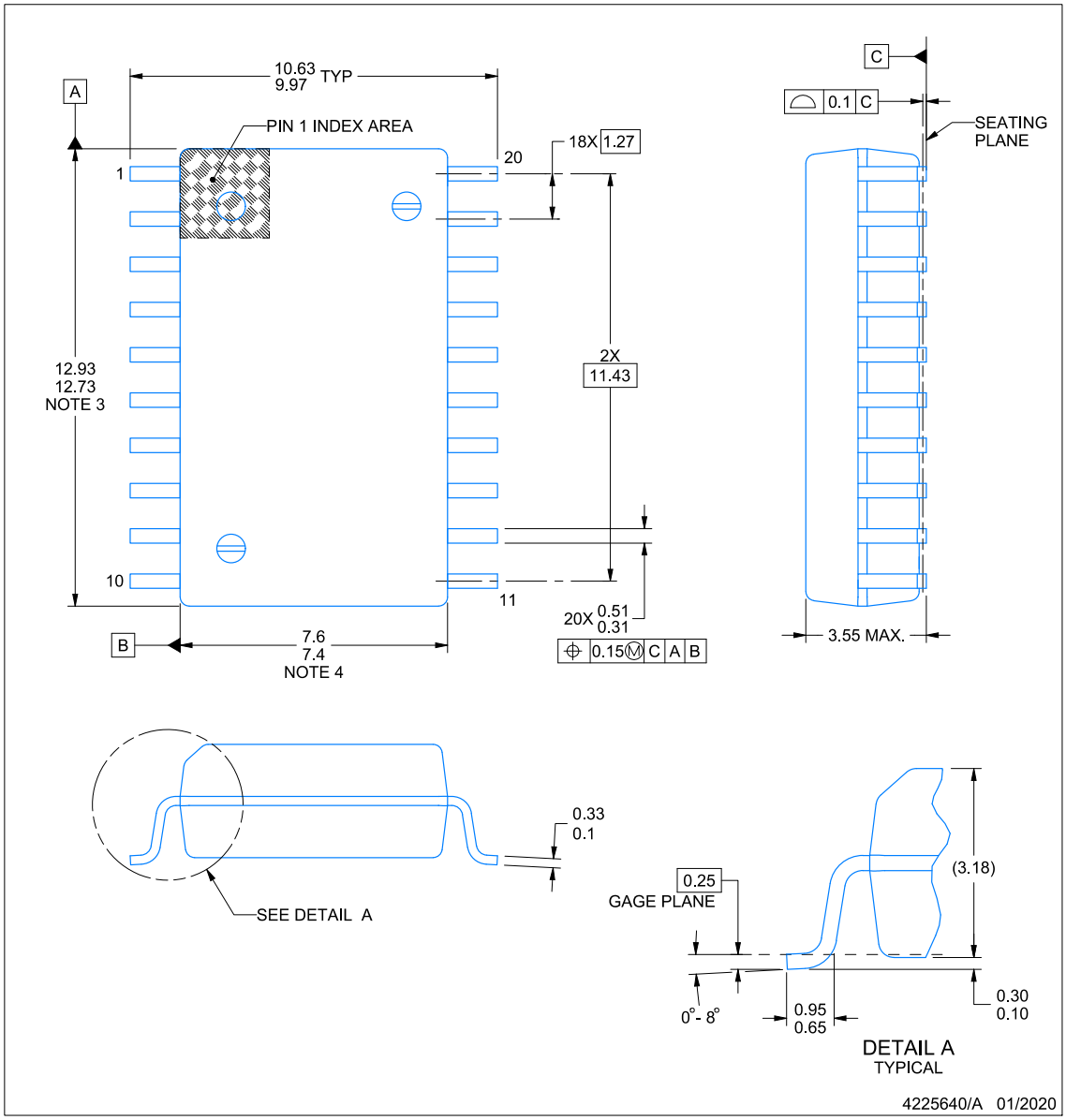
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

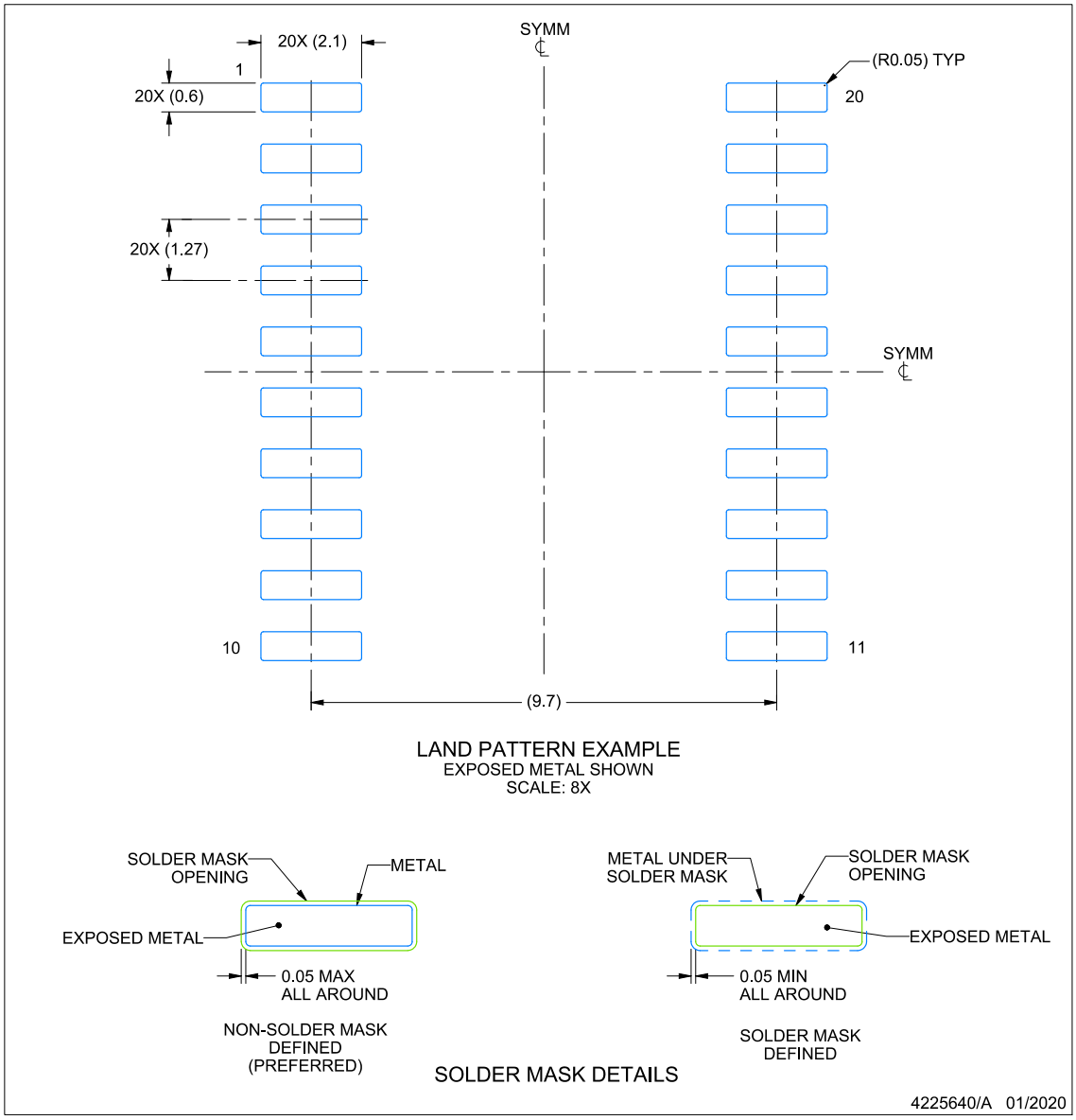
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



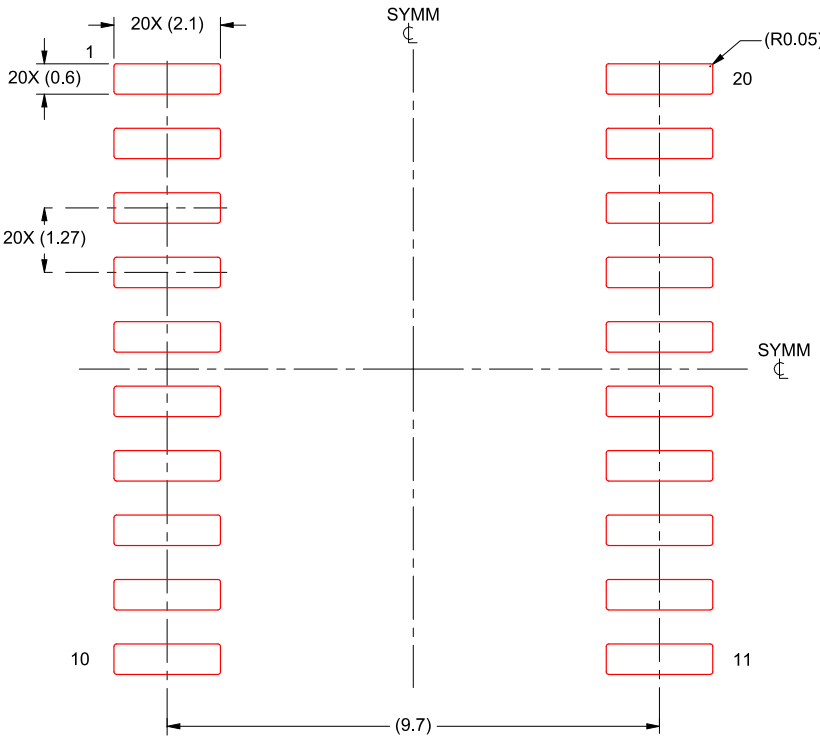
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFM0020A — **SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOW1044BDFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1044	Samples
ISOW1044DFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1044	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

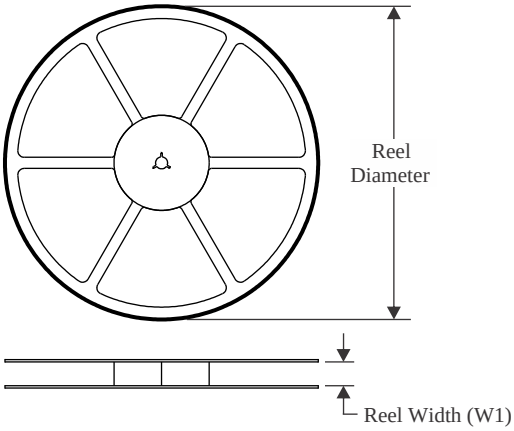
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

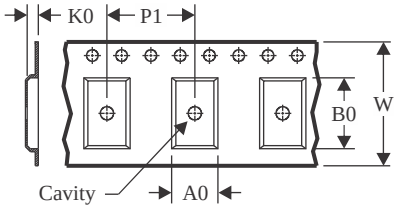
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

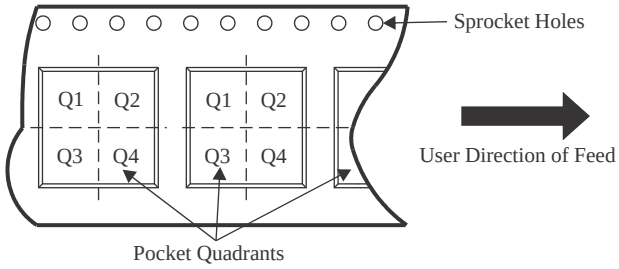


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

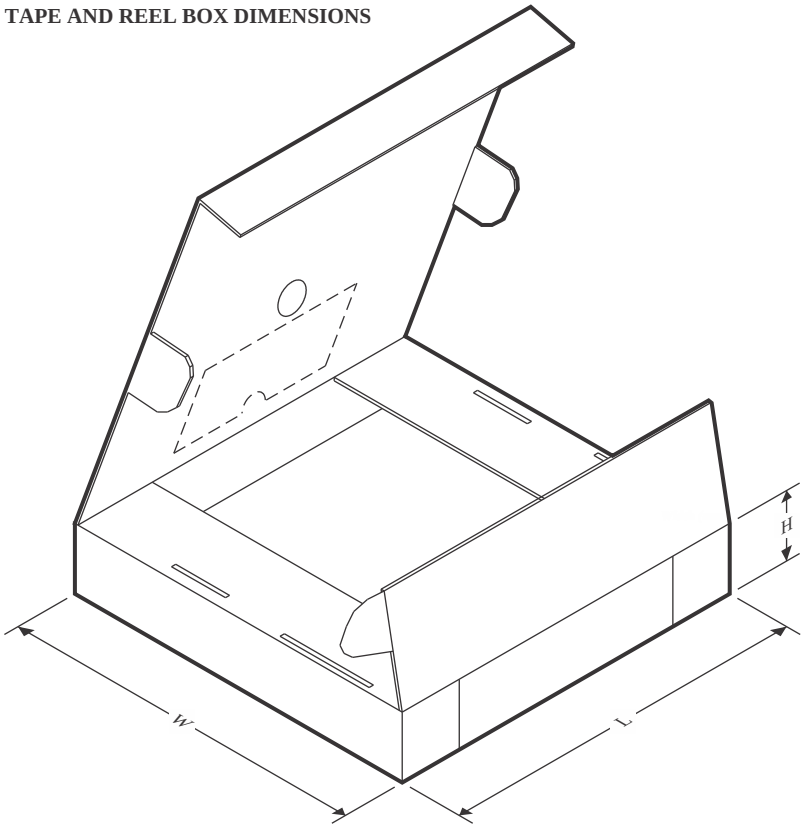
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW1044BDFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1044DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

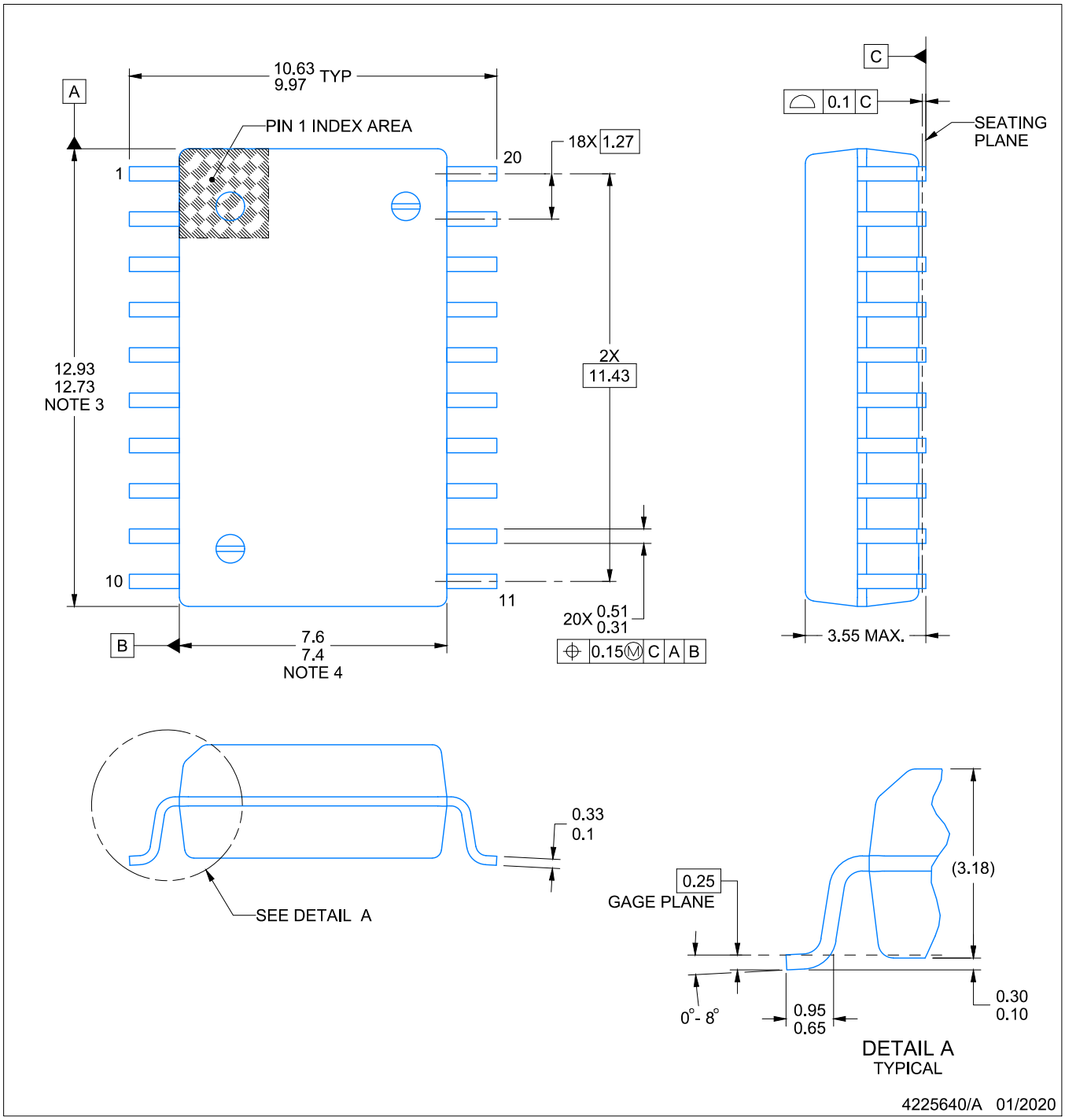
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW1044BDFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1044DFMR	SOIC	DFM	20	850	350.0	350.0	43.0

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



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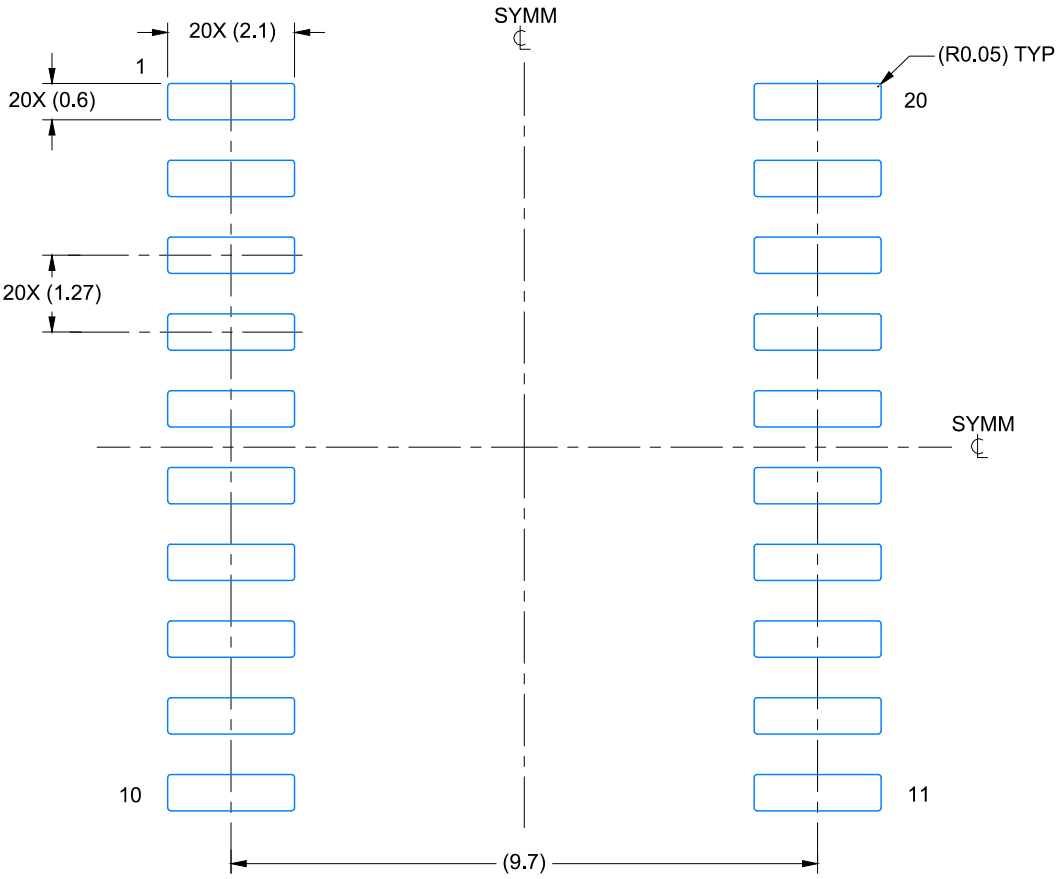
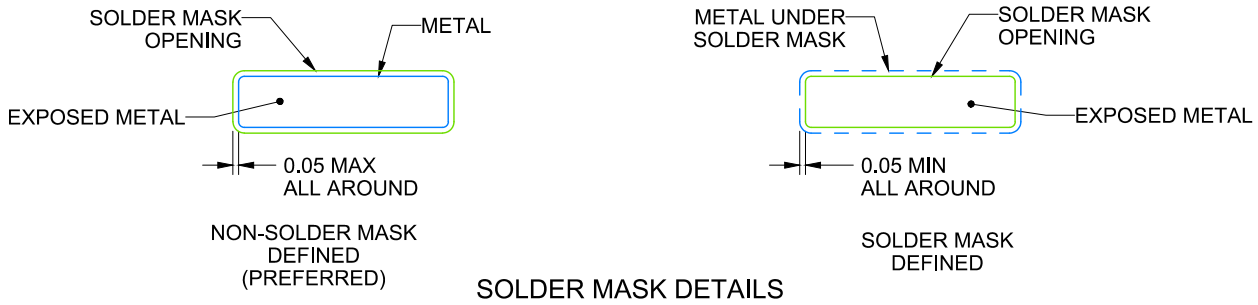


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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NOTES: (continued)

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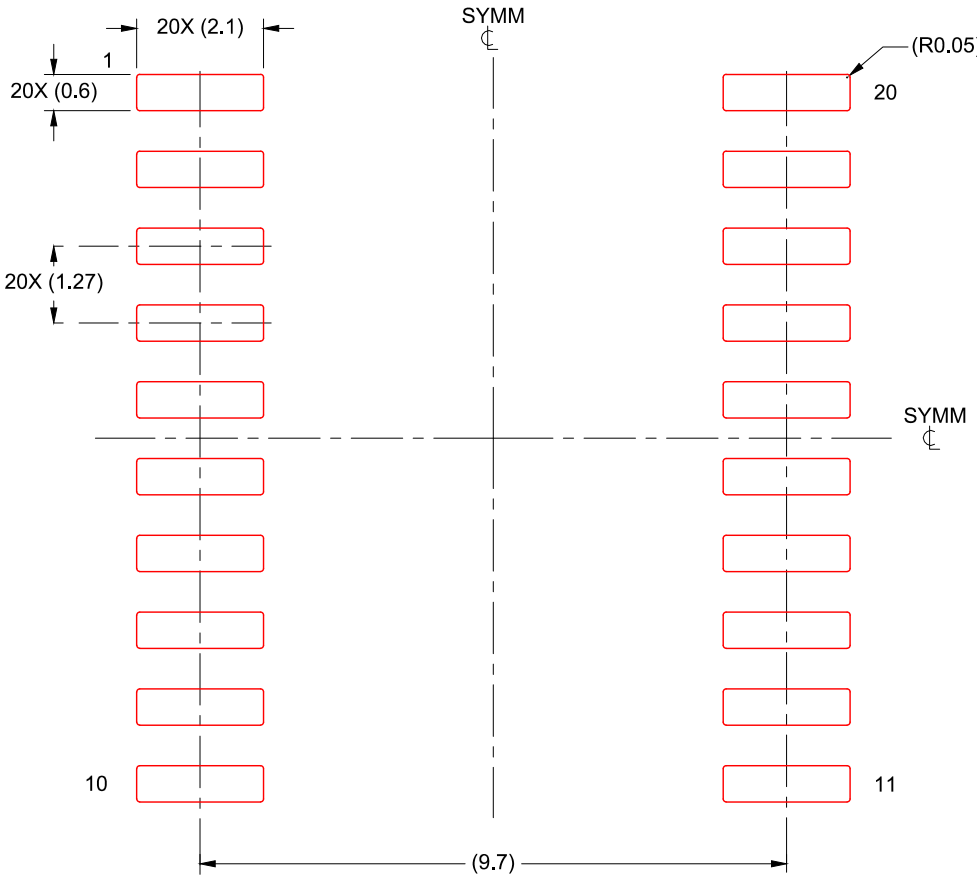

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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