TCAN1167-Q1 Automotive CAN FD System Basis Chip with LDO Output, Sleep Mode, and Watchdog

1 Features

- AEC Q100 (Grade 1) Qualified for automotive applications
- Meets the requirements of ISO 11898-2:2016
- Functional Safety Quality-Managed
  - Documentation available to aid in functional safety system design
- Wide input operational voltage range
- Integrated LDO for CAN transceiver supply
  - 5-V LDO with 100 mA output current capability
- Classic CAN and CAN FD up to 8 Mbps
  - Watchdog timer supporting multiple modes
    - Timeout
    - Window
    - Question and Answer Watchdog (Q&A)
- Operating modes programable via SPI
  - Normal mode
  - Silent mode
  - Standby mode
  - Low-power sleep mode
- High-voltage INH output for system power control
- Local wake-up support via the WAKE pin
- Advanced CAN bus fault detection support
- Defined behavior when unpowered
  - Bus and IO terminals are high impedance (no load to operating bus or application)
- Protection features:
  - ±58-V CAN bus fault tolerant
  - Load dump support on V_{SUP}
  - IEC ESD protection
  - Under-voltage and over-voltage protection
  - Thermal shutdown protection
  - TXD dominant state timeout (TXD DTO)
- Extra wide junction temperature support
- Available in the leadless VSON (14) package with wettable flank for improved automated optical inspection (AOI) capability

2 Applications

- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid, electric and powertrain systems

3 Description

The TCAN1167-Q1 is a high-speed Controller Area Network (CAN) system basis chip (SBC) that meets the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification. The transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps).

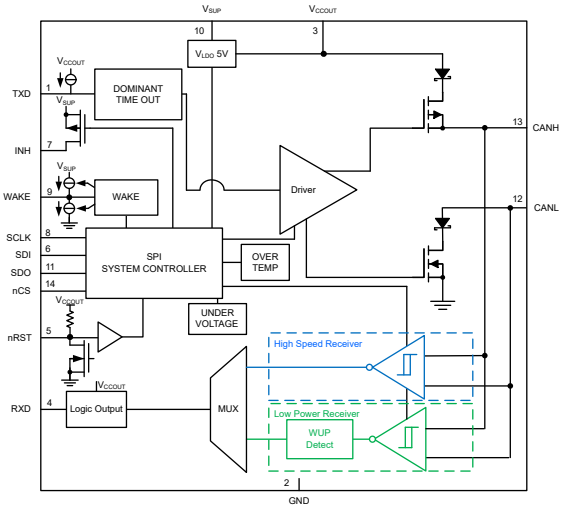
The TCAN1167-Q1 supports a wide input supply range and integrates a 5-V LDO output. The 5-V LDO output (V_{CCOUT}) supplies the CAN transceiver voltage internally as well as additional current externally.

The TCAN1167-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows an ultra-low-current sleep state where power is gated to all system components except for the TCAN1167-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1167-Q1 initiates system start-up by driving INH high.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TCAN1167-Q1	VSON (14)	4.5 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

DATE	REVISION	NOTES
December 2021	*	Initial Revision

5 Description (continued)

The TCAN1167-Q1 supports an ultra low-power standby mode where the high-speed transmitter and normal receiver are switched off and a low-power wake-up receiver enables remote wake-up via the ISO 11898-2:2016 defined wake-up pattern (WUP).

The TCAN1167-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node via the INH output pin. This allows an ultra-low-current sleep state in which power is gated to all system components except for the TCAN1167-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up pattern is detected on the bus or when a local wake-up is requested via the WAKE input, the TCAN1167-Q1 initiates node start-up by driving INH high.

The TCAN1167-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node via the INH output pin. This allows an ultra-low-current sleep state in which power is gated to all system components except for the TCAN1167-Q1, which remains in a low-power state while monitoring the CAN bus. When a wake-up event is detected, the TCAN1167-Q1 initiates node start-up by driving INH high.

The TCAN1167-Q1 supports watchdog funcitonality, ensuring the system is healthy by requiring the processor to reset the watchdog timer within a time window.

6 Pin Configurations and Functions

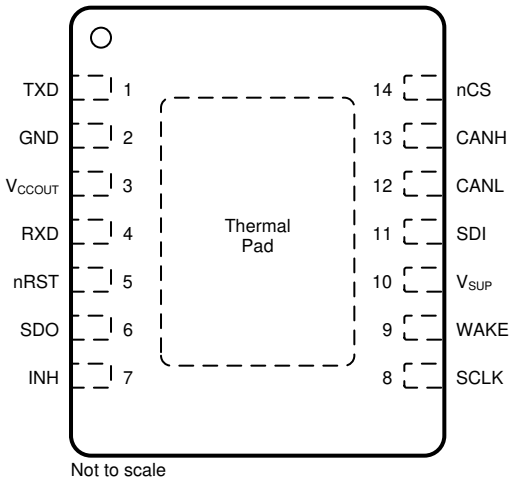


Figure 6-1. DMT Package, 14 Pin (VSON), Top View

Table 6-1. Pin Functions

Pin		TYPE	Description
Name	NO.		
TXD	1	Digital	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CCOUT}	3	Supply	5-V LDO regulated output voltage
RXD	4	Digital	CAN receive data output
nRST	5	Digital	Reset input/output
SDO	6	Digital	SPI data output
INH	7	High Voltage	Inhibit pin to control system voltage regulators and supplies, high voltage
SCLK	8	Digital	SPI clock input
WAKE	9	High Voltage	Reverse-blocked WAKE input terminal
V_{SUP}	10	Supply	Reverse-blocked battery supply input
SDI	11	Digital	SPI data input
CANL	12	Bus IO	Low-level CAN bus input/output line
CANH	13	Bus IO	High-level CAN bus input/output line
nCS	14	Digital	SPI chip select (active low)

7 Specifications

7.1 Absolute Maximum Ratings

over operating virtual junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range	–0.3	42	V
V_{CCOUT}	5 V regulated output	-0.3	6	V
V_{BUS}	CAN bus IO voltage range (CANH, CANL)	–58	58	V
V_{INH}	INH output pin voltage range	–0.3	42 and $V_O \le V_{SUP}$ + 0.3	V
$V_{(Logic\_Input)}$	Logic input terminal voltage range	–0.3	6	V
$V_{(Logic\_Output)}$	Logic output terminal voltage range	–0.3	6	V
$I_{O(LOGIC)}$	Logic output current		8	mA
$I_{O(INH)}$	INH output current		6	mA
$I_{O(WAKE)}$	Wake current if due to ground shifts $V_{(WAKE)} \le V_{(GND)}$ – 0.3 V, thus the current into WAKE must be limited via an external serial resistor		3	mA
T_J	Operating virtual junction temperature range	–40	150	°C
T_{STG}	Storage temperature	-65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pin	±4000	V
			HBM classification level 3A for V_{SUP},	±8000	
			HBM classification level 3B for global pins CANH & CANL	±10000	
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	

(1) AEC-Q100-002 indicates that HBM stresses shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)(1)	CAN bus terminals (CANH & CANL) to GND	IEC 61000-4-2 (150pF, 330Ω) unpowered contact discharge	±8000	V
		V_{SUP}		±8000	
V_{TRAN}	ISO 7637 ISO pulse transients(2)	CAN bus terminals (CANH & CANL) to GND, V_{SUP}	Pulse 1	–100	
			Pulse 2	75	
			Pulse 3a	–150	
			Pulse 3b	100	
	ISO 7637-3 transient(3)		DCC slow transient pulse	±30	

(1) Tested according to IEC 62228-3 CAN Transceiver, Section 6.4; DIN EN 61000-4-2
(2) Tested according to IEC 62228-3 CAN Transceiver, Section 6.3; standard pulse parameters defined in ISO 7637-2
(3) Tested according to ISO 7637-3; electrical transient transmission by capacitive and inductive coupling via lines other than supply line

7.4 Recomended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage range	5.5		28	V
$I_{OH(DO)}$	Digital output terminal high level output current	–2			mA
$I_{OL(DO)}$	Digital output terminal low level output current			2	mA

		MIN	NOM	MAX	UNIT
$I_{O(INH)}$	INH output current			1	mA
C_{VSUP}	V_{SUP} pin capacitance		0.1		µF
C_{VCCOUT}	V_{CCOUT} pin capacitance	10			µF
T_{SDR}	Thermal shutdown rising	175	180		°C
T_{SDF}	Thermal shutdown falling		165	170	°C
T_{SDW}	Thermal shutdown warning	150			°C
T_{HYS}	Thermal shutdown hysterisis		15		°C

7.5 Thermal Information

THERMAL METRIC(1)		DMT (VSON) 14 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	37.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	14.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Power Supply Characteristics

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
I_{SUP}	Supply current Bus biasing active: dominant	TXD = 0 V, R_L = 60 Ω, C_L = open See Figure 8-2			60	mA
		TXD = 0 V, R_L = 50 Ω, C_L = open See Figure 8-2			70	mA
	Supply current Bus biasing active: recessive	TXD = V_{CCOUT}, R_L = 50 Ω, C_L = open See Figure 8-2			3	mA
$I_{SUP(STB)}$	Supply current Standby mode Bus bias autonomous: inactive	5.5 V < V_{SUP} ≤ 19 V See Figure 8-2			230	µA
$I_{SUP(SLP)}$	Supply current Sleep mode Bus bias autonomous: inactive	5.5 V < V_{SUP} ≤ 19 V T_A > 85°C See Figure 8-2			50	µA
$I_{SUP(SLP)}$	Supply current Sleep mode Bus bias autonomous: inactive	5.5 V < V_{SUP} ≤ 19 V T_A ≤ 85°C See Figure 8-2			40	µA
$I_{SUP(BIAS)}$	Supply current Bus bias autonomous: active(1)	5.5 V < V_{SUP} ≤ 28 V See Figure 8-2			60	µA
UV_{SUPR}	Under voltage V_{SUP} threshold rising	Ramp Up	4.05		4.42	V
UV_{SUPF}	Under voltage V_{SUP} threshold falling	Ramp Down	3.9		4.25	V
V_{CCOUT} Characteristics						
V_{CCOUT}	5 V regulated output	V_{SUP} = 5.5 to 18 V I_L = 0 to 100 mA TXD = V_{CCOUT}	4.9	5	5.1	V
V_{CCOUT}	5 V regulated output	V_{SUP} = 5.65 to 18 V I_L = 0 to 100 mA TXD = 0 V; V_{CANH} = 0 V	4.9	5	5.1	V
V_{CCOUT_DROP}	Dropout voltage	5 V LDO, V_{SUP} – V_{CCOUT}, I_L = 125 mA		300	650	mV
$\Delta V_{CCOUT(\Delta VSUP)}$	Line regulation	V_{SUP} = 5.5 to 28 V, I_L = 10 mA, ΔV_{CCOUT}			50	mV
$\Delta V_{CCOUT(\Delta VSUPL)}$	Load regulation	I_L = 1 to 125 mA, V_{SUP} = 14 V, ΔV_{CCOUT}			50	mV

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UV_{VCCOUTR}$	Under voltage V_{CCOUT} threshold rising	Ramp Up	4.25	4.6	4.75	V
$UV_{VCCOUTF}$	Under voltage V_{CCOUT} threshold falling	Ramp Down	4.2	4.45	4.7	V
OV_{CCOUTR}	Over voltage V_{CCOUT} threshold rising	Ramp Up		5.7	6.15	V
OV_{CCOUTF}	Over voltage V_{CCOUT} threshold falling	Ramp Down	5.47	5.65		V
I_{L_VCCOUT}	Output current limit	V_{CCOUT} short to ground	175		275	mA
$PSRR_{VCCOUT}$	Power supply rejection ripple rejection	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, C_O = 10 µF	60			dB

(1) After a valid wake-up the total I_{SUP} current is the sum of $I_{SUP(STB)}$ and $I_{SUP(BIAS)}$ (I_{SUP} = $I_{SUP(STB)}$ + $I_{SUP(BIAS)}$)

7.7 Electrical Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver Electrical Characteristics							
$V_{O(D)}$	Dominant output voltage Bus biasing active	CANH	TXD = 0 V, 50 ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open See Figure 8-2	2.75		4.5	V
	Dominant output voltage Bus biasing active	CANL		0.5		2.25	V
$V_{O(R)}$	Recessive output voltage Bus biasing active		TXD = V_{CCOUT}, R_L = open (no load), R_{CM} = open See Figure 8-2	2		3	V
V_{SYM}	Driver symmetry Bus biasing active ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CCOUT}		R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = Open, R_{CM} = Open, TXD = 250 kHz, 1 Mhz, 2.5 MHz See Figure 8-2	0.9		1.1	V/V
V_{SYM_DC}	DC Driver symmetry Bus biasing active V_{CCOUT} – $V_{O(CANH)}$ – $V_{O(CANL)}$		R_L = 60 Ω, C_L = open See Figure 8-2	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Bus biasing active Dominant	CANH - CANL	TXD = 0 V, 50 Ω ≤ R_L ≤ 65 Ω, C_L = open See Figure 8-2	1.5		3	V
	Differential output voltage Bus biasing active Dominant	CANH - CANL	TXD = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, CL = open See Figure 8-2	1.4		3.3	V
	Differential output voltage Bus biasing active Dominant	CANH - CANL	TXD = 0 V, R_L = 2240 Ω, C_L = open See Figure 8-2	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Bus biasing active Bus biasing inactive Recessive	CANH - CANL	TXD = V_{CCOUT}, R_L = open Ω, C_L = open See Figure 8-2	–50		50	mV
$V_{O(INACT)}$	Pin output voltage Bus biasing inactive	CANH	TXD = V_{CCOUT} R_L = open (no load), C_L = open See Figure 8-2	-0.1		0.1	V
		CANL	TXD = V_{CCOUT} R_L = open (no load), C_L = open See Figure 8-2	-0.1		0.1	V
$V_{OD(STB)}$	Differential output voltage Bus biasing inactive	CANH - CANL	TXD = V_{CCOUT} R_L = open (no load), C_L = open See Figure 8-2	-0.2		0.2	V
$I_{OS(DOM)}$	Short-circuit steady-state output current Bus biasing active Dominant		TXD = 0 V -15 V ≤ $V_{(CANH)}$ ≤ 40 V See Figure 8-2 and Figure 8-8	–75			mA
	Short-circuit steady-state output current Bus biasing active Dominant		TXD = 0 V -15 V ≤ $V_{(CANL)}$ ≤ 40 V See Figure 8-2 and Figure 8-8			75	mA
$I_{OS(REC)}$	Short-circuit steady-state output current Bus biasing active Recessive		V_{BUS} = CANH = CANL -27 V ≤ V_{BUS} ≤ 42 V See Figure 8-2 and Figure 8-8	–3		3	mA
CAN Receiver Electrical Characteristics							

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(DOM)}$	Receiver dominant state input voltage range Bus biasing active	-12 V ≤ V_{CM} ≤ 12 V See Figure 8-3 and Table 9-14	0.9		8	V
$V_{IT(REC)}$	Receiver recessive state input voltage range Bus biasing active		-3		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Bus biasing active	See Figure 8-3 and Table 9-14	80	140		mV
$V_{DIFF(MAX)}$	Maximum rating of V_{DIFF}		-5		10	V
$V_{DIFF(DOM)}$	Receiver dominant state input voltage range Bus biasing inactive	-12 V ≤ V_{CM} ≤ 12 V See Figure 8-3 and Table 9-14	1.150		8	V
$V_{DIFF(REC)}$	Receiver recessive state input voltage range Bus biasing inactive		-3		0.4	V
V_{CM}	Common mode range	See Figure 8-3 and Table 9-14	–12		12	V
$I_{OFF(LKG)}$	Power-off (unpowered) bus input leakage current	V_{SUP} = 0 V, CANH = CANL = 5 V			2.5	µA
C_I	Input capacitance to ground (CANH or CANL) (1)	TXD = V_{CCOUT}			20	pF
C_{ID}	Differential input capacitance(1)	TXD = V_{CCOUT}			10	pF
R_{ID}	Differential input resistance	TXD = V_{CCOUT} -12 V ≤ V_{CM} ≤ 12 V	50		100	kΩ
R_{IN}	Input resistance (CANH or CANL)		25		50	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$ = 5 V	–1		1	%
TXD Input Characteristics						
V_{IH}	High level input voltage		0.7			V_{CCOUT}
V_{IL}	Low level input voltage				0.3	V_{CCOUT}
I_{IH}	High level input leakage current	TXD = V_{CCOUT}	–1	0	1	µA
I_{IL}	Low level input leakage current	TXD = 0 V	–130		–15	µA
R_{PU}	Pull-up resistance		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{SUP} = 0 V	–1	0	1	µA
C_I	Input Capacitance	V_{IN} = 0.4 x sin(2 × π × 2 × 10^6 × t) + 2.5 V		5		pF
RXD Output Characteristics						
V_{OH}	High level output voltage	I_O = –2 mA.	0.8			V_{CCOUT}
V_{OL}	Low level output voltage	I_O = 2 mA.			0.2	V_{CCOUT}
R_{PU}	Pull-up resistance		40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage curret	RXD = 5.5 V, V_{SUP} = 0 V	-5		5	µA
INH Output Characteristics						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = –6 mA		0.5	1	V
$I_{LKG(INH)}$	Sleep mode leakage current	INH = 0 V	–0.5		0.5	µA
R_{PD}	Pull-down resistance	Sleep Mode	2.5	4	6	MΩ
WAKE Input Characteristics						
V_{IH}	High-level input voltage	Sleep mode	4			V
V_{IL}	Low-level input voltage				2	V
I_{IL}	Low level input leakage current	WAKE = 1 V			3	µA
V_{HYS}	Input hysteresis		800		1200	mV
nRST Bidirectional Characteristics						
V_{IH}	High level input voltage		0.8			V_{CCOUT}
V_{IL}	Low level input voltage				0.2	V_{CCOUT}
V_{OL}	Low level output voltage	I_O = 2 mA.			0.2	V_{CCOUT}
I_{IH}	High level input leakage current	nRST = V_{CCOUT}	-1		1	µA
R_{PU}	Pull-up resistance to V_{CCOUT}		160	240	320	kΩ
SDI Input Characteristics						
V_{IH}	High level input voltage		0.8			V_{CCOUT}

Over recommended operating conditions with T_J = –40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V, and R_L = 60 Ω

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low level input voltage					0.2	V_{CCOUT}
I_{IH}	High level input leakage current		SDI = V_{CCOUT} (2)	-1		1	µA
I_{IL}	Low level input leakage current		SDI = 0 V	-130		-50	µA
R_{PU}	Pull-up resistance			40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current		SDI = 5.5 V, V_{SUP} = 0 V	-1		1	µA
C_{IN}	Input capacitance		20 MHz	4		10	pF
SCLK Input Characteristics							
V_{IH}	High level input voltage			0.7			V_{CCOUT}
V_{IL}	Low level input voltage					0.3	V_{CCOUT}
I_{IH}	High level input leakage current		SCLK = V_{CCOUT} (2)	50		130	µA
I_{IL}	Low level input leakage current		SCLK = 0 V	-1		1	µA
R_{PD}	Pull-down resistance			40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current		SCLK = 5.5 V, V_{SUP} = 0 V	-1		1	µA
C_{IN}	Input capacitance		20 MHz	4		10	pF
nCS Input Characteristics							
V_{IH}	High level input voltage	High level input voltage	High level input voltage	0.7			V_{CCOUT}
V_{IL}	Low level input voltage	Low level input voltage	Low level input voltage			0.3	V_{CCOUT}
I_{IH}	High level input leakage current		nCS = V_{CCOUT}	-1		1	µA
I_{IL}	Low level input leakage current		nCS = 0 V	-130		-50	µA
R_{PU}	Pull-up resistor			40	60	80	kΩ
$I_{LKG(OFF)}$	Unpowered leakage current		nCS = 5.5 V, V_{SUP} = 0 V	-1		1	µA
C_{IN}	Input capacitance		20 MHz	4		10	pF
SDO Output Characteristics							
V_{OH}	High-level output voltage		I_{OH} = -2 mA	0.8			V_{CCOUT}
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.2	V_{CCOUT}
$I_{LKG(OFF)}$	Unpowered leakage current		V_{nCS} = 5.5 V	-1		1	µA

(1) Test according to ISO 11898-2:2003
(2) Note that there is an internal pull-up resistor to V_{CCOUT}. If externally driven to a higher or lower voltage, the pin leakage measurement will be increased.

7.8 Switching Characteristics

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Switching Characteristics						
t_{POWER_UP}	CAN supply power up time	C_{VCCOUT} = 10 µF See Figure 8-9		1.8	4	ms
$t_{UV(SUP)}$	V_{SUP} filter time (rising and falling)		4		25	µs
$t_{UV(VCCOUT)}$	V_{CCOUT} filter time (rising and falling)	Time for device to enter sleep state reset state once UV_{CCOUT} is reached		30		µs
Device Switching Characteristics						
$t_{UV(nRST)}$	Undervoltage detection delay time nRST low			10	50	µs
t_{WK_FILTER}	Bus time to meet filtered bus requirments for wakeup request	See Figure 9-15	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wakeup timeout value		0.8		2	ms
$t_{SILENCE}$	Time out for bus inactivity			0.9	1.2	s
$t_{INACTIVE}$	Hardware timer for failsafe and power up inactivity(1)		3	4	5	min
t_{BIAS}	Time from the start of a dominant-recessive-dominant sequence until Vsym ≥ 0.1	Each phase: 6 µs See Figure 8-11			250	µs

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V and R_L = 60 Ω

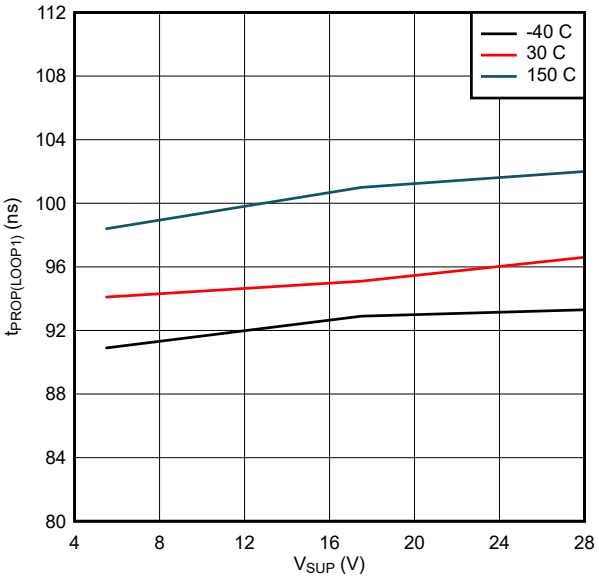
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CAN(ACTIVE)}$	Time from switching to CAN active mode to transceiver ready to transmit	V_{CCOUT} > $UV_{VCCOUT(R)}$			25	us
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Recessive to dominant	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF See Figure 8-6		100	160	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD) Dominant to recessive	R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF See Figure 8-6		120	175	ns
$t_{mode\_slp\_reset}$	WUP or LWU event to INH asserted high, see				50	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive	R_L = 60 Ω, C_L = 100 pF, R_{CM} = open See Figure 8-2	20	35	70	ns
t_{pLD}	Propagation delay time, low TXD to driver dominant		15	40	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			10	20	ns
t_R	Differential output signal rise time			40		ns
t_F	Differential output signal fall time			45		ns
t_{TXD_DTO}	Dominant timeout	R_L = 60 Ω, C_L = open See Figure 8-7, TXD = 0 V	1.2		3.8	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high RXD	$C_{L(RXD)}$ = 15 pF See Figure 8-3	25	80	140	ns
t_{pDL}	Propagation delay time, bus dominant input to RXD low output	$C_{L(RXD)}$ = 15 pF See Figure 8-3	20	50	110	ns
t_R	Output signal rise time (RXD)	$C_{L(RXD)}$ = 15 pF See Figure 8-3		8		ns
t_F	Output signal fall time (RXD)	$C_{L(RXD)}$ = 15 pF See Figure 8-3		5		ns
WAKE Characteristics						
t_{WAKE}	Time required for INH pin to go high after an local wake event occurs on the WAKE pin		40			µs
nRST Characteristics						
t_{nRST}	Minimum low time for reset	Input pulse width	15			µs
$t_{nRST(cold)}$	Output pulse width	Cold crank	20		27	ms
$t_{nRST(warm)}$	Output pulse width	Warm crank	1		1.5	ms
SPI Switching Characteristics						
f_{SCK}	SCK, SPI clock frequency	Normal, standby, and silent modes			4	MHz
t_{SCK}	SCK, SPI clock period	Normal, standby, and silent modes; See Figure 8-13	250			ns
t_{RSCK}	SCK rise time	See Figure 8-12			40	ns
t_{FSCK}	SCK fall time	See Figure 8-12			40	ns
t_{SCKH}	SCK, SPI clock high	Normal, standby, and silent modes; See Figure 8-13	125			ns
t_{SCKL}	SCK, SPI clock low	Normal, standby, and silent modes; See Figure 8-13	125			ns
t_{ACC}	First read access time from chip select		50			ns
t_{CSS}	Chip select setup time	See Figure 8-12	100			ns
t_{CSH}	Chip select hold time	See Figure 8-12	100			ns
t_{CSD}	Chip select disable time	See Figure 8-12	50			ns
t_{SISU}	Data in setup time	Normal, standby, and silent modes; See Figure 8-12	50			ns
t_{SIH}	Data in hold time	Normal, standby, and silent modes; See Figure 8-12	50			ns
t_{SOV}	Data out valid	Normal, standby, and silent modes; See Figure 8-13			80	ns
t_{RSO}	SO rise time	See Figure 8-13			40	ns

Over recomended operating conditions with T_J = -40°C to 150°C, unless otherwise noted. All typical values are taken at 25°C, V_{SUP} = 12 V and R_L = 60 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FSO}	SO fall time	See Figure 8-13			40	ns
CAN FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 8-6	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		155		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns		80		140	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 8-6	400		550	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		120		220	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns		80		135	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	R_L = 60 Ω, C_L = 100 pF $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$ See Figure 8-6	-50		20	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-45		15	ns
	Receiver timing symetry with $t_{BIT(TXD)}$ = 125 ns		-40		10	ns

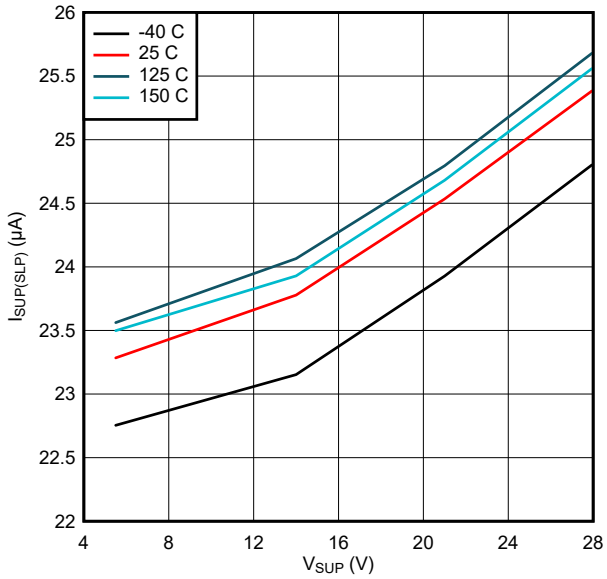
(1) Timer is reset when the CAN bus changes states.

7.9 Typical Characteristics



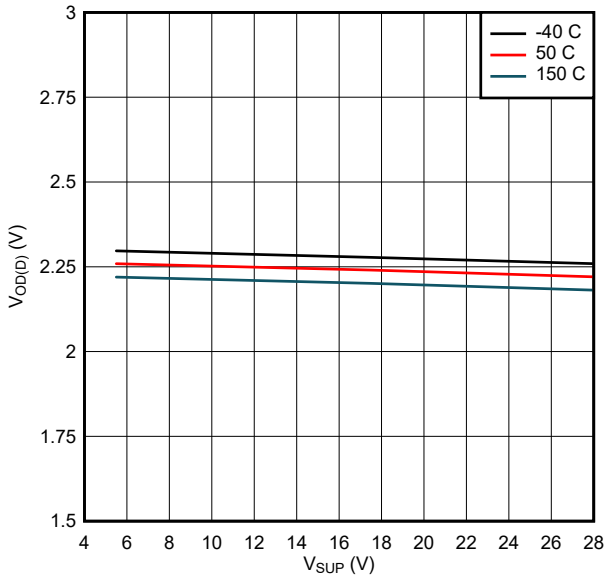
R_L = 60 Ω C_L = 100 pF C_{LRXD} = 15 pF

Figure 7-1. $t_{PROP(LOOP1)}$ over V_{SUP}



R_L = 60 Ω

Figure 7-2. I_{SUP} over V_{SUP} Sleep Mode



R_L = 60 Ω

Figure 7-3. $V_{OD(DOM)}$ over V_{SUP}

8 Parameter Measurement Information

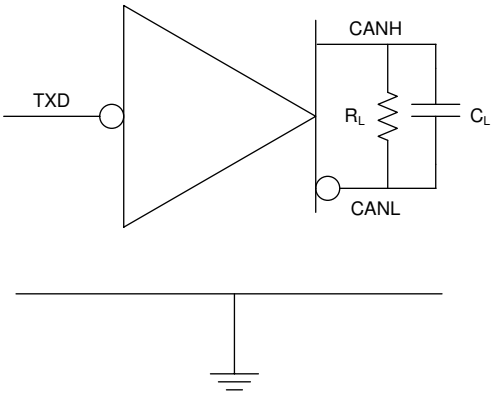


Figure 8-1. I_{SUP} Test Circuit

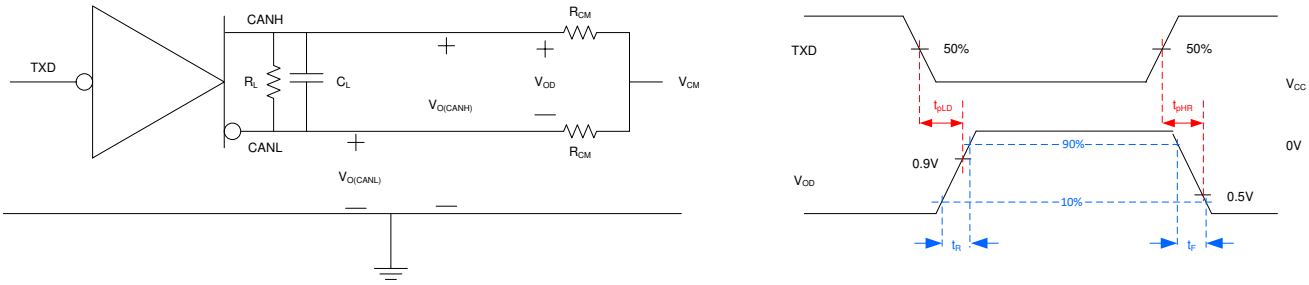


Figure 8-2. Driver Test Circuit and Measurement

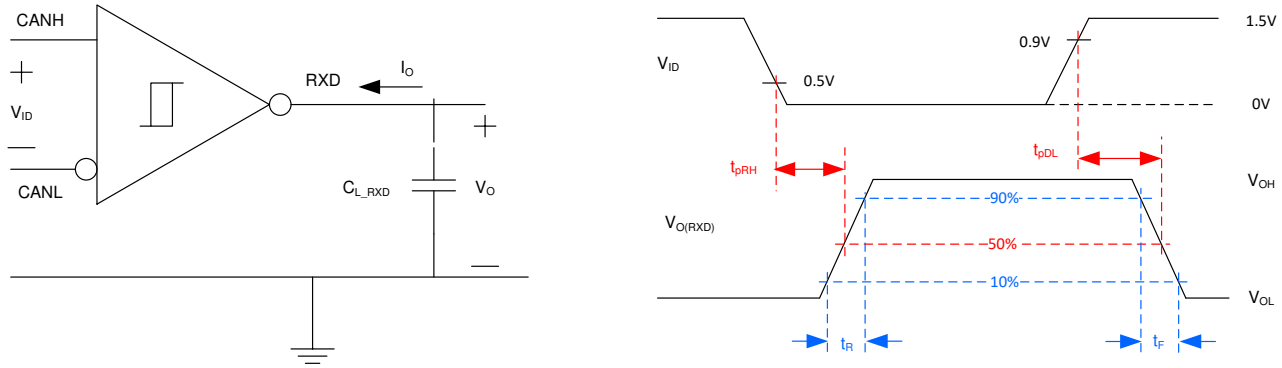


Figure 8-3. Receiver Test Circuit and Measurement

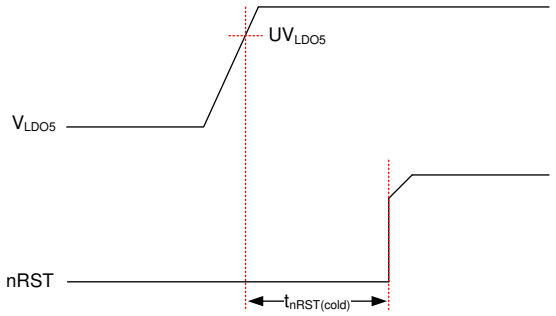


Figure 8-4. t_{nRST} Cold Start

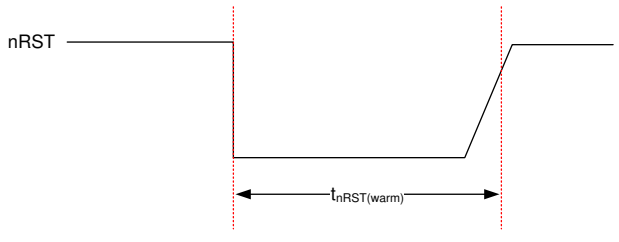


Figure 8-5. t_{nRST} Warm Start

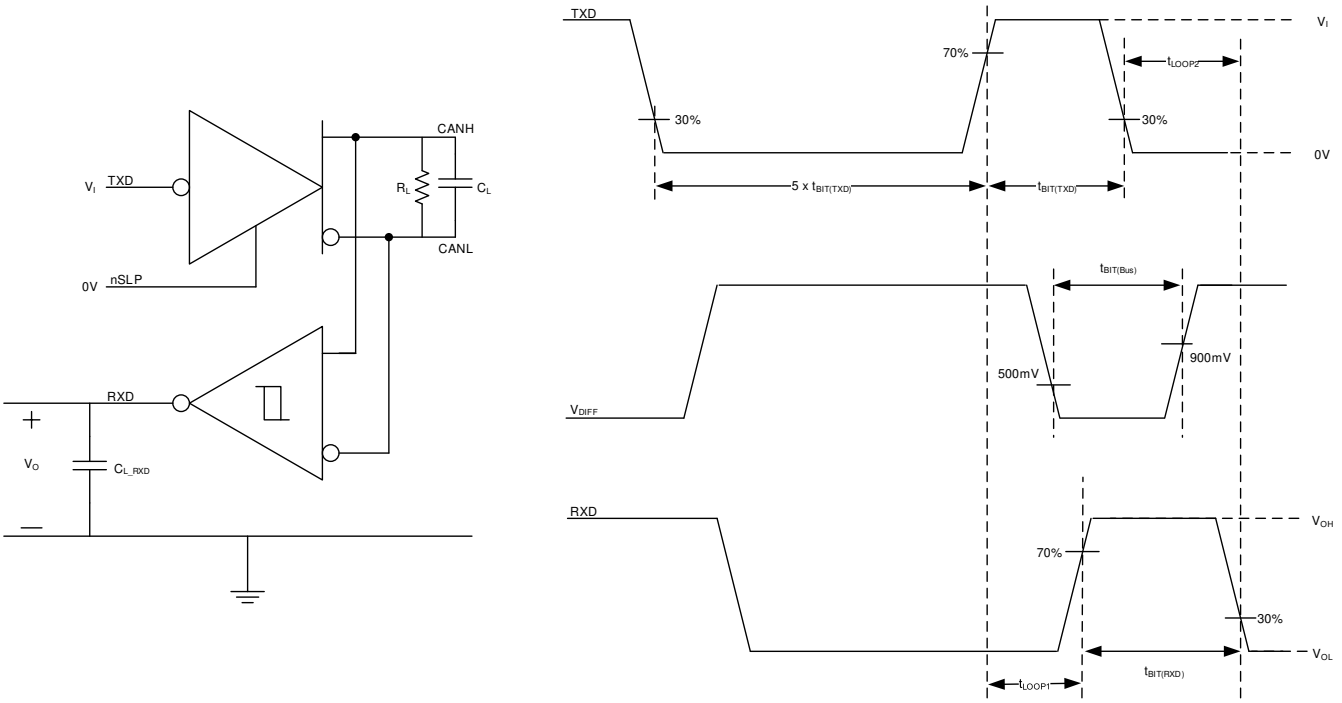


Figure 8-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

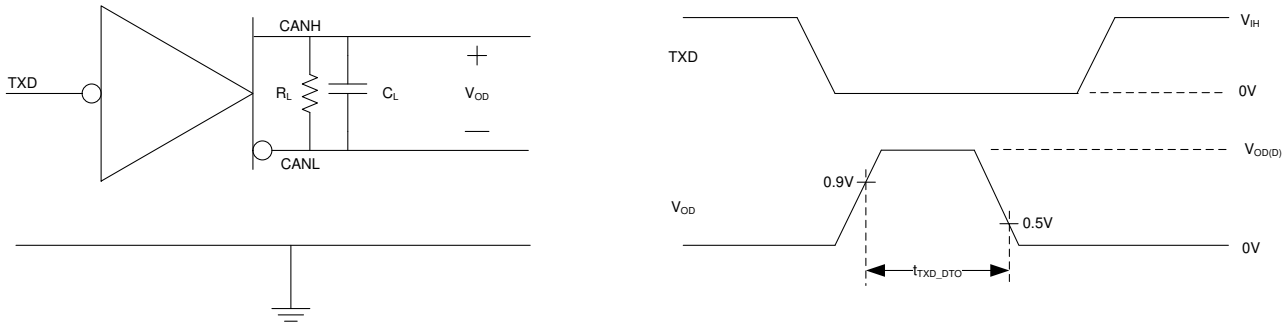


Figure 8-7. TXD Dominant Timeout Test Circuit and Measurement

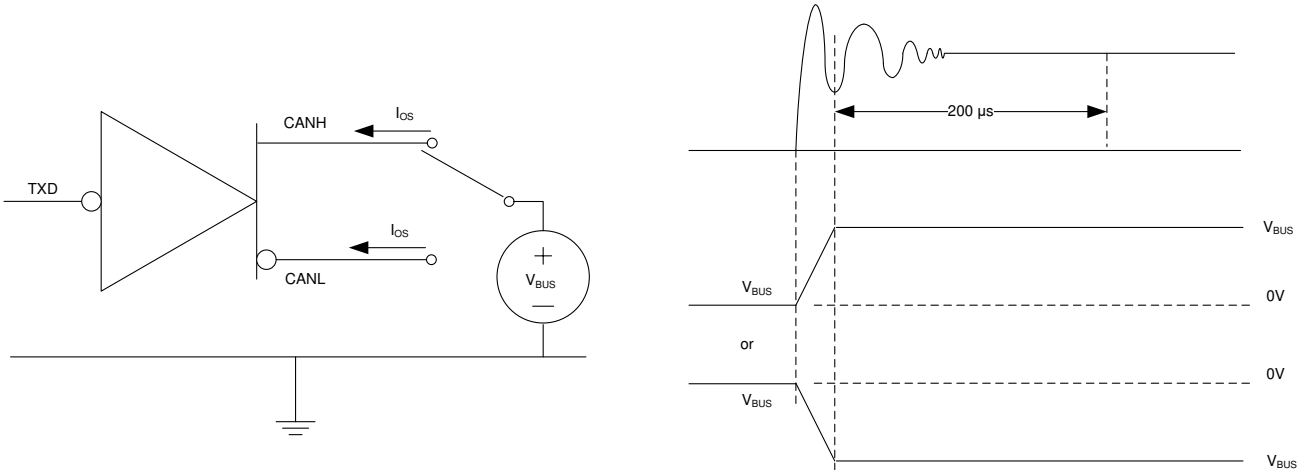


Figure 8-8. Driver Short-Circuit Current Test and Measurement

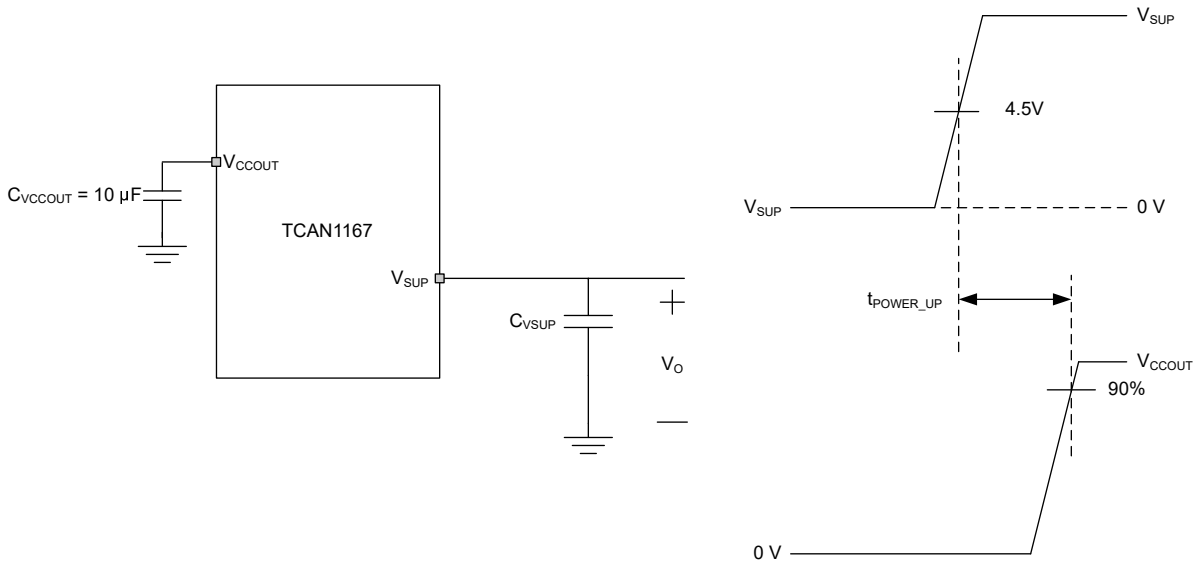


Figure 8-9. t_{POWER_UP} Timing Measurement

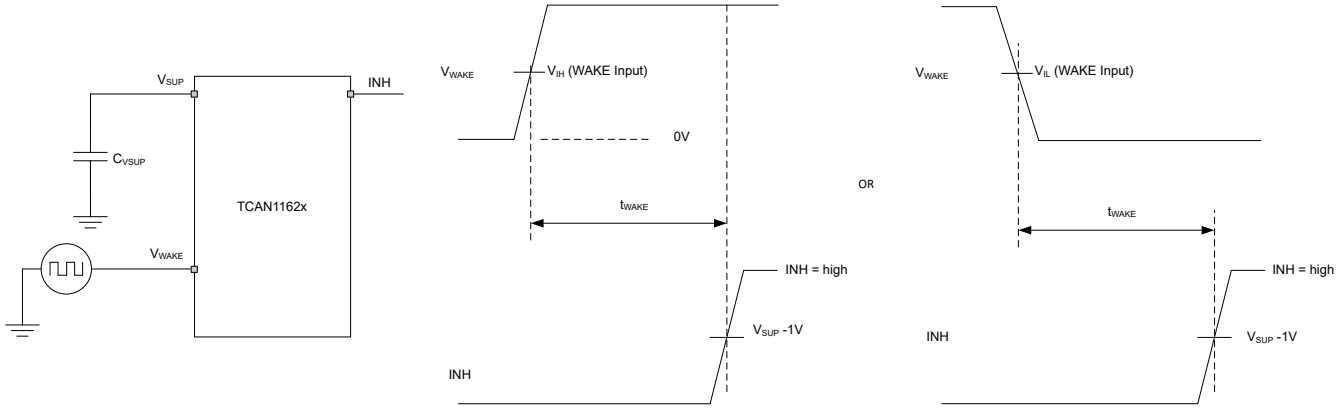


Figure 8-10. t_{WAKE} While Monitoring INH Output

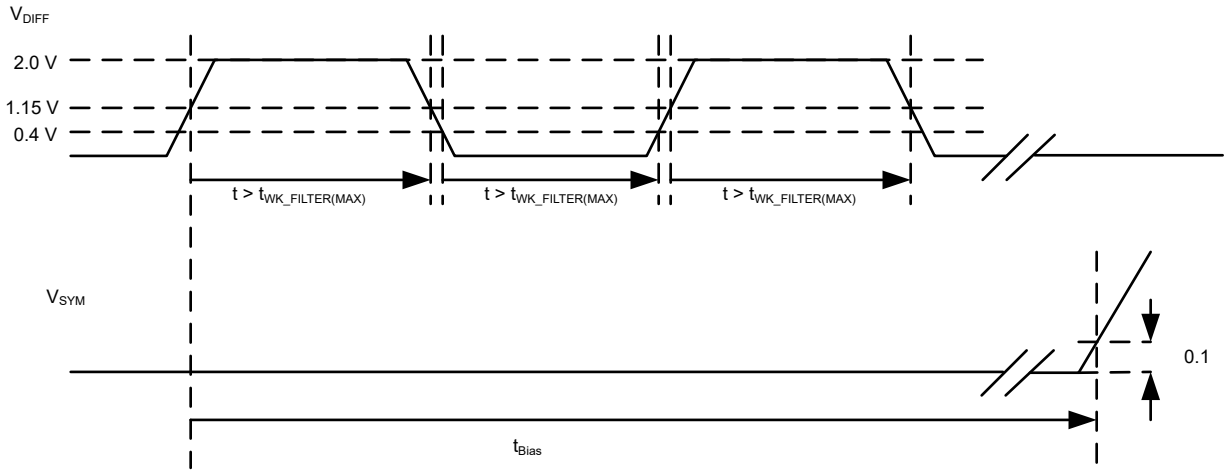


Figure 8-11. Test Signal Definition for Bias Reaction Time Measurement

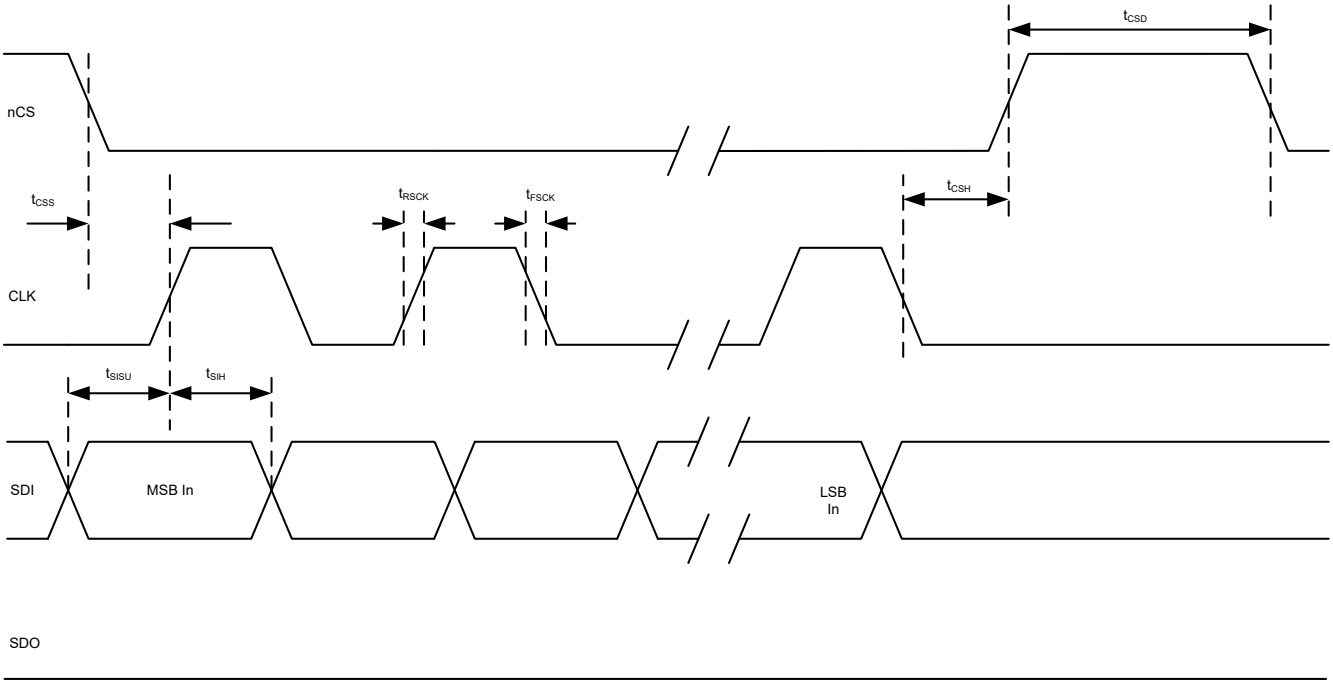


Figure 8-12. SPI AC Characteristic Write

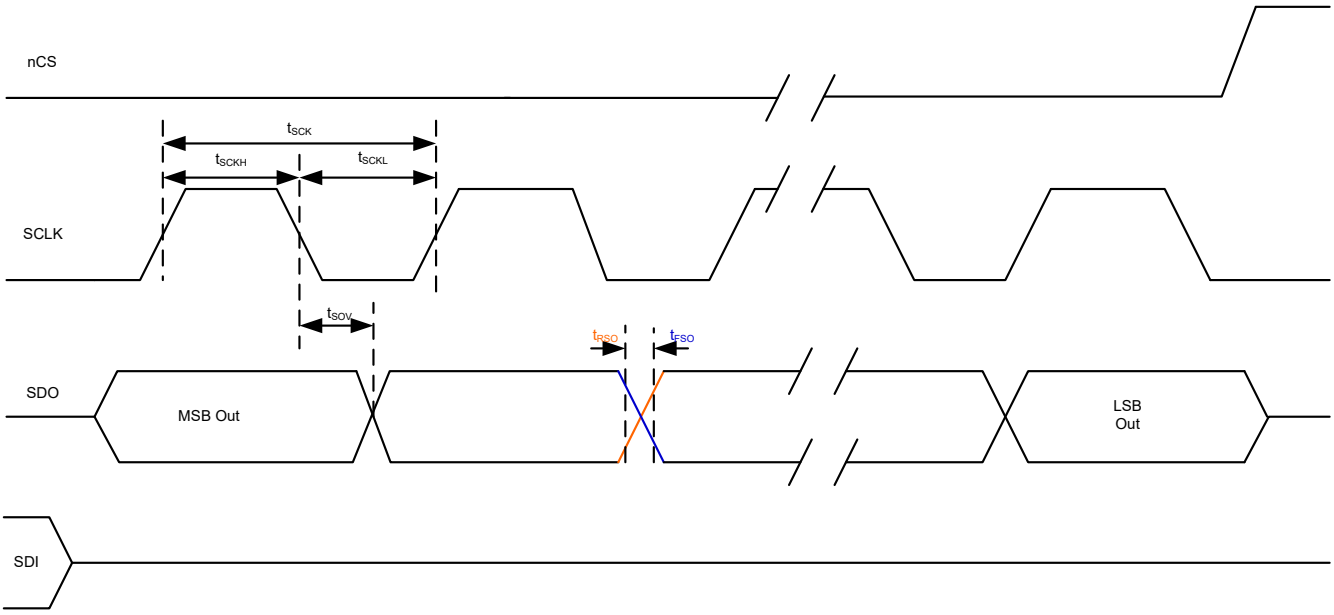


Figure 8-13. SPI AC Characteristic Read

9 Detailed Description

9.1 Overview

The TCAN1167-Q1 is a high speed Controller Area Network (CAN) system basis chip (SBC) that meets the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification. The transceiver supports both classical CAN and CAN FD networks up to 8 megabits per second (Mbps).

The TCAN1167-Q1 supports a wide input supply range and integrates a 5-V LDO output. The 5-V LDO output (V_{CCOUT}) supplies the CAN transceiver voltage internally as well as additional current externally.

The TCAN1167-Q1 allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a system via the INH output pin. This allows an ultra-low-current sleep state where power is gated to all system components except for the TCAN1167-Q1, while monitoring the CAN bus. When a wake-up event is detected, the TCAN1167-Q1 initiates system start-up by driving INH high.

9.2 Functional Block Diagram

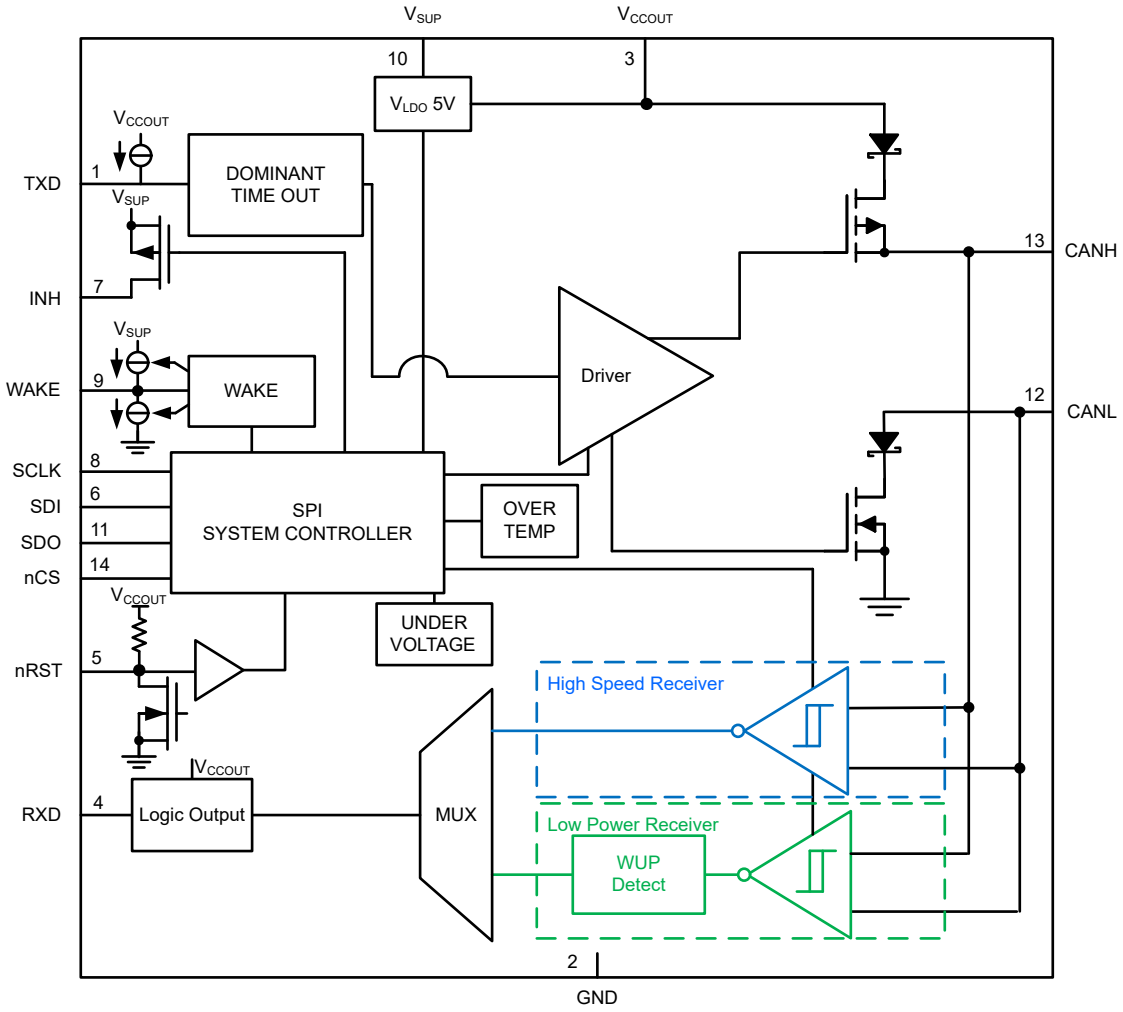


Figure 9-1. TCAN1167-Q1

9.3 Feature Description

9.3.1 V_{SUP} Pin

This pin is connected to the battery supply. It provides the supply to the internal regulators that support the digital core, the CAN transceiver, and the low power CAN receiver.

9.3.2 V_{CCOUT} Pin

An internal LDO provides power for the integrated CAN transceiver and the V_{CCOUT} output pin. The amount of current that can be delivered externally is dependent upon the CAN transceiver requirements during normal operation as well as the ambient operating temperature. When a CAN bus fault takes place that requires additional current from the LDO, the total available current to external load components may be degraded. During sleep mode the LDO is disabled and no current can be delivered. Once the device leaves sleep mode and enters other active modes the LDO is enabled for normal operation. This pin requires a 10 µF external capacitor as close to the pin as possible.

9.3.3 Digital Inputs and Outputs

The TCAN1167-Q1 has a V_{CCOUT} supply that is used to set the digital input thresholds. The input thresholds are ratio metric to the V_{CCOUT} supply using CMOS input levels. The TXD input is biased to the V_{CCOUT} level to force a recessive input in case the pin floats. The high level output voltage for the RXD and output pins is driven to the V_{CCOUT} level as logic-high outputs.

9.3.3.1 TXD Pin

TXD is a digital signal, referenced to V_{CCOUT}, from a CAN controller to the TCAN1167-Q1.

9.3.3.2 RXD Pin

RXD is a digital signal, referenced to V_{CCOUT}, from the TCAN1167-Q1 to a CAN controller.

When a wake event occurs, this pin is pulled low to signal that a wake event has taken place.

9.3.4 GND

GND is the ground pin and it must be connected to the PCB ground.

9.3.5 INH Pin

The TCAN1167-Q1 inhibit (INH) output pin can be used to control the enable of system power management devices allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INH pin has two states: driven high and high impedance. When the INH pin is driven high the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state the output will be left floating. The INH pin is high in the normal and standby modes and is low when in sleep mode. A 100 kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

This terminal should be considered a high-voltage logic terminal, not a power output thus should be used to drive the EN terminal of the system's power management device and not used as a switch for the power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside the system module.

9.3.6 WAKE Pin

The WAKE pin is a high-voltage reverse-blocked input used for the local wake-up (LWU) function. This function is explained further in Local Wake-Up (LWU) via WAKE Input Terminal section. The pin is defaulted to bi-directional edge trigger, meaning a local wake-up (LWU) is recognize on either a rising or falling edge of WAKE pin transition.

9.3.7 nRST Pin

The nRST is an bidirectional open drain low side driver with an integrated pull-up resistor to V_{CCOUT}. It can be pulled low by the device when placed in fail-safe mode.

During initial power-up of the device, a sleep mode to reset transition, a fail-safe mode to reset transition, or an undervoltage event will be recognized as a cold crank reset condition. The nRST pin will be held low for $t_{nRST(cold)}$ allowing the MCU and peripheral devices to power-up correctly before data transmission begins.

To enter reset mode from normal mode, or standby mode the nRST must be pulled low for a minimum of time of t_{nRST}. The TCAN1167-Q1 recognizes this and a watchdog error as a warm crank reset condition and holds the nRST pin low for $t_{nRST(warm)}$.

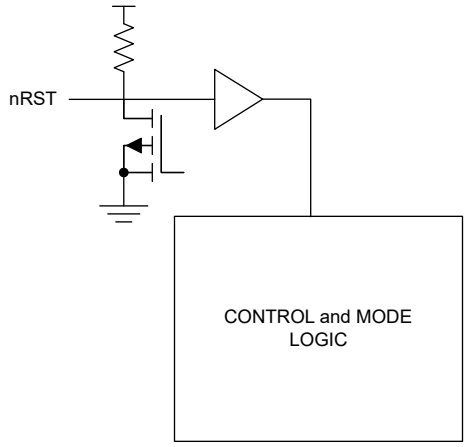


Figure 9-2. nRST Circuit

9.3.8 SDO

When nCS is low this pin is the SPI serial data output pin. When nCS is high, the pin will be tri-stated.

9.3.9 nCS Pin

The nCS pin is the SPI chip select pin. When pulled low and a clock is present the device can be written to or read from.

9.3.10 SCLK

The SCLK pin is the SPI clock. The clock rate should not exceed the max f_{SCK} value.

9.3.11 SDI

When nCS is low this pin is the SPI serial data input pin used for programming the device or requesting data.

9.3.12 CAN Bus Pins

These are the CAN high and CAN low, CANH and CANL, differential bus pins. These pins are connected to the CAN transceiver and the low-voltage wake receiver.

9.3.13 Local Faults

9.3.13.1 TXD Dominant Timeout (TXD DTO)

While the CAN driver is in active mode a TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time out constant of the circuit, t_{TXD_DTO}, expires the CAN driver is disabled releasing the bus lines to the recessive level. This keeps the bus free for communication between other nodes on the network. The CAN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant time out. The high-speed receiver and RXD terminal will reflect what is on the CAN bus during a TXD DTO fault. The TS terminal in driven low during a TXD DTO fault.

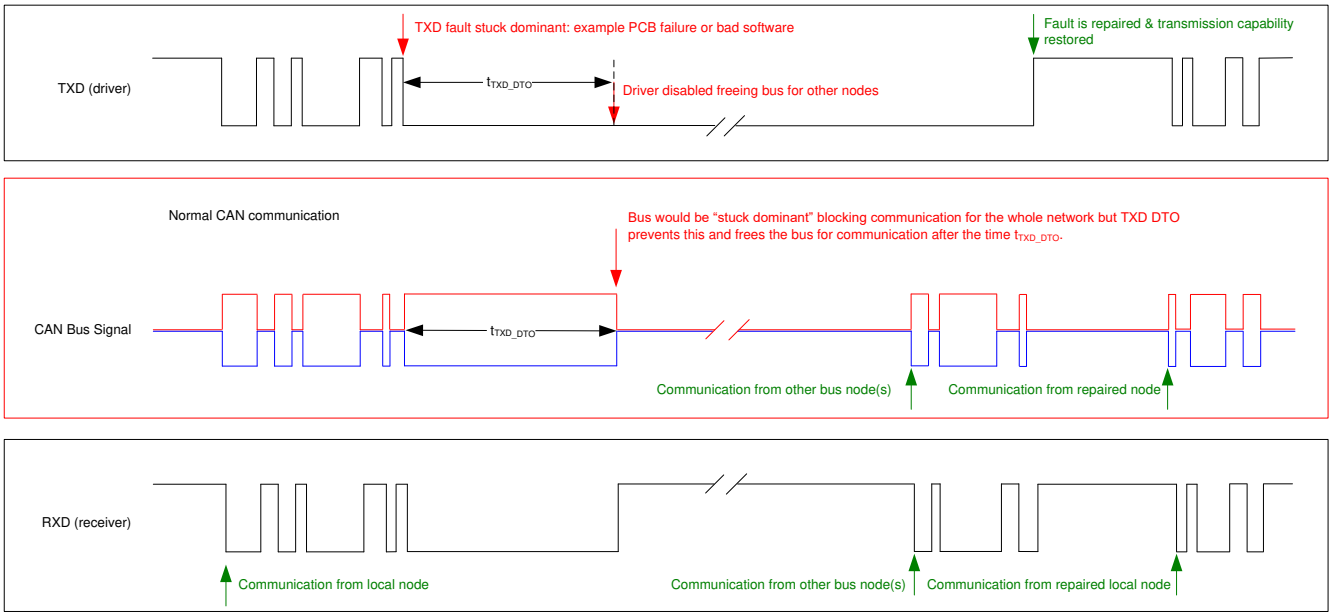


Figure 9-3. Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using the minimum t_{TXD_DTO} time and the maximum number of successive dominant bits (11 bits).

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

9.3.13.2 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1167-Q1 exceeds the thermal shutdown threshold, $T_J > T_{SDR}$, the device transitions into fail-safe mode and disables the transceiver's transmitter and receiver blocking transmission to and from the CAN bus. The TSD fault condition is cleared when the device junction temperature falls below the thermal shutdown temperature threshold, $T_J < T_{SDF}$. If the fault condition that caused the TSD fault is still present, the temperature may rise again and the device will enter thermal shutdown again. Prolonged operation with a TSD fault conditions may affect device reliability.

9.3.13.3 Under/Over Voltage Lockout

The supply terminals implement undervoltage and over voltage detection circuitry. If an undervoltage is detected the TCAN1167-Q1 transitions into reset mode. The SBC will remain in reset mode until the undervoltage event clears.

If the over voltage fault is detected the TCAN1167-Q1 transitions into fail-safe mode. These mode changes place the device in a known state which protect the system from unintended behavior. See Table 9-1

Table 9-1. Undervoltage / Over Voltage Lockout

Fault	Mode
UV_{CCOUT}	Reset
OV_{CCOUT}	Fail-safe

9.3.13.4 Unpowered Devices

The device is designed to be an ideal passive or no load to the CAN bus if it is unpowered. The CANH and CANL pins have low leakage currents when the device is un-powered so they present no load to the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

The logic terminals also have low leakage currents when the device is un-powered so they do not load down other circuits which may remain powered.

9.3.13.5 Floating Terminals

The TCAN1167-Q1 has internal pull-ups and pull-downs on critical pins to ensure a known operating behavior if the pins are left floating.

The TXD pin is pulled up to V_{CCOUT} which forces a recessive level if the pin floats. This internal bias should not be relied upon by design but rather a fall-safe option. Special care needs to be taken when the devive is used with a CAN controller that has open drain outputs. The device implements a weak internal pull-up resistor on the TXD pin. The CAN bit timing for CAN FD data rates will require special consideration and the pull-up strength should be considered carfully when using open drain outputs. An adequate external pull-up resistor must be used to ensure that the TXD output of the CAN controller maintains adequate bit timing input to the CAN device.

Table 9-2. Terminal Fail-Safe Biasing

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
nCS	Pull-up	Weakly biases nCS high to prevent un-intended SPI communication
SCLK	Pull-down	Weakly biased to ground
INH	Pull-down	Weakly biased to ground

9.3.13.6 CAN Bus Short Circuit Current Limiting

The TCAN1167-Q1 has several protection features that limit the short circuit current during dominant and recessive when a CAN bus line is shorted. The device has TXD dominant state timeout which prevents permanently having a higher short circuit current during a dominant state fault.

During CAN communication the bus switches between the dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. The average short circuit current should be used when considering system power for the termination resistors and common mode choke. The percentage dominant is limited by the TXD dominant state timeout and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure that there is a minimum recessive time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance and other network components.

9.3.13.7 Sleep Wake Error Timer

The sleep wake error (SWE) timer, $t_{INACTIVE}$, is a timer used to determine if specific external and internal functions are working. The SWE timer starts when the device enters standby mode and only runs in standby mode. A mode transistion stops the timer. If the timer times out while the device is in standby mode the WKERR

interrupt bit in the INT_1 register will be set, register 8'h51[4], and the RXD pin will be pulled low to indicate an interrupt. The TCAN1167-Q1 will then transition to sleep mode.

9.3.14 Watchdog

The TCAN1167-Q1 has an integrated watchdog function. The TCAN1167-Q1 provides a window based watchdog as well as selectable autonomous, time-out or question and answer (Q&A) watchdog using SPI programming. This function is default disabled. When enabled, the watchdog timer treats a mode transition as the first watchdog trigger event.

All four versions of the watchdog, autonomous, time-out, window and Q&A are avilable in normal and silent modes. When in standby mode the device will automactically transistion to a time-out watchdog. If autonomous has been selected the transistion to standby will keep the autonomous configuration. The watchdog timer is off in sleep mode.

9.3.14.1 Watchdog Error Counter

The TCAN1167-Q1 has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is set to trigger a watchdog error event. This counter can be changed to the fifth or ninth error. The error counter can be read at register 8'h13[3:2].

9.3.14.2 Watchdog SPI Control Programming

The watchdog is configured and controlled using registers 8’h13 through 8’h15. These registers are provided in table Table 9-3. The TCAN1167-Q1 watchdog can be set as autonomous, time-out, window or question and answer (Q&A) watchdog by setting 8’h13[7:6] to the method of choice. The time-out and window watchdog timer is based upon registers 8’h13[5:4] WD prescaler and 8’h14[7:5] WD timer and is in ms. See Table 9-3 for the achievable times. If using smaller time windows it is suggested to use the time-out version of the watchdog. This is for times between 4 ms and 64 ms.

Table 9-3. Watchdog Window and Time-out Timer Configuration (ms)

WD_TIMER (ms)	8'h13[5:4] WD_PRE			
8'h14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

Note

If timing parameters are changed while the watchdog is running, the WD stops until after the first input trigger event after the new parameters have been programmed at which time it runs based upon the new timing parameters.

9.3.14.3 Watchdog Timing

The device provides four methods for setting up the watchdog. If more frequent, < 64 ms, input trigger events are desired it is suggested to use the Time-out timer as this is an event within the time event and not specific to an open window.

Autonomous watchdog is a type of time-out watchdog. The difference from time-out is when it is enabled. In Standby (RXD=High, so no wake event) or Sleep mode, a wake event impacts the autonomous behavior. The wake event in standby mode is treated as a watchdog trigger event. Clearing the wake event in Standby will

both disable the Watchdog and set RXD=H. If another wake event takes place while the device is still in standby mode, it will be treated as a WD trigger event. While in sleep mode the WD is off but a wake event will transistion the device to standby mode and is treated as a WD trigger event. Regular time-out watchdog (or any other watchdog) requires a mode transistion to start the timer. Only Autonomous can do a trigger based on a Wake event. In Normal mode, Autonomous works like a time-out (always enabled).

When using the window watchdog it is important to understand the closed and open window aspects. The device is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be taken into account. Using the 60 ms nominal total window provides a closed and open window that are each 30 ms. Taking the ± 10% internal oscillator into account means the total window could be 54 ms, t_{WINDOW}, MIN or 66 ms, t_{WINDOW} MAX. The closed and open window would then be 27 ms, T_{WDOUT} MIN, or 33 ms, T_{WDOUT} MIN. From the 54 ms total window and 33 ms closed window the total open window is 21 ms. The trigger event needs to happen at the 43.5 ms ± 10.5 ms, safe trigger area. The same method is used for the other window values. Figure 9-4 provides the above information graphically. Once the WD trigger is written, the current Window is terminated and a new Closed Window is started.

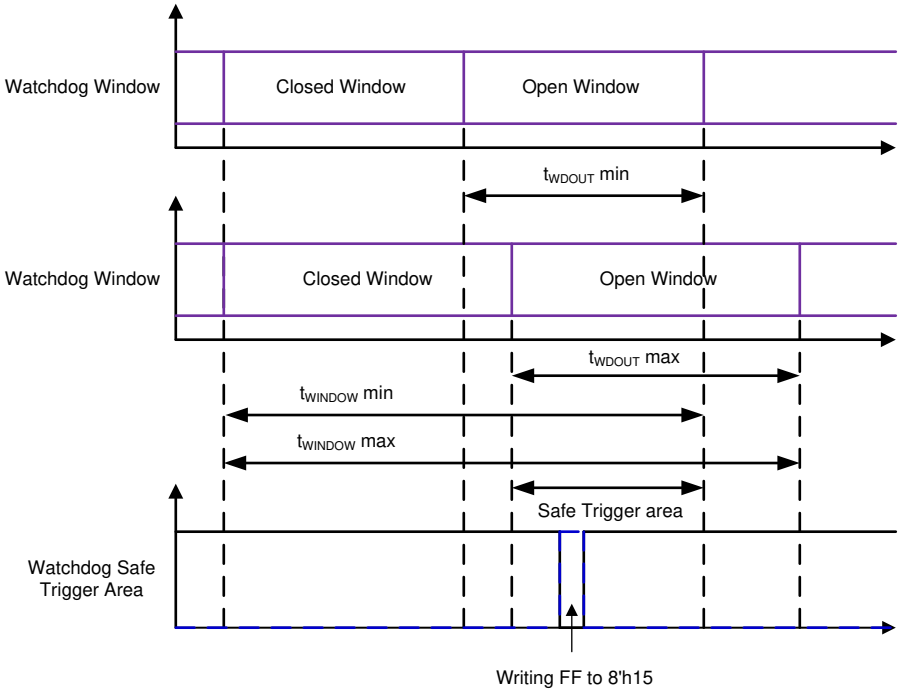


Figure 9-4. Window Watchdog Timing Diagram

9.3.14.4 Question and Answer Watchdog

The TCAN1167-Q1 has a watchdog timer that supports the window watchdog as well as the Q&A watchdog.

Section 9.3.14.5 explains the WD initialization events.

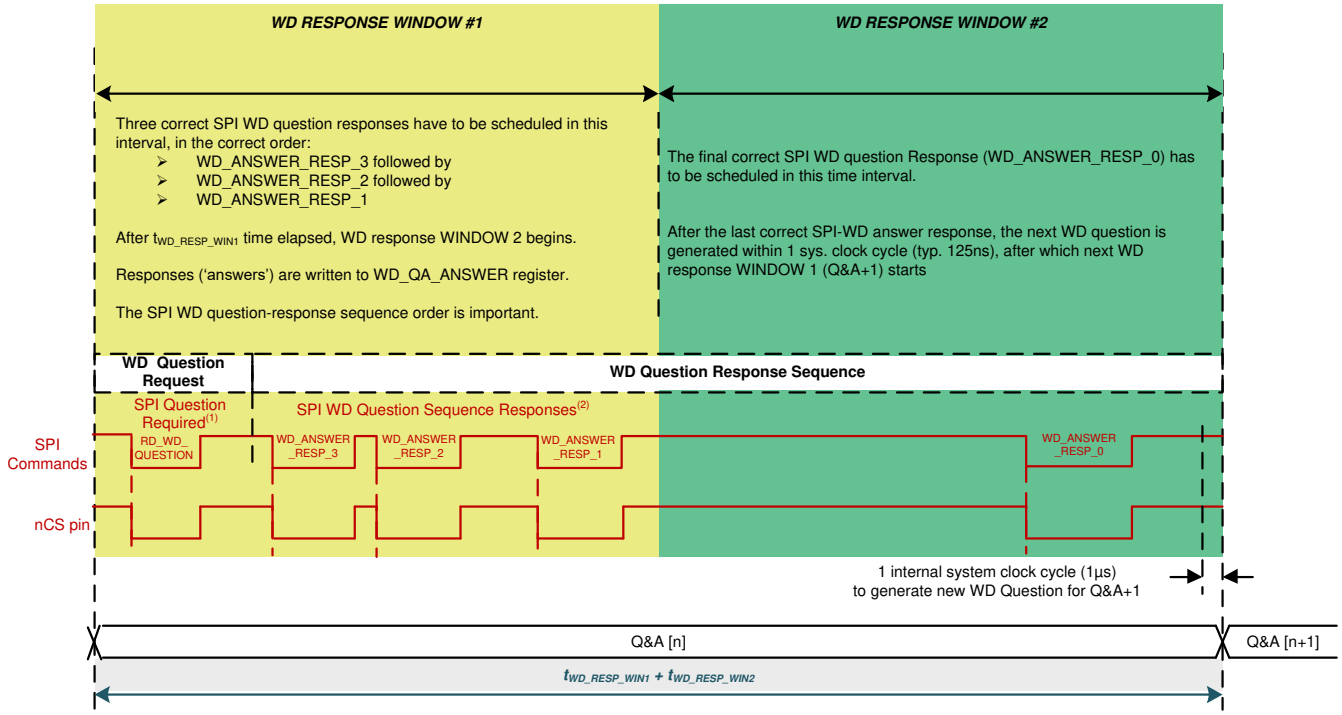
9.3.14.4.1 WD Question and Answer Basic information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write or a pin toggle, the MCU reads a ‘question’ from the TCAN1167-Q1 do math based on the question and then write the computed answers back to the TCAN1167-Q1. The correct answer is a four byte response. Each byte must be written in order and with the correct timing to have a correct answer.

There are two watchdog windows; referred to as WD Response window #1 and WD Response window #2 (Figure 9-5 WD QA Windows as example). The size of each window will be 50% of the total watchdog time, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is the MCU reads the question, when the question is read, the timer starts. The CPU must perform a mathematical function on the question, resulting in four bytes of answers. Three of the four answer bytes must be written to the answer register within the first window, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all four answer bytes were correct and in the correct order, then the response is considered good and a new question is generated, starting the cycle over again. Once the fourth answer is written into WD Response Window #2, that window is terminated and a new WD Response Window #1 is started.

If anything is incorrect or missed, the response is considered bad and the watchdog question will NOT change. In addition, an error counter will be incremented. Once this error counter hits a threshold (defined in the WD_ERR_CNT register field), the watchdog failure action will be performed. Examples of actions are an interrupt, or reset toggle, etc.



A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 9-5. WD Q&A Sequence Run for WD Q&A Multi-Answer Mode

9.3.14.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, Table 9-4.

Table 9-4. List of Watchdog Related Registers

Register Address	Register Name	Description
0x13	WD_CONFIG_1	Watchdog configuration and action in event of a failure
0x14	WD_CONFIG_2	Sets the time of the window, and shows current error counter value
0x15	WD_INPUT_TRIG	Register to reset or start the watchdog
0x16	WD_RST_PULSE	Reset pulse width in event of watchdog failure

Table 9-4. List of Watchdog Related Registers (continued)

Register Address	Register Name	Description
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to Table 9-3 to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, it is recommended that windows greater than 64 ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter hits the error counter threshold.

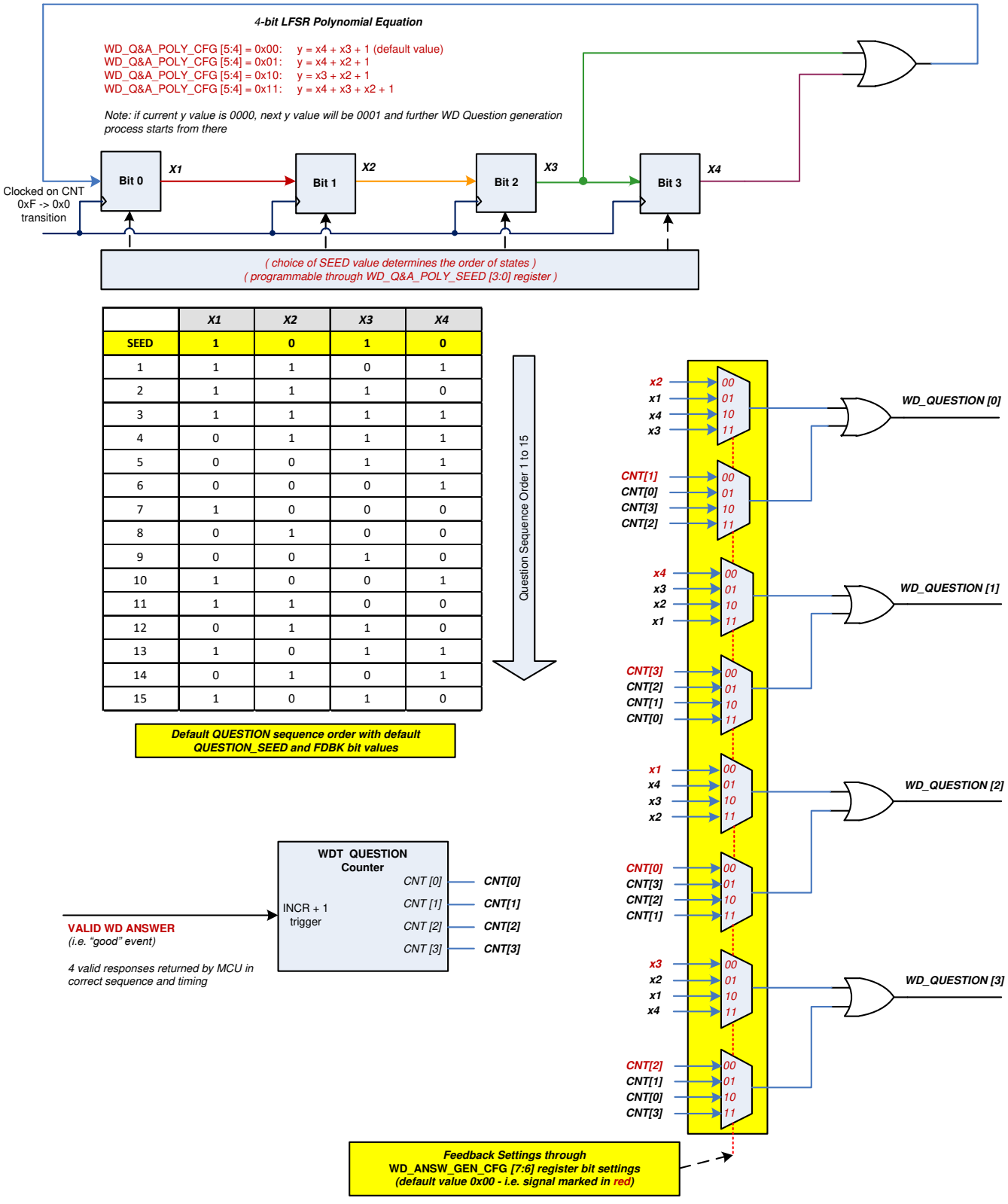
9.3.14.4.3 WD Question and Answer Value Generation

The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- For WD Q&A multi-answer:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION[3:0] bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from b1111 to b0000. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QUESTION [3:0] generation is given in Figure 9-6.



	X1	X2	X3	X4
SEED	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

A. If the current *y* value is 0000, the next *y* value is 0001. The next watchdog question generation process starts from that value.

Figure 9-6. Watchdog Question Generation

Table 9-5 contains the answers for each question, as long as the question polynomial and answer generation configuration are both at their default values.

Table 9-5. Example answers to questions with default settings

QUESTION IN WD_QUESTION_VALUE REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT 2'b11	WD_ANSW_CNT 2'b10	WD_ANSW_CNT 2'b01	WD_ANSW_CNT 2'b00
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

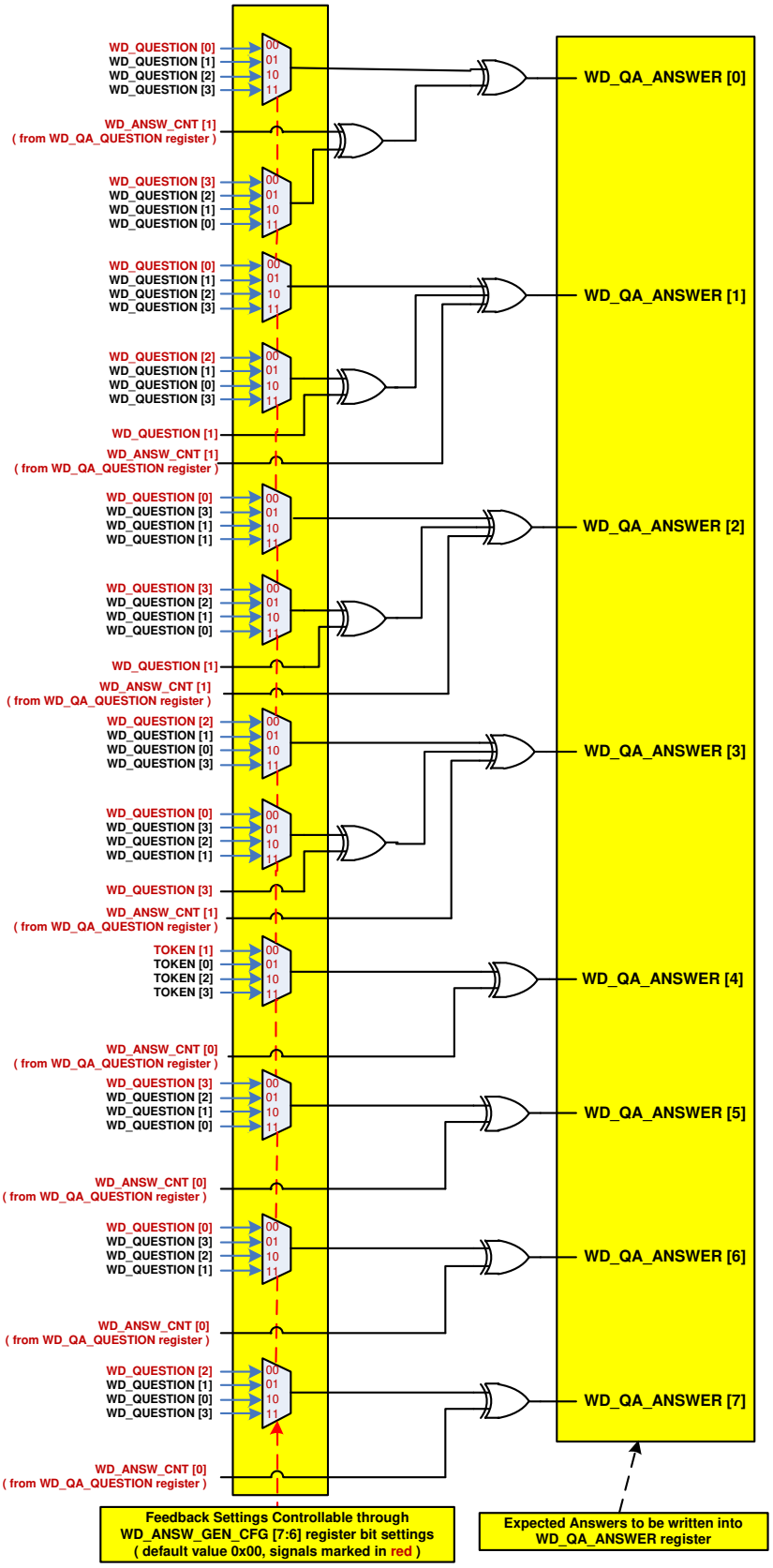


Figure 9-7. WD Expected Answer Generation

Table 9-6. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WD_QA_QUESTION REGISTER		COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		QA_ANSW_ERR	WD_ERR(1)	
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	No answers
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Total WD_ANSW_CNT[1:0] = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer				
2 CORRECT answer	1 CORRECT answer				
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer				
2 CORRECT answer	1 INCORRECT answer				
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 CORRECT ANSWER in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answer				
2 CORRECT answer	2 CORRECT answer				
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 CORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answer				
2 CORRECT answer	2 INCORRECT answer				
0 answer	3 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	
2 INCORRECT answer	1 CORRECT answer				
0 answer	3 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answer				
2 INCORRECT answer	1 INCORRECT answer				
0 answer	4 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answer		1b	1b	
2 INCORRECT answer	2 CORRECT answer				
0 answer	4 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Less than 3 INCORRECT ANSWER in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answer				
2 INCORRECT answer	2 INCORRECT answer				
3 CORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	0b	1b	Less than 4 CORRECT ANSW in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answer	0 answer		0b	1b	
1 CORRECT answer	0 answer				
3 CORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	0b	CORRECT SEQUENCE

Table 9-6. Correct and Incorrect WD Q&A Sequence Run Scenarios for WD Q&A Multi-Answer Mode (WD_CFG = 0b) (continued)

NUMBER OF WD ANSWERS		ACTION	WD STATUS BITS IN WD_QA_QUESTION REGISTER		COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2		QA_ANSW_ERR	WD_ERR(1)	
3 CORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] < 4
3 INCORRECT answer	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
3 INCORRECT answer	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	Total WD_ANSW_CNT[1:0] = 4
4 CORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	0b	1b	
3 CORRECT answer + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	1b	4 CORRECT or INCORRECT ANSWER in RESPONSE WINDOW 1
2 CORRECT answer + 2 INCORRECT answer	Not applicable				
1 CORRECT answer + 3 INCORRECT answer	Not applicable				

9.3.14.5 Question and Answer WD Example

For this example, we'll walk through a single sequence with the following configuration settings, Table 9-7.

Table 9-7. Example Configuration Settings

Item	Value	Description
Watchdog window size	1024 ms	Window size of 1024 ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	9 (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

9.3.14.5.1 Example configuration for desired behavior

Table 9-8 register writes will configure the part for the example behavior specified above. Most of the settings are power on defaults.

Table 9-8. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11011101 / 0xDD
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

9.3.14.5.2 Example of performing a question and answer sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the four answer bytes
3. Send three of them within the first response window
4. Wait and send the last byte in the second response window

See Table 9-9 for an example of the first loop sequence.

Table 9-9. Example First Loop

Step	Register	Data	Description
1	WD_INPUT_TRIG (0x15)	[W] 0xFF	Start the watchdog (since it isn't started yet), also keep a timer internally to flag when response window 1 ends and window 2 starts.
2	WD_QA_QUESTION (0x2F)	[R] 0x3C	Read the question. Question is 0x3C
3	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3 (See Table 9-5 example answers to questions with default settings to see answers)
4	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
5	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
6	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

At this point, you can read the WD_QA_QUESTION (0x2F) register to see if the error counter has increased or if QA ERROR is set.

9.3.15 Bus Fault Detection and Communication

The TCAN1167-Q1 provides advanced bus fault detection. TCAN1167-Q1 is used for illustration purposes. The device can determine certain fault conditions and set a status/interrupt flag so that the MCU can understand what the fault is. Detection takes place and is recorded if the fault is present during four dominant to recessive transitions with each dominant bit being ≥ 2 µs. As with any bus architecture where termination resistors are at

each end not every fault can be specified to the lowest level, meaning exact location. The fault detection circuitry is monitoring the CANH and CANL pins (currents) to determine if there is a short to battery, short to ground, short to each other or opens. From a system perspective, the location of the device can impact what fault can be detected. See Figure 9-8 as an example of node locations and how they can impact the ability to determine the actual fault location. Figure 9-9 through Figure 9-13 show the various bus faults based upon the three node configuration. Table 9-10 shows what can be detected and by which device. Fault 1 is detected as ½ termination and Fault 2 is detected as no termination.

Bus fault detection is a system-level situation. If the fault is occurring at the ECU then the general communication of the bus is compromised. For complete coverage of a node a system level diagnostic step for each node and the ability to communicate this back to a central point is needed.

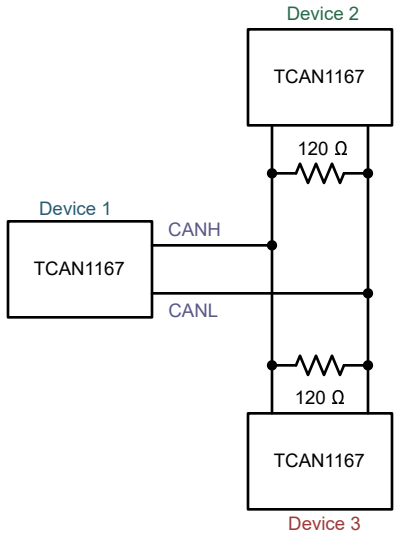
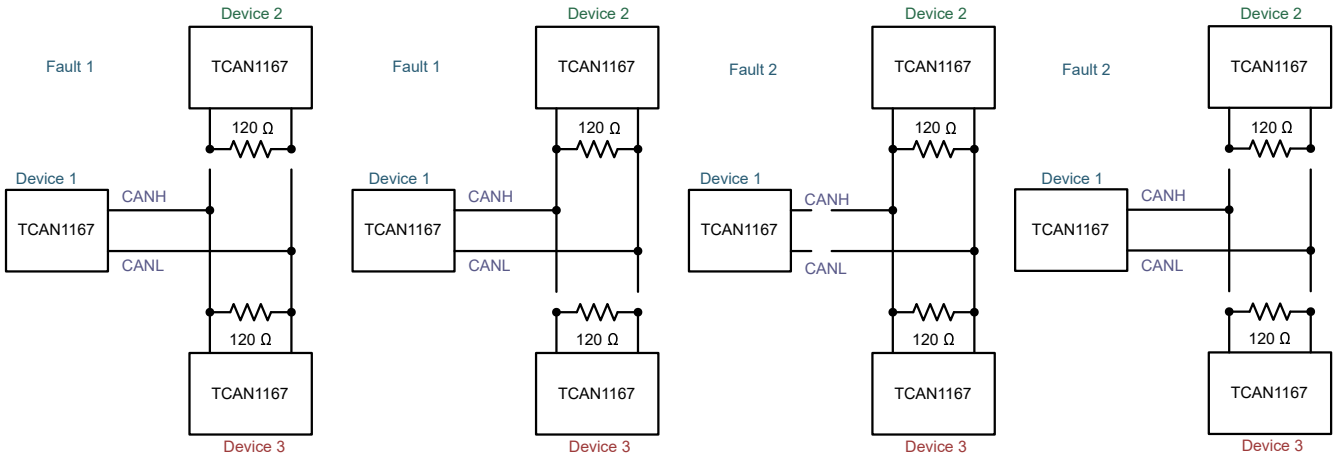


Figure 9-8. Three Node Example



- Fault 1 is any case where ½ termination is seen
- Fault 2 is any case where no termination is seen

Figure 9-9. Fault 1 and 2 Examples

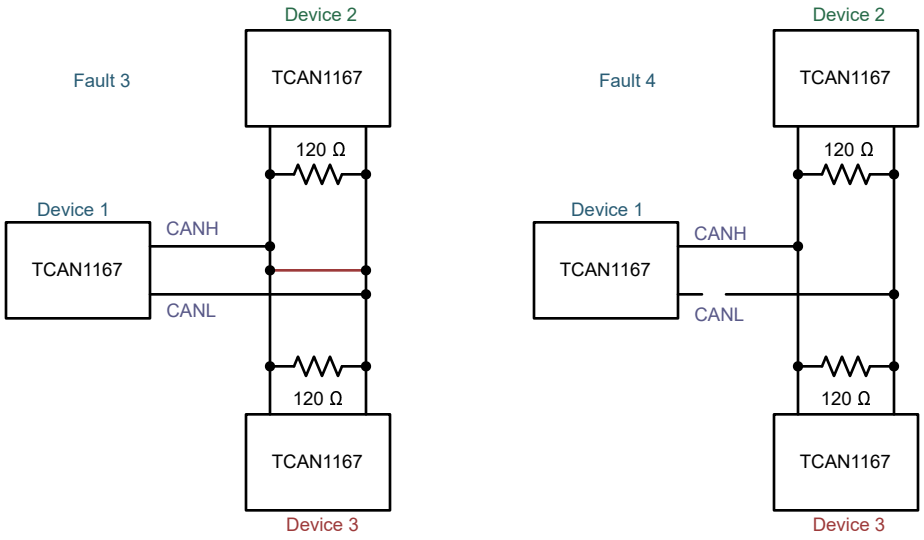


Figure 9-10. Fault 3 and 4 Examples

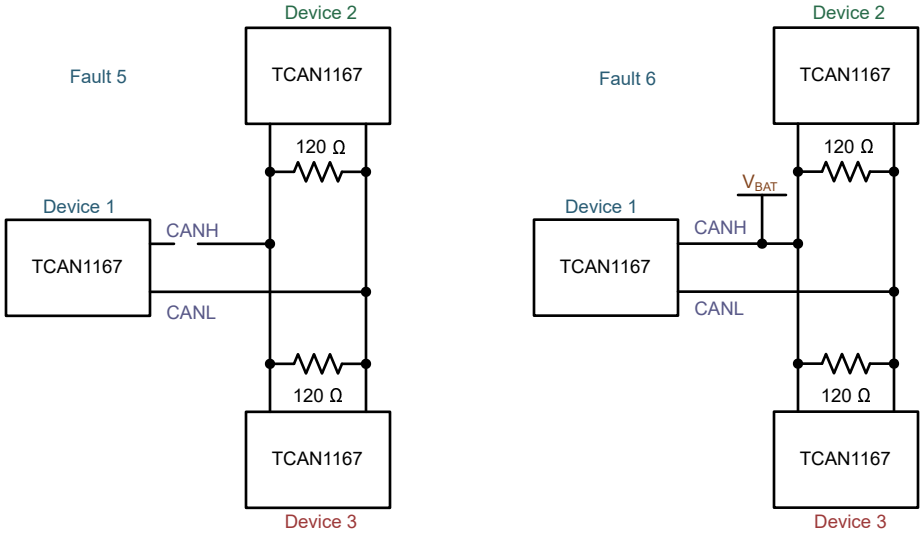


Figure 9-11. Fault 5 and 6 Examples

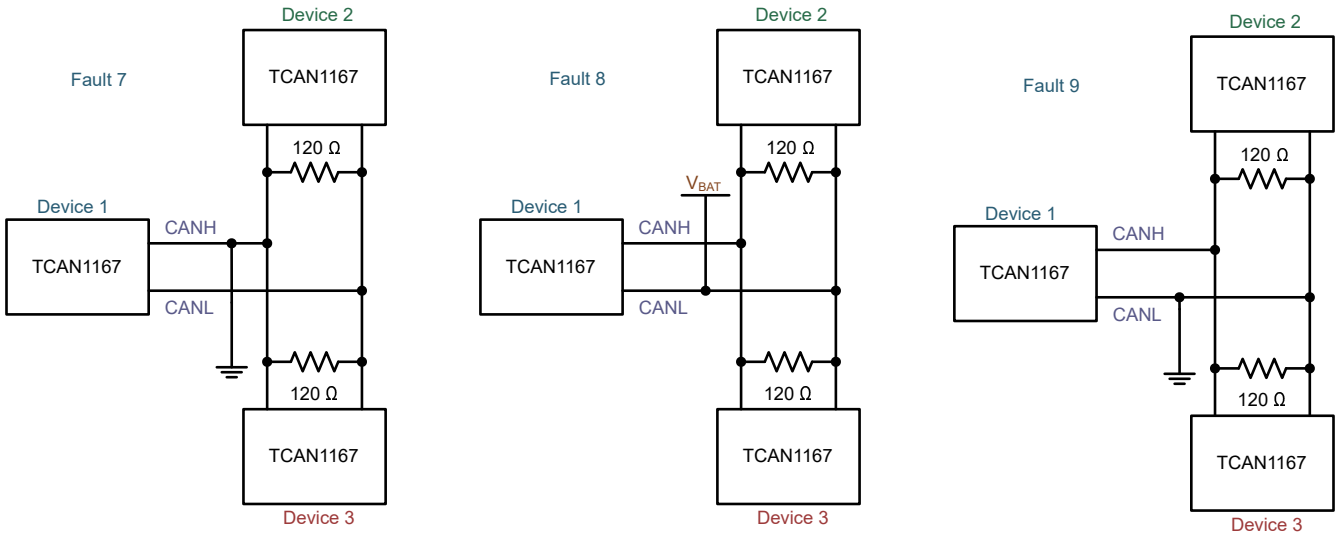


Figure 9-12. Fault 7, 8 and 9 Examples

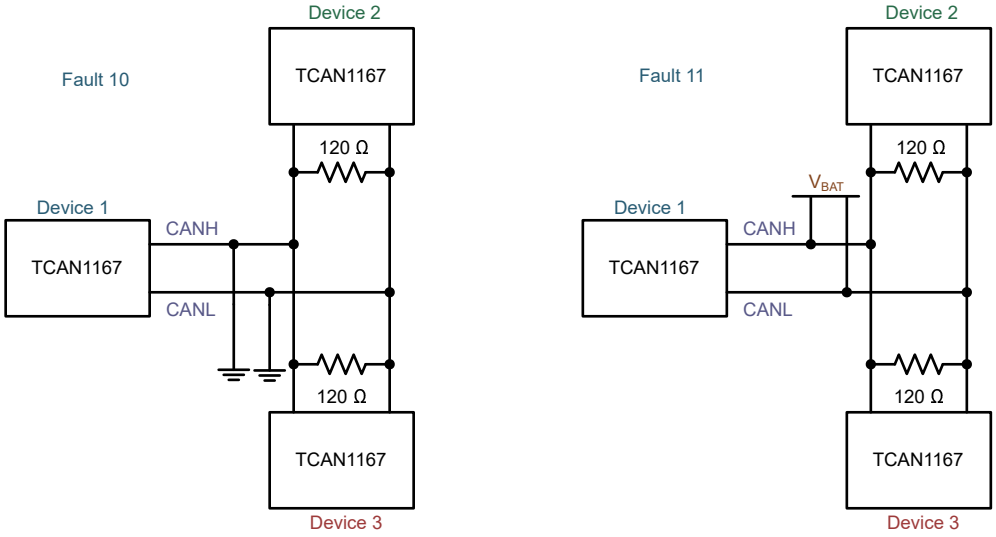


Figure 9-13. Fault 10 and 11 Examples

Table 9-10. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Fault Detected
1	Open	Open	All positions see this fault as half termination and detect them
2	Open	Open	Depending upon open location the device detects this as no termination.
3	Open	Normal	Yes but cannot tell the difference between it and Fault 2 and 4; Device 2 and Device 3 does not see this fault
4	Normal	Open	Yes but cannot tell the difference between it and Fault 2 and 3; Device 2 and Device 3 does not see this fault
5	Shorted to CANL	Shorted to CANH	Yes but not location
6	Shorted to V_{bat}	Normal	Yes but not location
7	Shorted to GND	Normal	Yes but cannot tell the difference between this and Fault 10
8	Normal	Shorted to V_{bat}	Yes but cannot tell the difference between this and Fault 11
9	Normal	Shorted to GND	Yes but not location
10	Shorted to GND	Shorted to GND	Yes but cannot tell the difference between this and Fault 7
11	Shorted to V_{bat}	Shorted to V_{bat}	Yes but cannot tell the difference between this and Fault 8

Table 9-11. Bus Fault Interrupt Flags Mapping to Fault Detection Number

Address	BIT(S)	DEFAULT	FLAG	DESCRIPTION	FAULT DETECTED	ACCESS
8'h54	7	1'b0	RSVD	Reserved		
	6	1'b0	CANBUSTERMOPEN	CAN Bus has one termination point open	Fault 1	R/WC
	5	1'b0	CANHCANL	CANH and CANL Shorted Together	Fault 5	R/WC
	4	1'b0	CANHBAT	CANH Shorted to V_{bat}	Fault 6	R/WC
	3	1'b0	CANLGND	CANL Shorted to GND	Fault 9	R/WC
	2	1'b0	CANBUSOPEN	CAN Bus Open (One of three possible places)	Faults 2, 3 and 4	R/WC
	1	1'b0	CANBUSGND	CANH Shorted to GND or Both CANH & CANL Shorted to GND	Faults 7 and 10	R/WC
	0	1'b0	CANBUSBAT	CANL Shorted to Vbat or Both CANH & CANL Shorted to Vbat	Faults 8 and 11	R/WC

9.4 Device Functional Modes

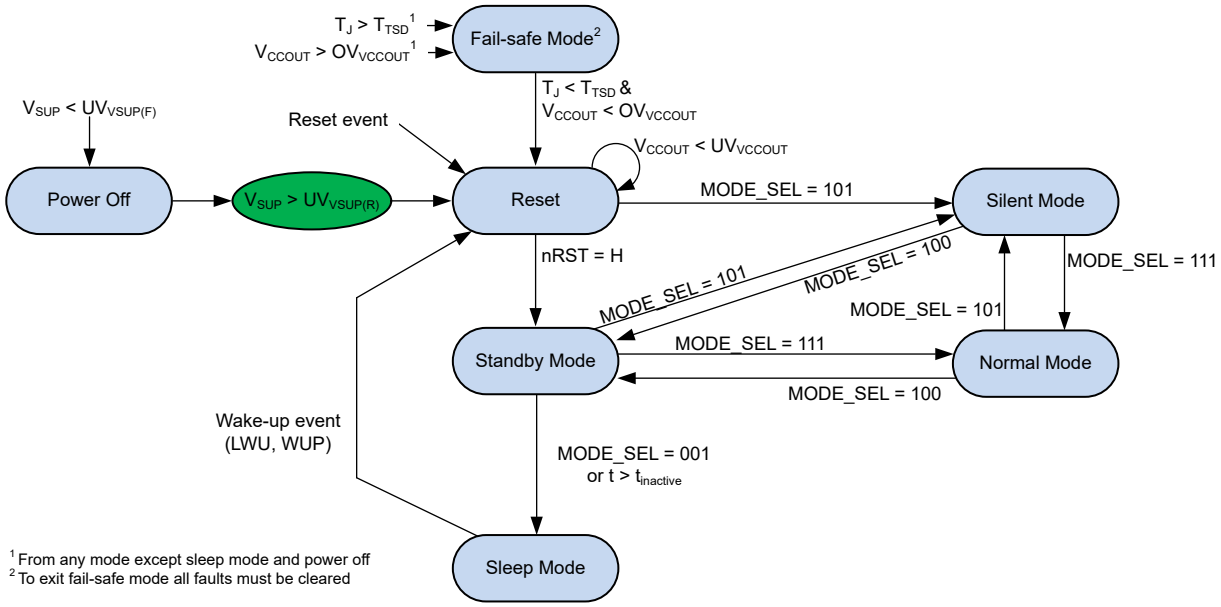


Figure 9-14. TCAN1167 State Machine

Table 9-12. TCAN1167 Mode Overview

Block	Power Off	Reset	Fail-safe	Normal	Standby	Silent	Sleep
V_{CCOUT}	Off	On	Off	On	On	On	Off
INH	Off	V_{SUP}	V_{SUP}	V_{SUP}	V_{SUP}	V_{SUP}	Off
Low Power CAN RX	Off	Off	Fault determines	Off	Active	Off	Active
CAN Transmitter	Off	CAN Autonomous	Off	CAN Active	CAN Autonomous	Off	CAN Autonomous
CAN Receiver	Off	CAN Autonomous	Off	CAN Active	CAN Autonomous	CAN Active	CAN Autonomous
RXD	High impedance	V_{CCOUT}	V_{CCOUT}	Mirrors Bus State	Entrance Dependent	Mirrors Bus State	V_{CCOUT}
Watchdog	Off	Off	Off	Active	Active	Active	Off
SPI	Disabled	Disabled	Fault determines	Active	Active	Active	Disabled

9.4.1 Operating Mode Description

9.4.1.1 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The $t_{INACTIVE}$ timer in not active in normal mode.

9.4.1.2 Silent Mode

Silent mode is commonly referred to as listen only and receive only mode. In this mode, the CAN driver is disabled but the receiver is fully operational and CAN communication is unidirectional into the device. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD terminal.

Silent mode is similar to normal mode, excep that TXD is ignored. RXD works just the same as normal mode.

9.4.1.3 Standby Mode

The RXD output pin is asserted low while in standby mode if the a wake event or a fault is detected. Note that a POR counts as a wake event and will also cause RXD to latch low.

In standby mode a fail-safe timer, $t_{INACTIVE}$, is enabled. The $t_{INACTIVE}$ timer add an additional layer of protection by requiring the system controller to configure the TCAN1167-Q1 to normal mode before it expires. This feature forces the TCAN1167-Q1 to transition to its lowest power mode, sleep mode, if the processor does not come up properly.

9.4.1.4 Sleep Mode

Sleep mode is the lowest power mode of the TCAN1167-Q1 where the CAN transceiver is placed in the CAN autonomous inactive state by changing to sleep mode via a SPI write. In sleep mode, the CAN transmitter and receiver are switched off, the bus pins are biased to ground after $t_{SILENCE}$ expires, and the transceiver cannot send or receive data. The INH pin is switched off in sleep mode causing any system power elements controlled by INH to be switched off thus reducing system power consumption. While in sleep mode, the low power receiver actively monitors the CAN bus for a valid wake-up pattern and the I_{SUP} current is reduced to its minimum level.

Sleep mode is entered if:

- Write sleep mode to the MODE_SEL bits in the SPI mode control register.
- SWE timer expires (see Sleep Wake Error Timer)

Sleep mode is exited if:

- If a valid wake-up pattern (WUP) is received via the CAN bus pins
- A local WAKE (LWU) event
- A reset event occurs (goes to reset mode)

9.4.1.4.1 Remote Wake Request via Wake-Up Pattern (WUP)

The TCAN1167-Q1 implements a low-power wake receiver in the standby and sleep mode that uses the multiple filtered dominant wake-up pattern (WUP) defined in the ISO11898-2:2016 standard.

The wake-up pattern (WUP) consists of a filtered dominant bus, then a filtered recessive bus time followed by a second filtered bus time. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic do not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant. The other bus traffic do not reset the bus monitor. Immediately upon receiving of the second filtered dominant, the bus monitor recognizes the WUP and drives the RXD terminal low.

The WUP consists of:

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP, and a wake request may be generated. Bus state times more than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is generated. See Figure 9-15 for the timing diagram of the WUP.

The pattern and t_{WK_FILTER} time used for the WUP and wake request prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a wake request.

ISO11898-2:2016 has two sets of times for a short and long wake-up filter times. The t_{WK_FILTER} timing for the TCAN1167-Q1 has been picked to be within the min and max values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back to back bit times at 1 Mbps triggers the filter in either bus state.

For an additional layer of robustness and to prevent false wake-ups, the device implements the $t_{WK\_TIMEOUT}$ timer. For a remote wake-up event to successfully occur, the entire wake-up pattern must be received within the timeout value. If a the full wake-up pattern is notreceived before the $t_{WK\_TIMEOUT}$ expires, then the internal logic is reset and the device remains in sleep mode without waking up. The full pattern must then be transmitted again within the $t_{WK\_TIMEOUT}$ window. See Figure 9-15.

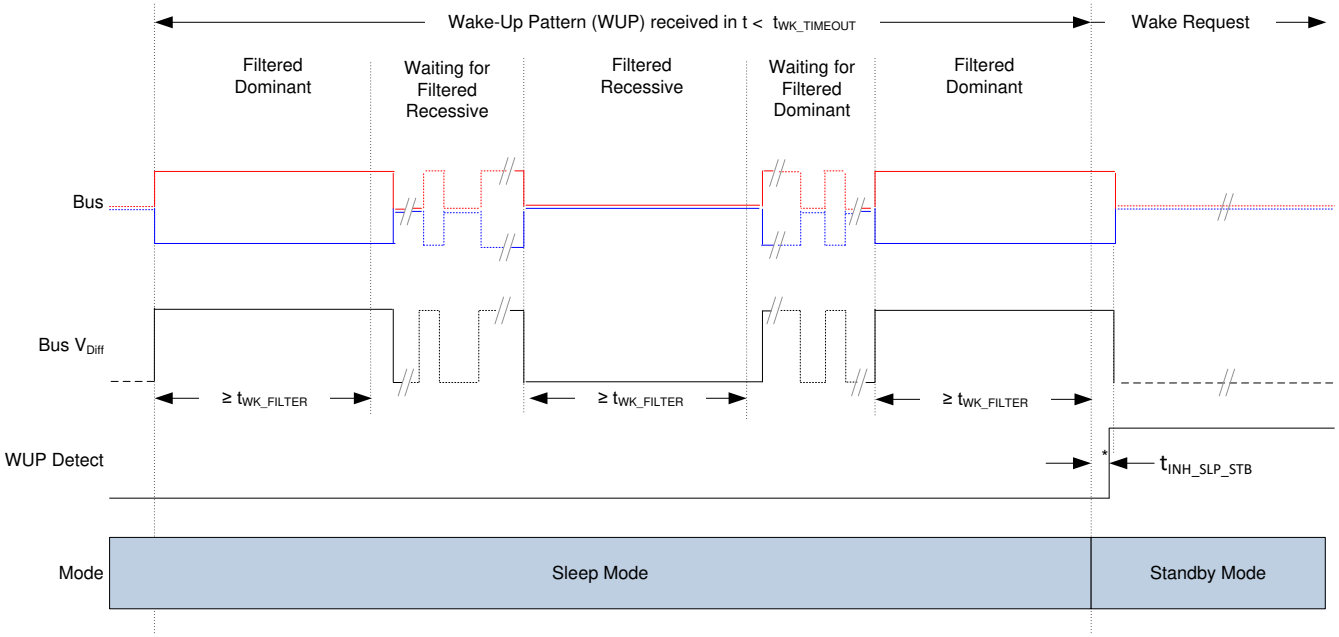


Figure 9-15. Wake-Up Pattern (WUP) From Sleep Mode To Standby Mode

9.4.1.4.2 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage reverse battery protected input which can be used for local wake-up (LWU) requests via a voltage transition. A LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin could be used with a switch to V_{SUP} or to ground. If the terminal is unused, it should be pulled to V_{SUP} or ground to avoid unwanted parasitic wake-up events.

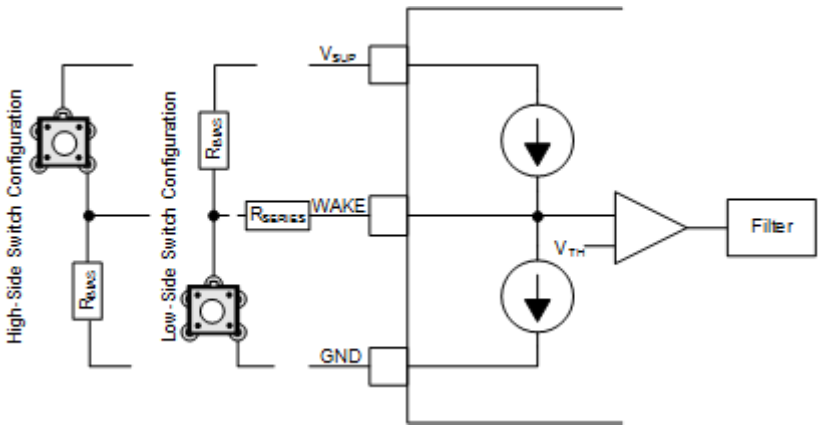


Figure 9-16. WAKE Circuit Example

Figure 9-16 shows two possible configurations for the WAKE pin, a low-side and high-side switch configuration. The objective of the series resistor, R_{SERIES}, is to protect the WAKE input of the device from over current conditions that may occur in the event of a ground shift or ground loss. The minimum value of R_{SERIES} can be calculated using the maximum supply voltage, V_{SUPMAX}, and the maximum allowable current of the WAKE pin, $I_{IO(WAKE)}$. R_{SERIES} is calculated using:

$$R_{SERIES} = V_{SUPMAX} / I_{IO(WAKE)} \quad (3)$$

If the battery voltage never exceeds 42 V_{DC}, then the R_{SERIES} value is approximately 10 kΩ.

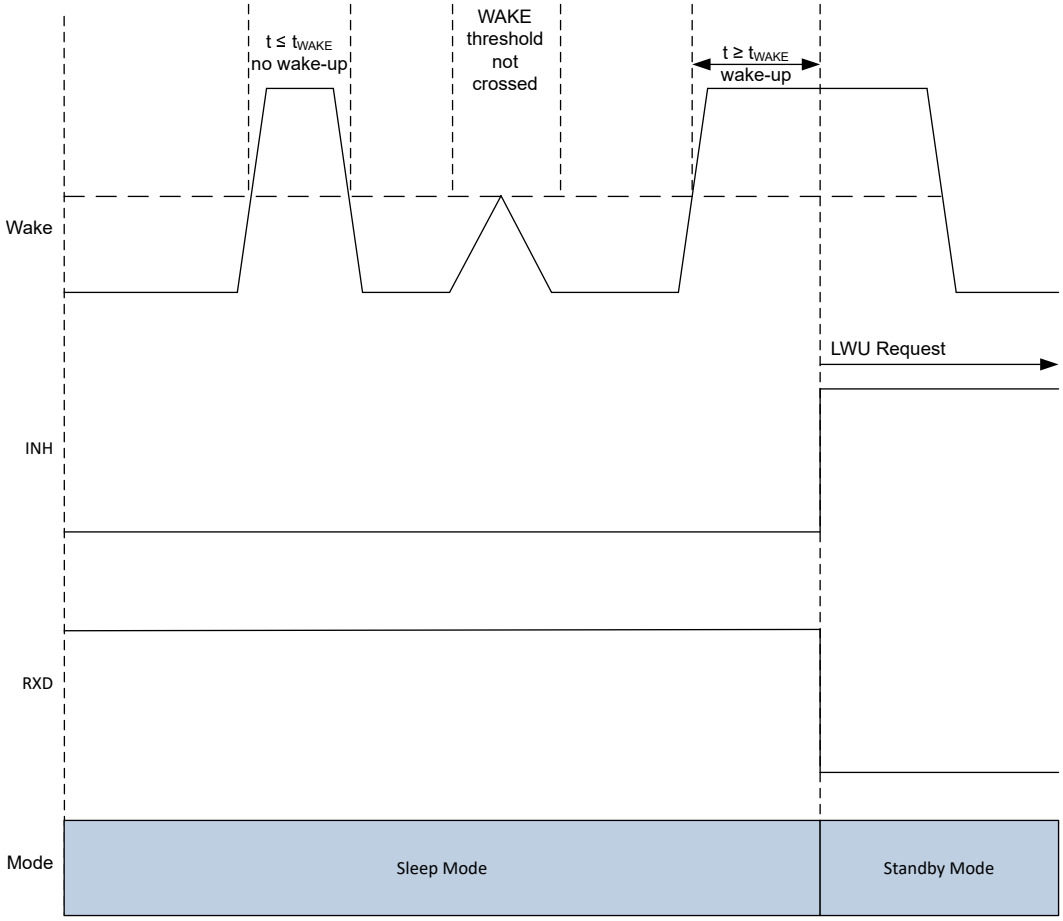
The R_{BIAS} resistor is used to set the static voltage level of the WAKE input when the switch is not in use. When the switch is in use in a high-side switch configuration, the R_{BIAS} resistor in combination with the R_{SERIES} resistor sets the WAKE pin voltage above the V_{IH} threshold. The maximum value of R_{BIAS} can be calculated using the maximum supply voltage, V_{SUPMAX}, the maximum WAKE threshold voltage V_{IH}, the maximum WAKE input current I_{IH} and the series resistor value R_{SERIES}. R_{BIAS} is calculated using:

$$R_{BIAS} < ((V_{SUPMAX} - V_{IH}) / I_{IH}) - R_{SERIES} \quad (4)$$

If the battery voltage never exceed 42 V_{DC}, then the R_{BIAS} resistor value must be less than 650-kΩ.

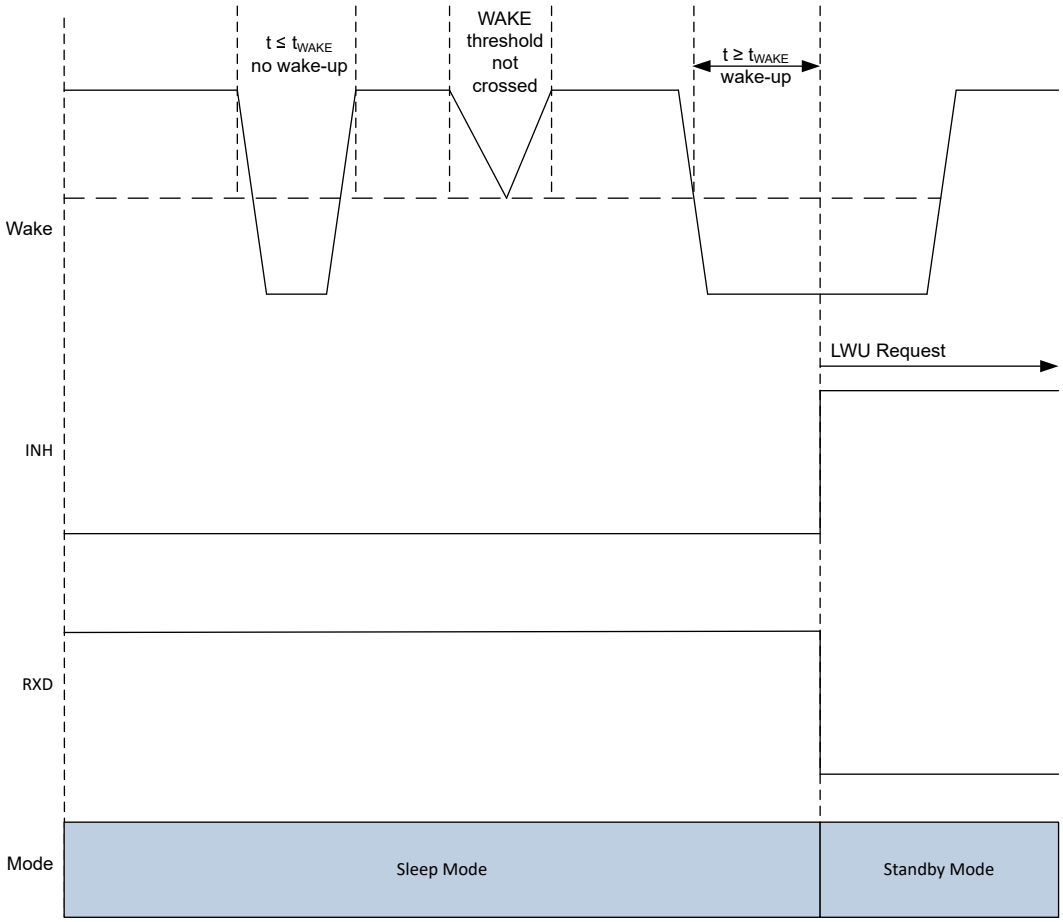
The LWU circuitry is active in sleep mode. .

The WAKE circuitry is switched off normal mode.



The RXD pin is only driven once V_{CCOUT} is present.

Figure 9-17. LWU Request Rising Edge



The RXD pin is only driven once V_{CCOUT} is present.

Figure 9-18. LWU Request Falling Edge

9.4.1.5 Reset Mode

Reset mode is a low power mode of the TCAN1167-Q1 where the nRST pin is asserted low allowing the controller to power up correctly. In this state the CAN transmitter and receiver are off, the bus pins are biased to ground, and the transceiver cannot send or receive data.

While in reset mode the low power receiver actively monitors the CAN bus for a valid wake-up pattern. If a valid wake-up pattern is received the CAN bus pins transition to the CAN autonomous active state where CANH and CANL are internally biased to 2.5 V from the V_{SUP} power rail. The reception of a valid wake-up pattern generates a wake-up request by the CAN transceiver that is output to the RXD pin.

The TCAN1167-Q1 will enter reset mode due to following conditions:

- Power-on
- nRST pulled low externally

The TCAN1167-Q1 will enter reset mode upon clearing any of the following fault conditions and leaving fail-safe mode:

- $T_J < T_{SDF}$
- Over voltage event

9.4.1.6 Fail-safe Mode

Fail-safe mode is a low power mode in which the TCAN1167-Q1 is in a protected state. While in fail-safe mode the internal regulator (V_{CCOUT}) is off, the INH pin is off, the reset pin is low, and the CAN transmitter and receiver are off.

Fail-safe mode is entered if:

- $T_J > T_{SDR}$
- $V_{VCCOUT} > OV_{CCOUTR}$

Fail-safe mode is exited if all of the following criteria are met:

- $T_J < T_{SDF}$
- $V_{VCCOUT} < OV_{CCOUTF}$
- A valid wake-up event exists

If the fault condition is not cleared within $t_{INACTIVE}$ then the device will transition into it's lowest power mode, sleep mode.

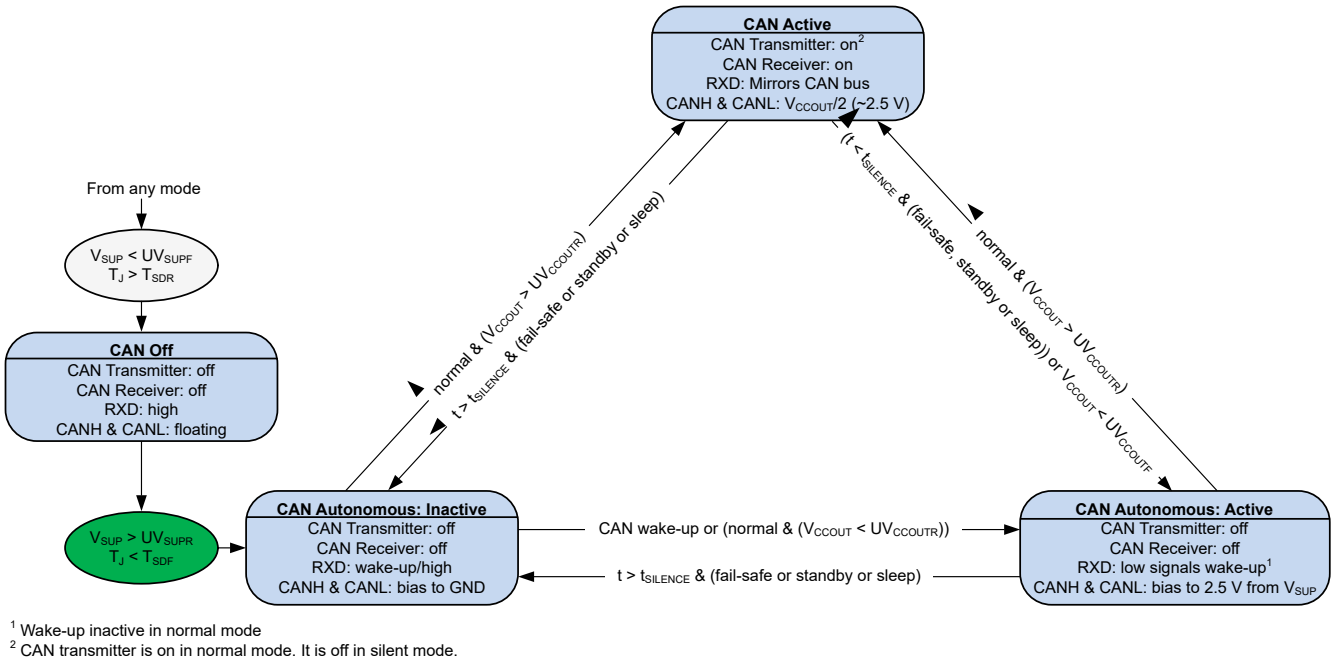
9.4.2 CAN Transceiver

9.4.2.1 CAN Transceiver Operation

The TCAN1167-Q1 CAN transverse has three modes of operation; CAN active, CAN autonomous active, and CAN autonomous inactive.

9.4.2.2 CAN Transceiver Modes

The TCAN1167-Q1 supports the ISO 11898-2:2016 CAN physical layer standard autonomous bus biasing scheme. Autonomous bus biasing enables the transceiver to switch between CAN active, CAN autonomous active, and CAN autonomous inactive which helps to reduce RF emissions.



[1] Wake-up inactive in normal mode
[2] CAN transmitter is on in normal mode. It is off in silent mode.

Figure 9-19. TCAN1167 CAN Transceiver State Machine

9.4.2.2.1 CAN Off Mode

In CAN off mode the CAN transceiver is switched off and the CAN bus lines are truly floating. In this mode the device presents no load to the CAN bus while preventing reverse currents from flowing into the device if the battery or ground connection is lost.

The CAN off state is entered if:

- $T_J > T_{SDR}$
- $V_{SUP} < UV_{SUPF}$

The CAN transceiver switches between the CAN off state and CAN autonomous inactive mode if:

- $V_{SUP} > UV_{SUPR}$
- $T_J < T_{SDF}$

9.4.2.2.2 CAN Autonomous: Inactive and Active

When the CAN transceiver is in standby mode or sleep mode the CAN bias circuit is switched off and the transceiver moves to the autonomous inactive state. In the autonomous inactive state the CAN pins are biased to GND. When a valid wake-up event occurs the CAN bus is biased to 2.5 V. If the controller does not transition the TCAN1167-Q1 into normal mode before the $t_{SILENCE}$ timer expires, then the CAN biasing circuit is again switched off and the CAN pins are biased to ground.

The CAN transceiver switches to the CAN autonomous mode if any of the following conditions are met:

- The TCAN1167-Q1 transitions from CAN off mode to CAN autonomous inactive

The CAN transceiver switches between the CAN autonomous inactive mode and CAN autonomous active mode if:

- A valid wake-up event
- The TCAN1167-Q1 transitions to normal mode and no undervoltage faults exist.

The CAN transceiver switches between the CAN autonomous active mode and CAN autonomous inactive mode if:

- t > $t_{SILENCE}$ and the TCAN1167-Q1 transitions to standby mode, sleep mode, or fail-safe mode.

9.4.2.2.3 CAN Active

When the TCAN1167-Q1 is in normal mode the CAN transceiver is in active mode. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The CAN bias voltage in CAN active mode is derived from:

- V_{CCOUT}

The CAN transceiver switches between the CAN autonomous inactive or active mode and CAN active mode if:

- The TCAN1167-Q1 transitions to normal mode and no undervoltage faults exist.

The CAN transceiver blocks its transmitter and receiver after entering CAN active mode if the TXD pin is asserted low before leaving standby mode. This prevents disruptions to CAN bus in the event that the TXD pin has a TXD DTO fault.

When the TCAN1167-Q1 is in silent mode the CAN driver is disabled, but the receiver is fully operational. The CAN bias voltage is derived from the same CAN active mode.

9.4.2.3 Driver and Receiver Function Tables

Table 9-13. Driver Function Table

DEVICE MODE	TXD INPUTS(1)	BUS OUTPUTS		DRIVEN BUS STATE(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or Open	High impedance	High impedance	Biased to V_{CCOUT}/2
Silent	x	High impedance	High impedance	Biased to V_{CCOUT}/2
Standby	x	High impedance	High impedance	Biased to GND
Sleep	x	High impedance	High impedance	Biased to GND

(1) x = irrelevant
(2) For bus states and typical bus voltages see Figure 9-20

Table 9-14. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} – V_{CANL}$	BUS STATE	RXD TERMINAL
Normal/Silent	V_{ID} ≥ 0.9 V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Indeterminate	Indeterminate
	V_{ID} ≤ 0.5 V	Recessive	High
	Open (V_{ID} ≈ 0 V)	Open	High
Standby	V_{ID} ≥ 1.15 V	Dominant	High Low if wake-up event persists
	0.5 V < V_{ID} < 1.15 V	Indeterminate	
	V_{ID} ≤ 0.4 V	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	
Sleep	V_{ID} ≥ 1.15 V	Dominant	High Low if wake-up event persists. Tri-state if V_{SUP} are not present
	0.4 V < V_{ID} < 1.15 V	Indeterminate	
	V_{ID} ≤ 0.4 V	Recessive	
	Open (V_{ID} ≈ 0 V)	Open	

9.4.2.4 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 9-20.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to one half of the CAN transceiver supply voltage via the high resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the CAN bus will be greater than the differential voltage of a single CAN driver. The TCAN1167-Q1 CAN transceiver implements low-power standby and sleep modes which enables a third bus state where the bus pins are biased to ground via the high resistance internal resistors of the receiver.

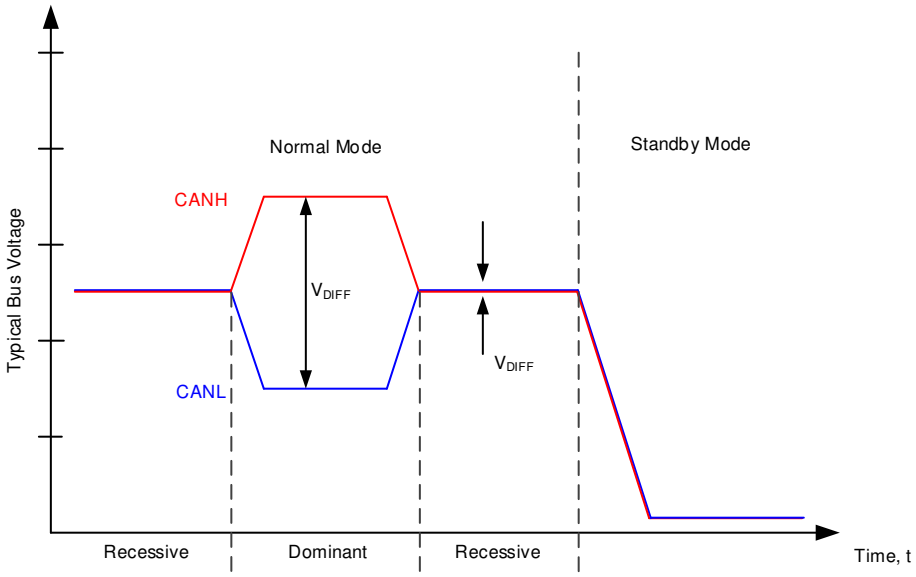


Figure 9-20. Bus States

9.5 Programming

9.5.1 Serial Peripheral Interface (SPI) Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out) and SCLK (Serial Clock). Each SPI transaction is a 16, 24 or 32 bits containing an address and read/write command byte followed by one to three data bytes. The data shifted out on the SDO pin for the transaction always starts with the Global Status Register (byte). This register provides the high level status information about the device status. The two data bytes which are the ‘response’ to the command byte are shifted out next. Data bytes shifted out during a write command is content of the registers prior to the new data being written and updating the registers. Data bytes shifted out during a read command are the content of the registers and the registers is not updated.

The SPI data input data on SDI is sampled on the low to high edge of the clock (SCLK). The SPI output data on SDO is changed on the high to low edge of the clock (SCLK).

When the device is in sleep mode, SPI communication is disabled, and the device must be woken up in order to resume SPI communciation.

9.5.2 Serial Clock Input (SCLK)

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI data input, SDI, is sampled on the falling edge of SPI clock and the SPI data output, SDO, is changed on the falling edge of the SPI clock. See Figure 9-21

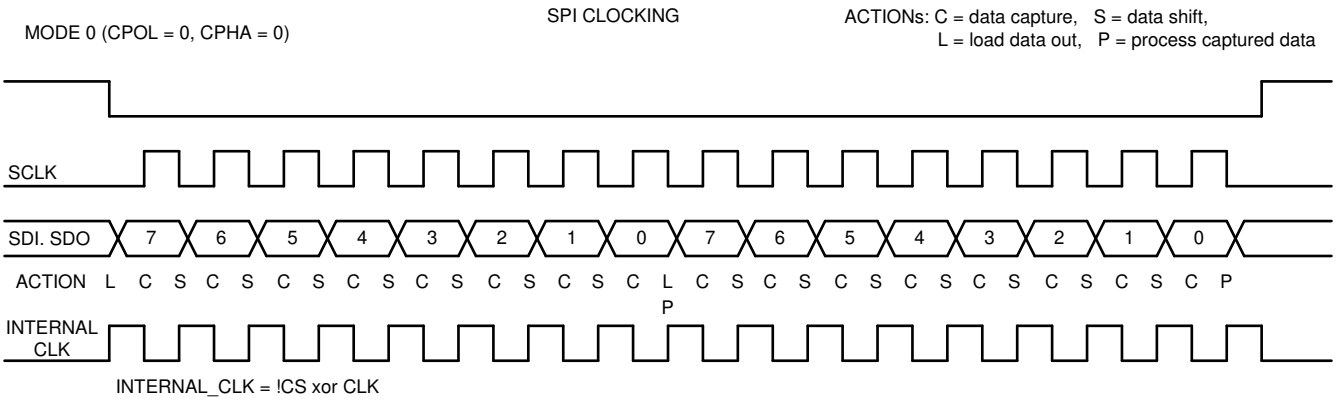


Figure 9-21. SPI Clocking

9.5.3 Serial Data Input (SDI)

The SDI pin is used to let the device know which register address is being read from or written to. During a write, the number of clock cycles determines how many data bytes up to three will be loaded into sequential addresses. The minimum number of clock cycles for a write is 16 supporting the initial address and write command followed by one byte of data as seen in Figure 9-22. The TCAN1167-Q1 supports burst read and write. Figure 9-23 shows an example of a 32-bit write which includes the initial 7-bit address, write bit and three data bytes. This all requires 32 clock cycles. Once the SPI is enabled by a low on nCS, the SDI samples the input data on each rising edge of the SPI clock (SCLK). The data is shifted into an appropriate sized shift register and after the correct number of clock cycles the shift register is full and the SPI transaction is complete. For a write command code, the new data is written into the addressed register only after the exact number of clock cycles have been shifted in by SCLK and the nCS has a rising edge to deselect the device. For a burst write if there are 31 clock cycles of SCLK (1 clock cycle less than the full 3 byte write), the third byte write won't happen while the first two bytes write will be executed. If the correct number of clock cycles and data are not shifted in during one SPI transaction (nCS low), the SPIERR flag is set.

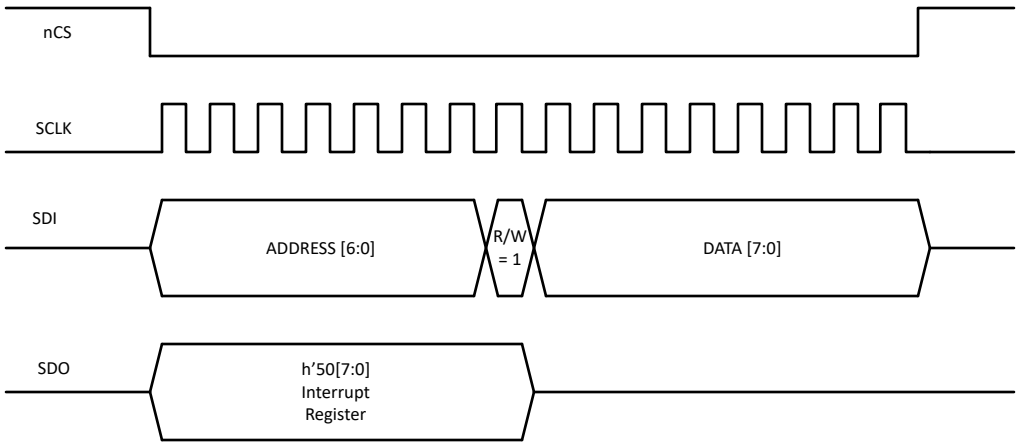


Figure 9-22. SPI Write

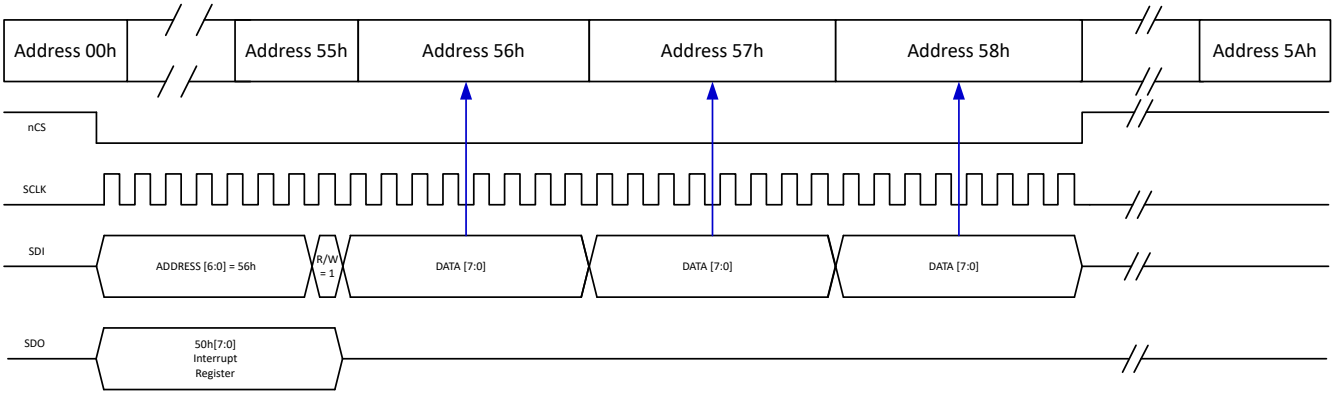


Figure 9-23. 32-bit SPI Burst Write

9.5.4 Serial Data Output (SDO)

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the global interrupt register 8'h50, bit 7. The Global Interrupt register, INT_GLOBAL, is the first byte to be shifted out. The SDO pin provides data out from the device to the processor. For a write command this is the only data that will be provided on the SDO pin. For a read command he one to three bytes of data from successive address will be provided on the SDO line. Figure 9-24 and Figure 9-25 shows examples of a single address read and of a three sequential address read utilizing the 32-bit burst read. The 32-bit burst read shows the global interrupt register followed by the three requested data bytes.

Note

If a read happens faster than 2 µs after a write the global fault flag status may not reflect any status change that the write may have initiated.

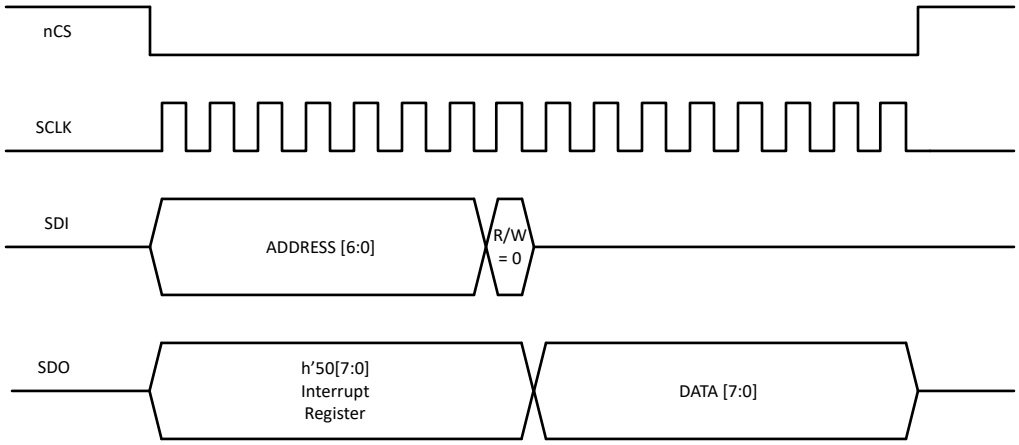


Figure 9-24. SPI Read

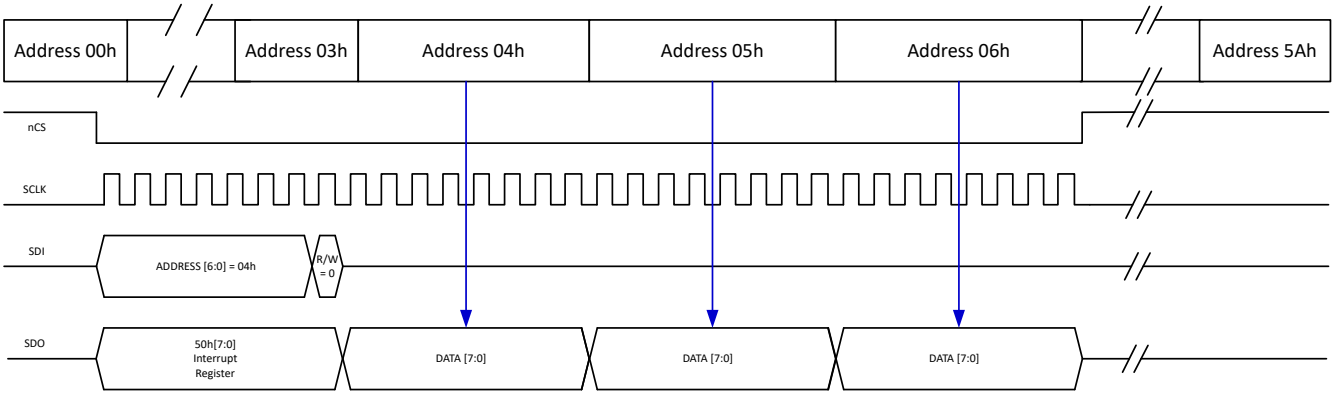


Figure 9-25. 32-bit SPI Burst Read

9.5.5 Chip Select Not (nCS)

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the Serial Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

9.5.6 Registers

Device Registers lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Device Registers should be considered as reserved locations and the register contents should not be modified.

Table 9-15. Device Registers

Address	Acronym	Register Name	Section
0h + formula	DEVICE_ID_y	Device Part Number	Go
8h	REV_ID_MAJOR	Major Revision	Go
9h	REV_ID_MINOR	Minor Revision	Go
Ah + formula	SPI_RSVD_x	SPI reserved registers	Go
Fh	Scratch_Pad_SPI	Read and Write Test Register SPI	Go
10h	MODE_CNTRL	Mode configurations	Go
13h	WD_CONFIG_1	Watchdog configuration 1	Go
14h	WD_CONFIG_2	Watchdog configuration 2	Go
15h	WD_INPUT_TRIG	Watchdog input trigger	Go
2Dh	WD_QA_CONFIG	Q and A Watchdog configuration	Go
2Eh	WD_QA_ANSWER	Q and A Watchdog answer	Go
2Fh	WD_QA_QUESTION	Q and A Watchdog question	Go
40h	STATUS	CAN Transceiver Status	Go
50h	INT_GLOBAL	Global Interrupts	Go
51h	INT_1	Interrupts	Go
52h	INT_2	Interrupts	Go
53h	INT_3	Interrupts	Go
54h	INT_CANBUS	CAN Bus fault interrupts	Go
56h	INT_ENABLE_1	Interrupt enable for INT_1	Go
57h	INT_ENABLE_2	Interrupt enable for INT_2	Go
58h	INT_ENABLE_3	Interrupt enable for INT_3	Go
59h	INT_ENABLE_CANBUS	Interrupt enable for INT_CANBUS	Go
5Ah + formula	INT_RSVD_y	Interrupt Reserved Register INT_RSVD0 through INT_RSVD5	Go

Complex bit access types are encoded to fit into small table cells. Device Access Type Codes shows the codes that are used for access types in this section.

Table 9-16. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	H R	Set or cleared by hardware Read
Write Type		
H	H	Set or cleared by hardware
W	W	Write
W1C	1C W	1 to clear Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

9.5.6.1 DEVICE_ID_y Register (Address = 0h + formula) [reset = xxh]

DEVICE_ID_y is shown in Figure 9-24 and described in Table 9-17.

Return to Summary Table.

Device Part Number

Offset = 0h + y; where y = 0h to 7h

Figure 9-24. DEVICE_ID_y Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-xxh							

Table 9-17. DEVICE_ID_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	0b	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 54h = T Address 01h = 43h = C Address 02h = 41h = A Address 03h = 4Eh = N Address 04h = 31h = 1 Address 05h = 31h = 1 Address 06h = 36h = 6 Address 07h = 37h = 7

9.5.6.2 REV_ID_MAJOR Register (Address = 8h) [reset = 00h]

REV_ID_MAJOR is shown in Figure 9-25 and described in Table 9-18.

Return to Summary Table.

Major Revision

Figure 9-25. REV_ID_MAJOR Register

7	6	5	4	3	2	1	0
Major_Revision							
R-00h							

Table 9-18. REV_ID_MAJOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Major_Revision	R	00h	Major die revision

9.5.6.3 REV_ID_MINOR Register (Address = 9h) [reset = 00h]

REV_ID_MINOR is shown in Figure 9-26 and described in Table 9-19.

Return to Summary Table.

Minor Revision

Figure 9-26. REV_ID_MINOR Register

7	6	5	4	3	2	1	0
Minor_Revision							
R-00h							

Table 9-19. REV_ID_MINOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Minor_Revision	R	00h	Minor die revision

9.5.6.4 SPI_RSVD_x Register (Address = Ah + formula) [reset = 00h]

SPI_RSVD_x is shown in Figure 9-27 and described in Table 9-20.

Return to Summary Table.

Configuration Reserved Bits Ah to Eh

Offset = Ah + x; where x = 0h to 4h

Figure 9-27. SPI_RSVD_x Register

7	6	5	4	3	2	1	0
SPI_RSVD_x							
R-00h							

Table 9-20. SPI_RSVD_x Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPI_RSVD_x	R	00h	SPI reserved registers 0 - 4

9.5.6.5 Scratch_Pad_SPI Register (Address = Fh) [reset = 00h]

Scratch_Pad_SPI is shown in Figure 9-28 and described in Table 9-21.

Return to Summary Table.

Read and Write Test Register SPI

Figure 9-28. Scratch_Pad_SPI Register

7	6	5	4	3	2	1	0
Scratch_Pad							
R/W-00h							

Table 9-21. Scratch_Pad_SPI Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Scratch_Pad	R/W	00h	Read and Write Test Register SPI

9.5.6.6 MODE_CNTRL Register (Address = 10h) [reset = 04h]

MODE_CNTRL is shown in Figure 9-29 and described in Table 9-22.

Return to Summary Table.

Mode select and feature enable and disable register

Figure 9-29. MODE_CNTRL Register

7	6	5	4	3	2	1	0
RSVD			FD_EN	RSVD	MODE_SEL		
R-000b			R/W-0b	R-0b	R/W-100b		

Table 9-22. MODE_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RSVD	R	000b	Reserved
4	FD_EN	R/W	0b	Fault detection enable 0b = Disabled 1b = Enabled

Table 9-22. MODE_CNTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RSVD	R	0b	Reserved
2-0	MODE_SEL	R/W	100b	Mode of operation select 001b = Sleep 100b = Standby 101b = Silent 111b = Normal **Note** NOTE: The current mode will be read back and all other values are reserved

9.5.6.7 WD_CONFIG_1 Register (Address = 13h) [reset = 54h]

WD_CONFIG_1 is shown in Figure 9-30 and described in Table 9-23.

Return to Summary Table.

Watchdog configuration setup 1

Figure 9-30. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		WD_ERR_CNT_SET		RSVD	WD_EN
R/W-01b		R/W-01b		R/W-01b		R-0b	R/W-0b

Table 9-23. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	01b	Watchdog configuration 00b = Autonomous 01b = Timeout 10b = Window 11b = Q&A
5-4	WD_PRE	R/W	01b	Watchdog prescalar 0b = Factor 1 1b = Factor 2 10b = Factor 3 11b = Factor 4
3-2	WD_ERR_CNT_SET	R/W	01b	Sets the watchdog event error counter that upon overflow the watchdog output will trigger 0b = Immediate trigger on each WD event 1b = Triggers on the fifth error event 10b = Triggers on the ninth error event 11b = Triggers on the 15th error event
1	RSVD	R	0b	Reserved
0	WD_EN	R/W	0b	Watchdog enable 0b = Disabled 1b = Enabled

9.5.6.8 WD_CONFIG_2 Register (Address = 14h) [reset = 02h]

WD_CONFIG_2 is shown in Figure 9-31 and described in Table 9-24.

Return to Summary Table.

Watchdog configuration setup 2

Figure 9-31. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				RSVD

Figure 9-31. WD_CONFIG_2 Register (continued)

R/W-000b	R/H-0001b	R-0b

Table 9-24. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	000b	Sets window or timeout times based upon the WD_PRE setting See WD_TIMER table
4-1	WD_ERR_CNT	R/H	0001b	Watchdog error counter Running count of errors up to 15 errors
0	RSVD	R	0b	Reserved

9.5.6.9 WD_INPUT_TRIG Register (Address = 15h) [reset = 00h]

WD_INPUT_TRIG is shown in Figure 9-32 and described in Table 9-25.

Return to Summary Table.

Writing FFh resets WD timer if accomplished at appropriate time

Figure 9-32. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
W1C-00h							

Table 9-25. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00h	Write FFh to trigger WD

9.5.6.10 WD_QA_CONFIG Register (Address = 2Dh) [reset = 0h]

WD_QA_CONFIG is shown in Figure 9-33 and described in Table 9-26.

Return to Summary Table.

Q&A watchdog configuration bits

Figure 9-33. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_Q&A_POLY_CFG		WD_Q&A_POLY_SEED			
R/W-00b		R/W-00b		R/W-0000b			

Note

Upon power up, WD_Q&A_POLY_SEED will read back 0000b, but the actual seed value is 101b. Once written to, the read back value and actual value will be the same.

Table 9-26. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_Q&A_POLY_CFG	R/W	00b	WD q&a polynomial configuration
3-0	WD_Q&A_POLY_SEED	R/W	0000b	WD q&a polynomial seed value loaded when device is in the RESET state

9.5.6.11 WD_QA_ANSWER Register (Address = 2Eh) [reset = 0h]

WD_QA_ANSWER is shown in Figure 9-34 and described in Table 9-27.

Return to Summary Table.

Q&A watchdog answer bits

Figure 9-34. WD_QA_ANSWER Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R-00h							

Table 9-27. WD_QA_ANSWER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W	00h	MCU watchdog q&a answer response byte

9.5.6.12 WD_QA_QUESTION Register (Address = 2Fh) [reset = 0h]

WD_QA_QUESTION is shown in Figure 9-35 and described in Table 9-28.

Return to Summary Table.

Q&A watchdog question bits

Figure 9-35. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0
RSVD	QA_ANSW_ERR	WD_ANSW_CNT		WD_QUESTION			
R-0b	W1C-0b	R-00b		R-0000b			

Table 9-28. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	QA_ANSW_ERR	W1C	0b	Watchdog q&a answer error flag
5-4	WD_ANSW_CNT	R	00b	Current state of received watchdog q&a error counter When WD enabled value will show up as 2'h3
3-0	WD_QUESTION	R	0000b	Current watchdog question value When WD is enabled value will show up as 4'hC

9.5.6.13 STATUS (address = 40h) [reset = 00h]

STATUS is shown in Table 9-29 and described in Table 9-30.

Return to Summary Table.

CAN transceiver status

Table 9-29. STATUS Register

7	6	5	4	3	2	1	0
STATUS_RSVD				CAN_ACTIVE	TSILENCE	RSVD	TXDDOM
R-0000b				R/U-0b	R/U-0b	R-0b	R/U-0b

Table 9-30. STATUS Register Field Description

Bit	Field	Type	Reset	Description
7-4	STATUS_RSVD	R	0000b	Reserved
3	CAN_ACTIVE	R/U	0b	CAN active mode 0b = No 1b = Yes
2	TSILENCE	R/U	0b	CAN bus in $t_{SILINCE}$ 0b = No 1b = Yes
1	RSVD	R	0b	Reserved

Table 9-30. STATUS Register Field Description (continued)

Bit	Field	Type	Reset	Description
0	TXDDOM	R/U	0b	TXD Low is preventing entering CAN Active mode 0b = No 1b = Yes

9.5.6.14 INT_GLOBAL Register (Address = 50h) [reset = 0h]

INT_GLOBAL is shown in Figure 9-36 and described in Table 9-31.

Return to Summary Table.

Logical OR of all to certain interrupts

Figure 9-36. INT_GLOBAL Register

7	6	5	4	3	2	1	0
GLOBALERR	INT_1	INT_2	INT_3	INT_CANBUS	RSVD		
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	R-0b		

Table 9-31. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBALERR	RH	0b	Logical OR of all interrupts
6	INT_1	RH	0b	Logical OR of INT_1 register
5	INT_2	RH	0b	Logical OR of INT_2 register
4	INT_3	RH	0b	Logical OR of INT_3 register
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2-0	RSVD	R	0b	Reserved

9.5.6.15 INT_1 Register (Address = 51h) [reset = 0h]

INT_1 is shown in Figure 9-37 and described in Table 9-32.

Return to Summary Table.

Interrupts

Figure 9-37. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT	LWU	WKERR	RSVD	CANSLNT	RSVD	CANDOM
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R-0b	R/W1C-0b

Table 9-32. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. NOTE: This interrupt bit will be set for every watchdog error event and does not reliy upon the Watchdog error counter
6	CANINT	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	WKERR	R/W1C	0b	Wake error bit is set when the SWE timer has expired and the state machine has returned to Sleep mode
3	RSVD	R	0b	Reserved
2	CANSLNT	R/W1C	0b	CAN silent
1	RSVD	R	0b	Reserved
0	CANDOM	R/W1C	0b	CAN bus stuck dominant

9.5.6.16 INT_2 Register (Address = 52h) [reset = 40h]

INT_2 is shown in Figure 9-38 and described in Table 9-33.

Return to Summary Table.

Interrupts

Figure 9-38. INT_2 Register

7	6	5	4	3	2	1	0
RSVD	PWRON	OVCCOUT	UVSUP	RSVD	UVCCOUT	TSD	TSDW
R-0b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-33. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved
6	PWRON	R/W1C	1b	Power on
5	OVCCOUT	R/W1C	0b	V_{CCOUT} overvoltage
4	UVSUP	R/W1C	0b	V_{SUP} undervoltage
3	RSVD	R	0b	Reserved
2	UVCCOUT	R/W1C	0b	V_{CCOUT} undervoltage
1	TSD	R/W1C	0b	Thermal Shutdown
0	TSDW	R/W1C	0b	Thermal Shutdown Warning

9.5.6.17 INT_3 Register (Address 53h) [reset = 0h]

INT_3 is shown in Figure 9-39 and described in Table 9-34.

Return to Summary Table.

Figure 9-39. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	RSVD						
R/W1C-0b	R-00h						

Table 9-34. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6-0	RSVD	R	00h	Reserved

9.5.6.18 INT_CANBUS Register (Address = 54h) [reset = 0h]

INT_CANBUS is shown in Figure 9-40 and described in Table 9-35.

Return to Summary Table.

CAN bus faults that include shorts and opens

Figure 9-40. INT_CANBUS Register

7	6	5	4	3	2	1	0
RESERVED		CANHCANL	CANHBAT	CANLGND	CANBUSOPEN	CANBUSGND	CANBUSBAT
R-0b		R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-35. INT_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0b	Reserved. Reads return 0.
5	CANHCANL	R/W1C	0b	CANH and CANL shorted together

Table 9-35. INT_CANBUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CANHBAT	R/W1C	0b	CANH shorted to Vbat
3	CANLGND	R/W1C	0b	CANL shorted to GND
2	CANBUSOPEN	R/W1C	0b	CAN bus open
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

9.5.6.19 INT_ENABLE_1 Register (Address = 56h) [reset = F3h]

INT_ENABLE_1 is shown in Figure 9-41 and described in Table 9-36.

Return to Summary Table.

Interrupt mask for INT_1

Figure 9-41. INT_ENABLE_1 Register

7	6	5	4	3	2	1	0
WD_ENABLE	CANINT_ENABLE	LWU_ENABLE	WKERR_ENABLE	RSVD	CANSLNT_ENABLE	RSVD	CANDOM_ENABLE
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-1b	R-0b	R/W-1b

Table 9-36. INT_ENABLE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_ENABLE	R/W	1b	Watchdog event interrupt enable
6	CANINT_ENABLE	R/W	1b	CAN bus wake up interrupt enable
5	LWU_ENABLE	R/W	1b	Local wake up enable
4	WKERR_ENABLE	R/W	1b	Wake error enable
3	RSVD	R	0b	Reserved
2	CANSLNT_ENABLE	R/W	1b	CAN silent enable
1	RSVD	R	0b	Reserved
0	CANDOM_ENABLE	R/W	1b	CAN bus stuck dominant enable

9.5.6.20 INT_ENABLE_2 Register (Address = 57h) [reset = 3Fh]

INT_ENABLE_2 is shown in Figure 9-42 and described in Table 9-37.

Return to Summary Table.

Interrupt mask for INT_2

Figure 9-42. INT_ENABLE_2 Register

7	6	5	4	3	2	1	0
RSVD		OVCC_ENABLE	UVSUP_ENABLE	RSVD	UVCC_ENABLE	TSD_ENABLE	TSDW_ENABLE
R-0b		R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b

Table 9-37. INT_ENABLE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSVD	R	0b	Reserved
5	OVCC_ENABLE	R/W	1b	V_{CC} over voltage enable
4	UVSUP_ENABLE	R/W	1b	V_{SUP} undervoltage enable
3	RSVD	R	0b	Reserved
2	UVCC_ENABLE	R/W	1b	V_{CC} undervoltage enable
1	TSD_ENABLE	R/W	1b	Thermal shutdown enable

Table 9-37. INT_ENABLE_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSDW_ENABLE	R/W	1b	Thermal shutdown warning enable

9.5.6.21 INT_ENABLE_3 Register (Address =58h) [reset = 80h]

INT_ENABLE_3 is shown in Figure 9-43 and described in Table 9-38.

Return to Summary Table.

Interrupt mask for INT_3

Figure 9-43. INT_ENABLE_3 Register

7	6	5	4	3	2	1	0
SPIERR_ENABLE	RSVD						
R/W-1b	R-00h						

Table 9-38. INT_ENABLE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_ENABLE	R/W	1b	SPI error interrupt enable
6-0	RSVD	R	00h	Reserved

9.5.6.22 INT_ENABLE_CANBUS Register (Address = 59h) [reset = 7Fh]

INT_ENABLE_CANBUS is shown in Figure 9-44 and described in Table 9-39.

Return to Summary Table.

Interrupt mask for INT_CANBUS

Figure 9-44. INT_ENABLE_CANBUS Register

7	6	5	4	3	2	1	0
RESERVED		CANHCANL_ENABLE	CANHBAT_ENABLE	CANLGND_ENABLE	CANBUSOPEN_ENABLE	CANBUSGND_ENABLE	CANBUSBAT_ENABLE
R-0b		R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 9-39. INT_ENABLE_CANBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0b	Reserved
5	CANHCANL_ENABLE	R/W	1b	CANH and CANL shorted together enable
4	CANHBAT_ENABLE	R/W	1b	CANH shorted to Vbat enable
3	CANLGND_ENABLE	R/W	1b	CANL shorted to GND enable
2	CANBUSOPEN_ENABLE	R/W	1b	CAN bus open enable
1	CANBUSGND_ENABLE	R/W	1b	CAN bus shorted to GND enable
0	CANBUSBAT_ENABLE	R/W	1b	CAN bus shorted to Vbat enable

9.5.6.23 INT_RSVD_y Register (Address = 5Ah + formula) [reset = 00h]

INT_RSVD_y is shown in Figure 9-45 and described in Table 9-40.

Return to Summary Table.

Register address 5Ah through 5Fh

Offset = 5Ah + (y * 1h); where y = 0h to 7h

Figure 9-45. INT_RSVD_y Register

7	6	5	4	3	2	1	0

Figure 9-45. INT_RSVD_y Register (continued)

RESERVED
R-00h

Table 9-40. INT_RSVD_y Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	00h	Reserved

10 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.2 Typical Application

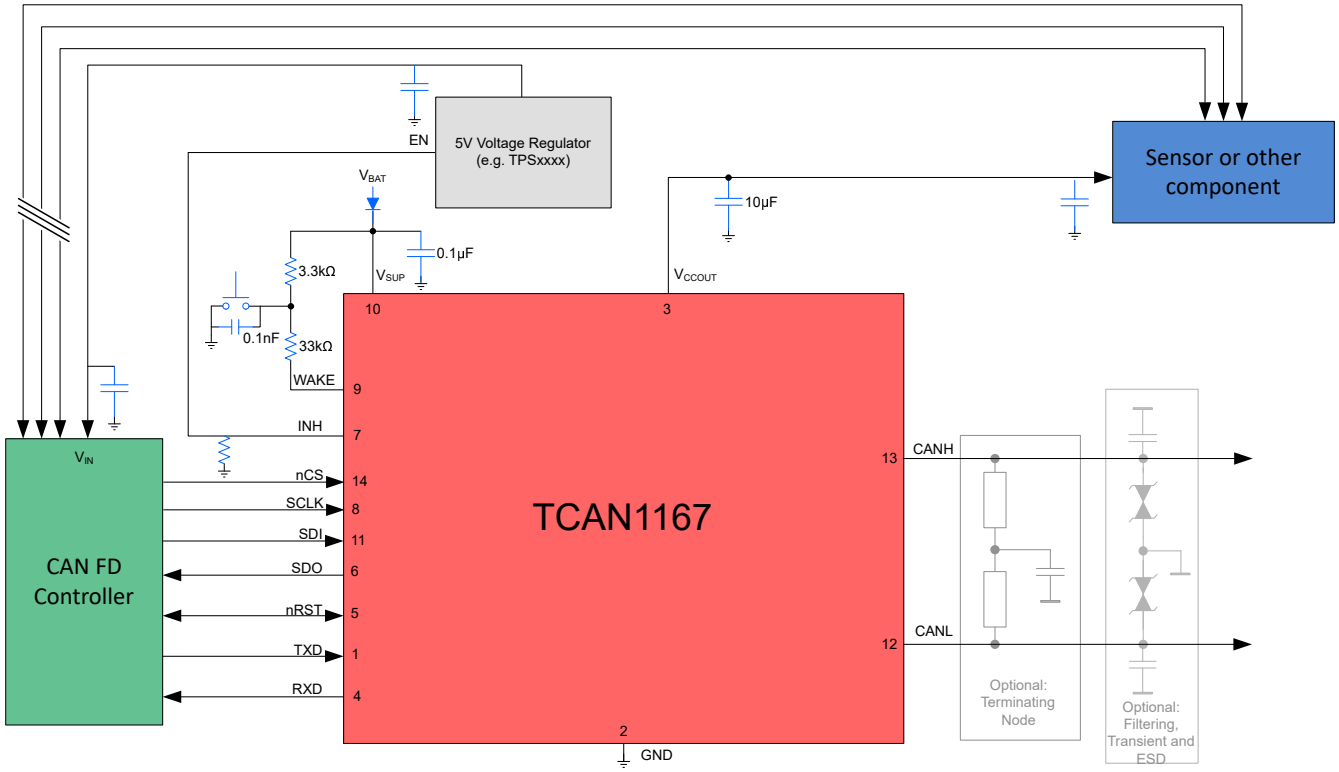


Figure 10-1. Typical Application

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1167-Q1

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1167-Q1 is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1167-Q1 is a minimum of 40 kΩ. If 100 TCAN1167-Q1 devices are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately

52 Ω. Therefore, the TCAN1167-Q1 theoretically supports over 100 devices on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Termination

Termination may be a single 120-Ω resistor at the end of the bus on either the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired then split termination may used, see Figure 10-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines..

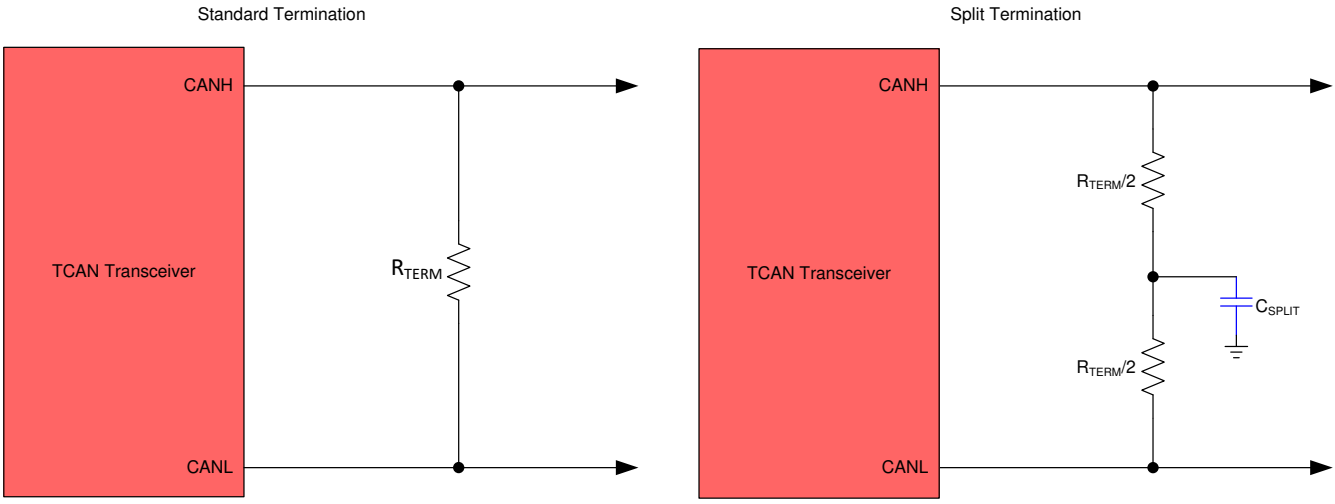
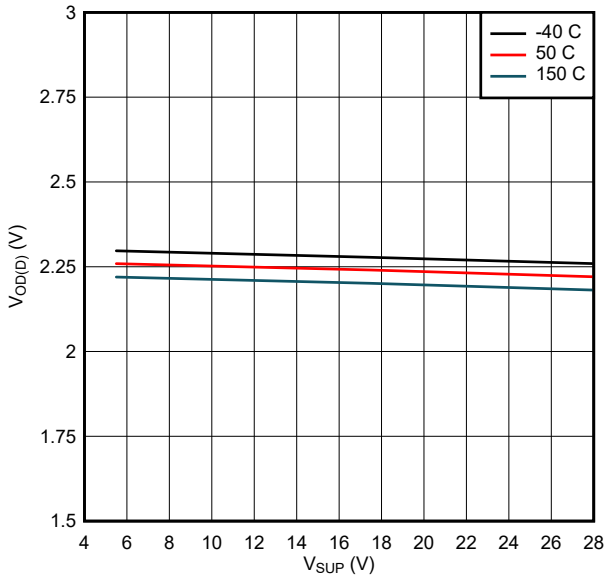


Figure 10-2. CAN Bus Termination Concepts

10.3 Application Curves



R_L = 60 Ω

Figure 10-3. $V_{OD(D)}$ over V_{SUP}

11 Power Supply Requirements

The TCAN1167-Q1 is designed to operate from a V_{SUP} input supply voltage range between 5.5 V and 28 V. Input supplies must be well regulated. A bypass capacitance, typically 100 nF, should be placed close to the device V_{SUP} supply pin. This helps to reduce supply voltage ripple present on the outputs of the switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes and traces.

12 Layout

12.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device itself. Transient voltage suppression (TVS) device can be added for extra protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

A high-frequency current follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors with the center or split tap of the termination connected to ground via capacitor. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination.

12.2 Layout Example

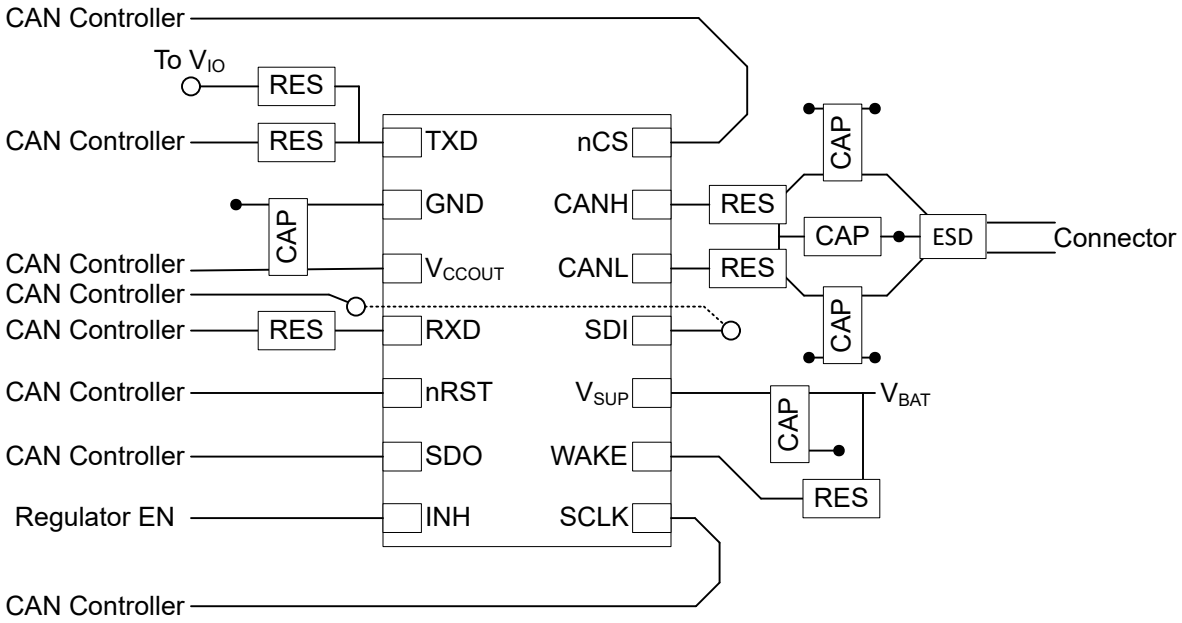


Figure 12-1. TCAN1167 Example Layout

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 Documentation Support

13.1.1 Related Documentation

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1167DMTRQ1	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-45 to 150	1167	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

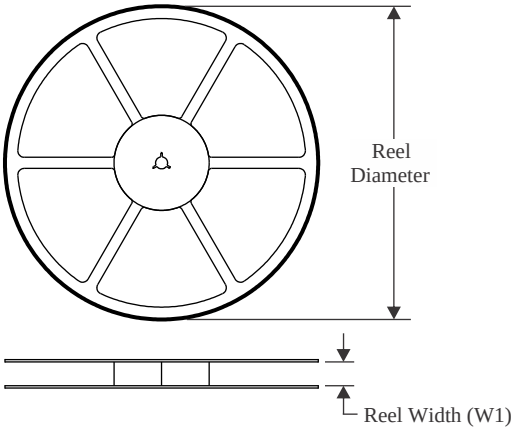
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

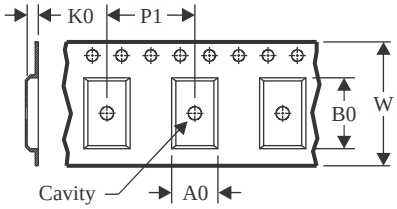
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

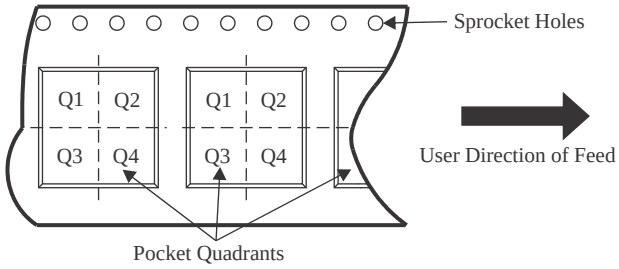


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

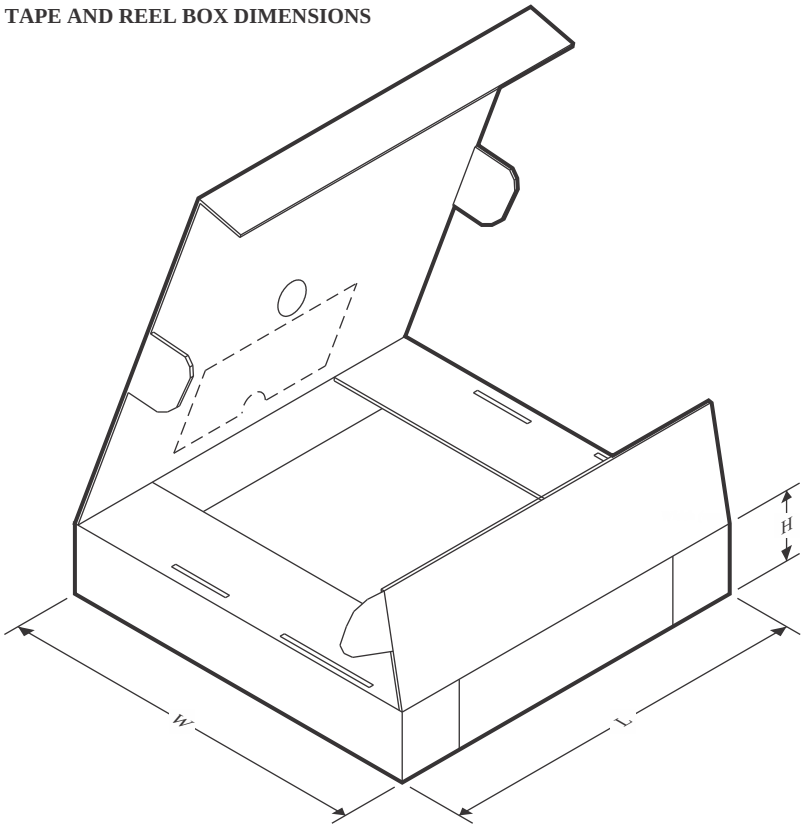
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1167DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1167DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

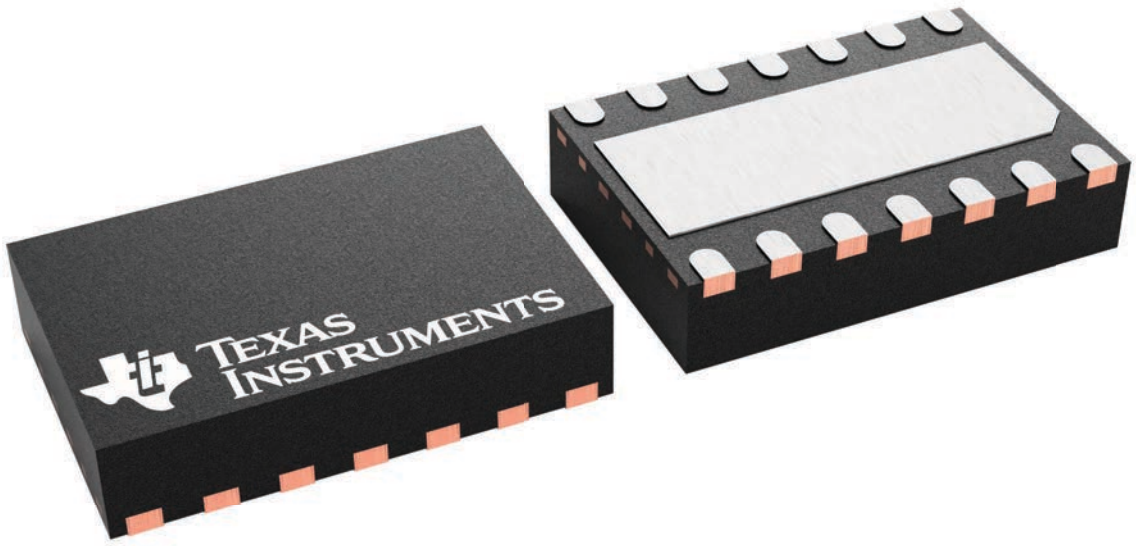
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



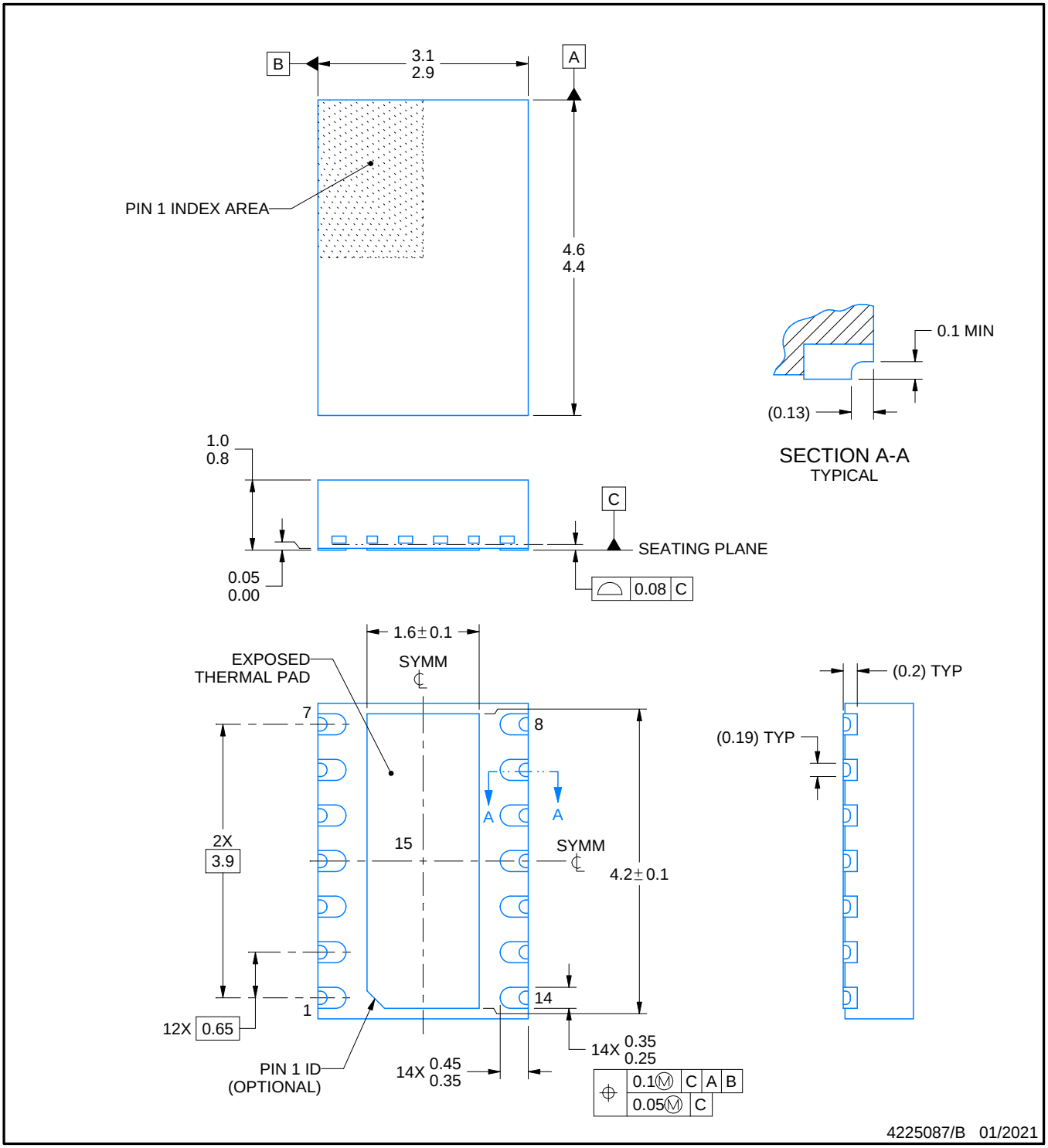
4225088/A

DMT0014B

PACKAGE OUTLINE

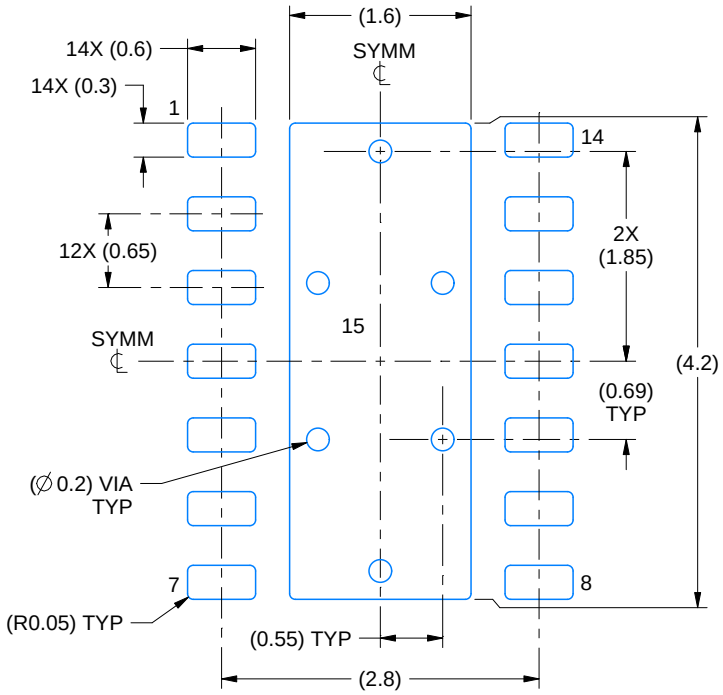
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

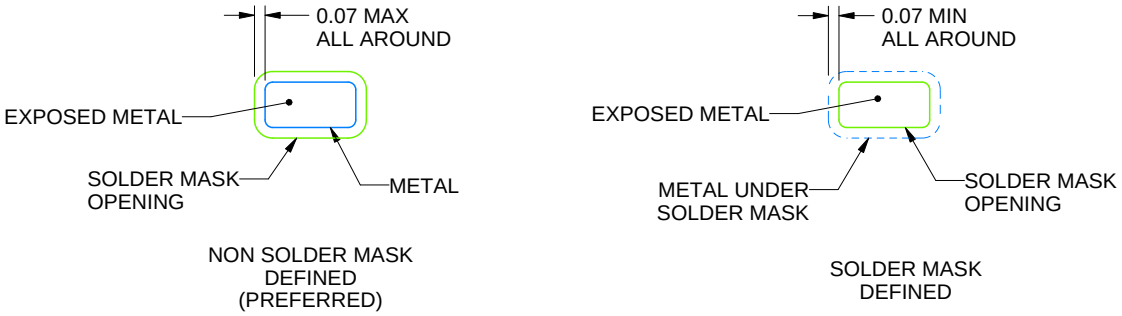


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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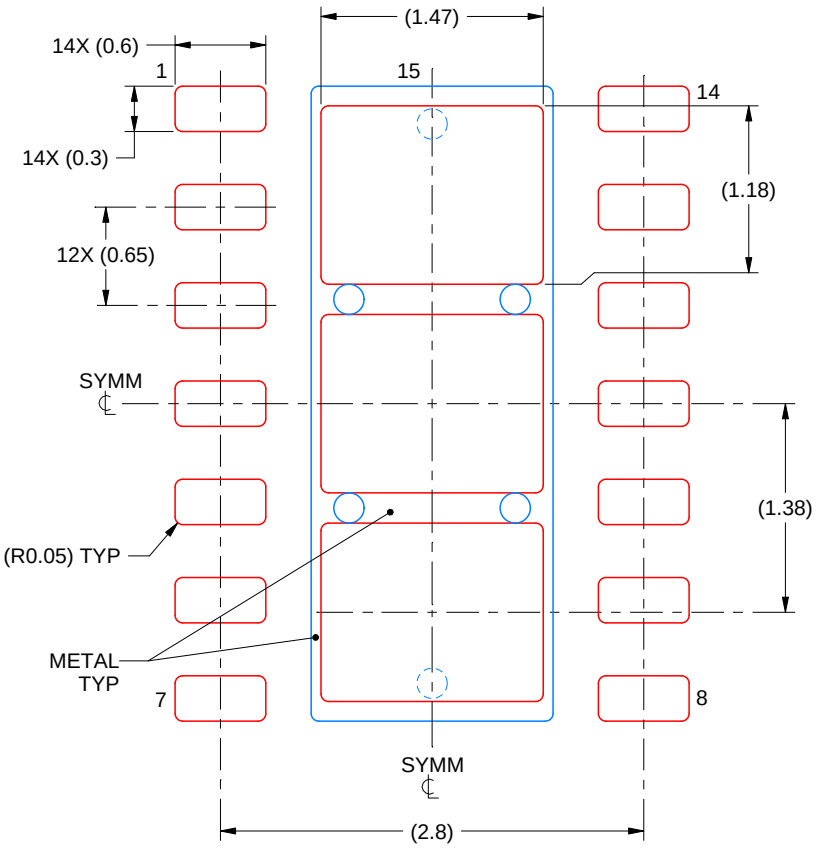
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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