Technical White Paper

RS-485 Basics Series

Kankan Wang, Hao Liu *Transceiver Interface*

1 Introduction

Since its definition in 1983, RS-485 has become the preferred interface standard for many industrial fieldbus applications. This article is intended to provide a useful, informative, and centralized resource for understanding the fundamentals of RS-485 and addressing common application questions that arise when designing RS-485 networks.

RS-485, formally known as American National Standards Institute (ANSI) Telecommunications Industry Association (TIA)/Electronic Industries Alliance (EIA)-485-A, is a balanced data transmission standard for serial communication. RS-485 allows for robust transmission of moderate data rates over long distances in multipoint communication applications, such as factory and building automation, motor control, and other field bus applications.

The RS-485 standard only specifies the electrical characteristics of drivers and receivers; it does not specify a protocol. Many higher-level interface standards reference RS-485 for their physical layer, such as Modicon bus (ModBus), process field bus (ProfiBus), DMX512, and others.

Figure 1-1 illustrates some common interface standards. RS-485 improves noise immunity and extends the distance supported by RS-232 by implementing a differential, rather than single-ended, signaling technique. And while electrically similar, RS-485 extends RS-422 to allow for bidirectional communication.

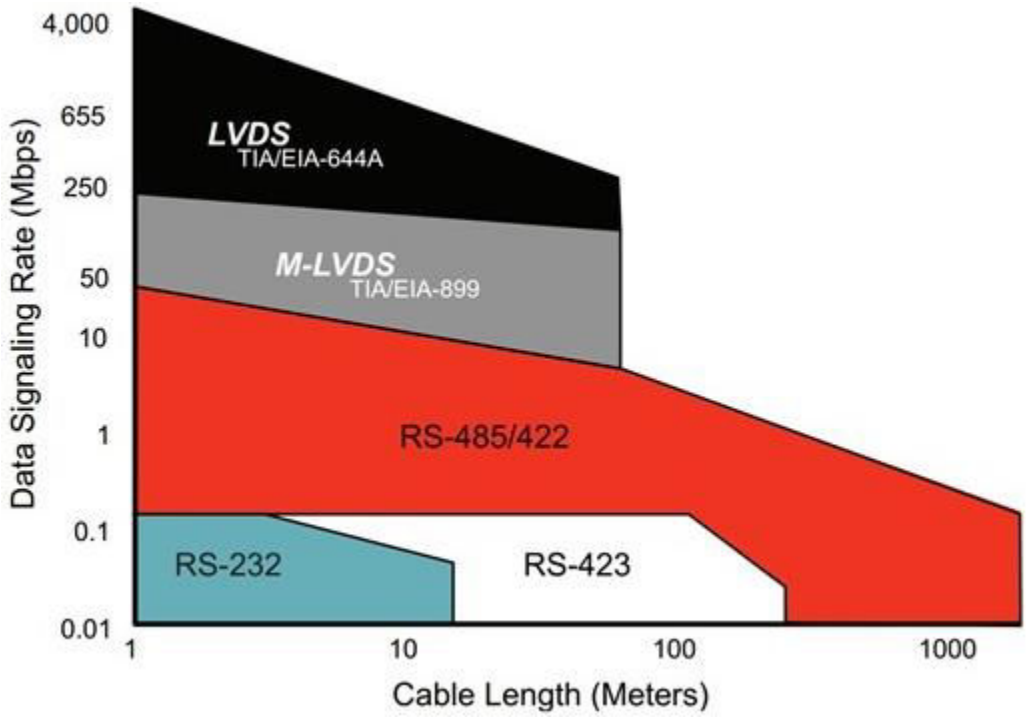

Figure 1-1. Common Interface Standards

Additionally, RS-485 allows for communication over greater distances than multipoint low-voltage differential signaling (M-LVDS) because of its larger signaling levels and wider common-mode range. However, for data rates higher than 50 megabits per second, M-LVDS becomes increasingly advantageous for its reduced power consumption relative to RS-485.

RS-485 networks consist of multiple nodes connected in parallel to a bus. Figure 1-2 shows the typical network connections for half- and full-duplex RS-485 implementations. The majority of RS-485 applications implement half-duplex (two-wire) communication. Full-duplex communication requires two signal pairs (four-wire), and facilitates higher throughput by allowing nodes to transmit and receive data simultaneously. Modern transceiver designs allow hundreds of nodes to connect to the bus.

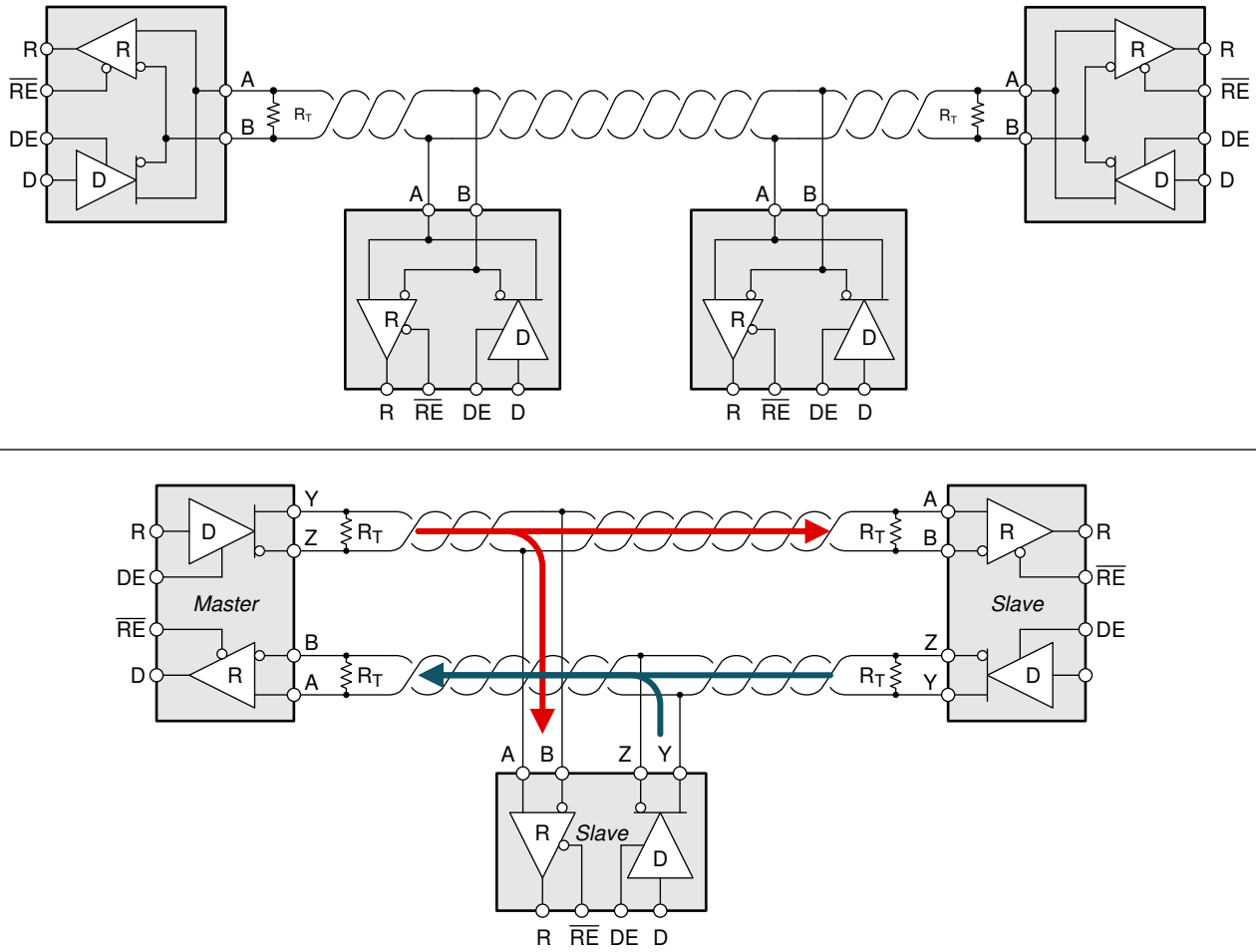

Figure 1-2. Half- and Full-Duplex RS-485 Network Connections

Section 2 and Section 4, respectively, discuss the basic design and operation of the RS-485 driver and receiver. This document also covers receiver failsafe operation, transceiver power dissipation, transient protection, and more.

2 The RS-485 Driver

Many common RS-485 questions can be resolved with a basic understanding of the structure and operation of the driver and receiver. This section discusses the RS-485 driver and the relevant specifications in the RS-485 standard.

Figure 2-1 shows the equivalent output schematic for the driver of the THVD1550 half-duplex transceiver from TI. The output structure consists of an H-bridge driver with high- and low-side transistors on each of the A and B outputs, which are in parallel with electrostatic discharge (ESD) cells on each terminal. The diodes in-series with each transistor prevent reverse current flow from the bus terminals to the power supply if the voltage on A or B is greater than VCC, or from ground to the bus terminals if the voltage on A or B is below the ground potential.

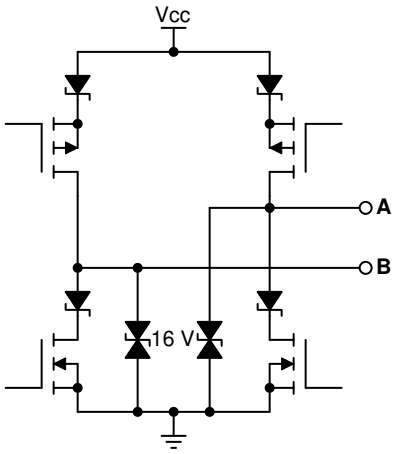

Figure 2-1. Differential Output Driver Structure

Figure 2-2 shows that the basic operation of the driver simplifies to the high- and low-output logic states.

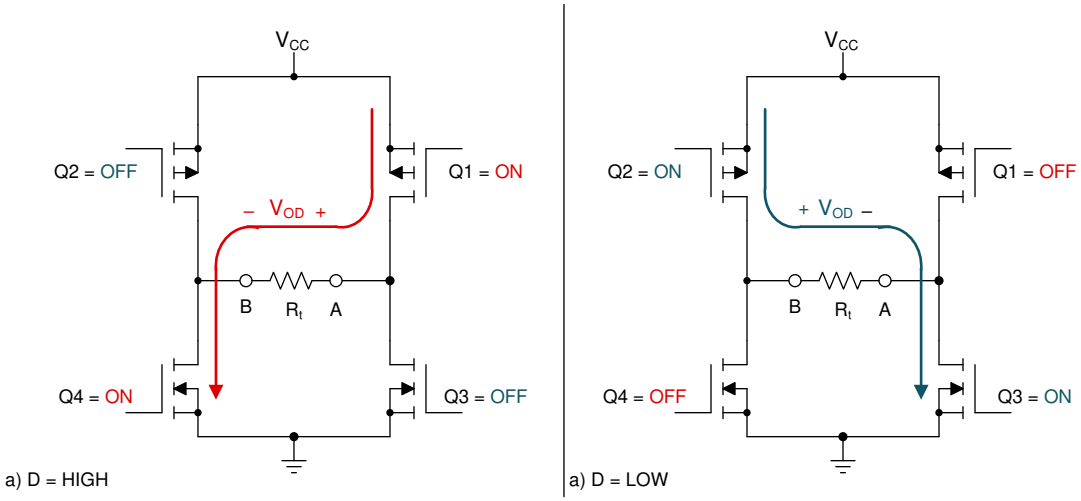

Figure 2-2. RS-485 Output Driver Operation

The resulting waveform can be modeled as a positive and negative differential voltage superimposed onto a common-mode offset voltage, which is typically close to VCC/2, as Figure 2-3 shows.

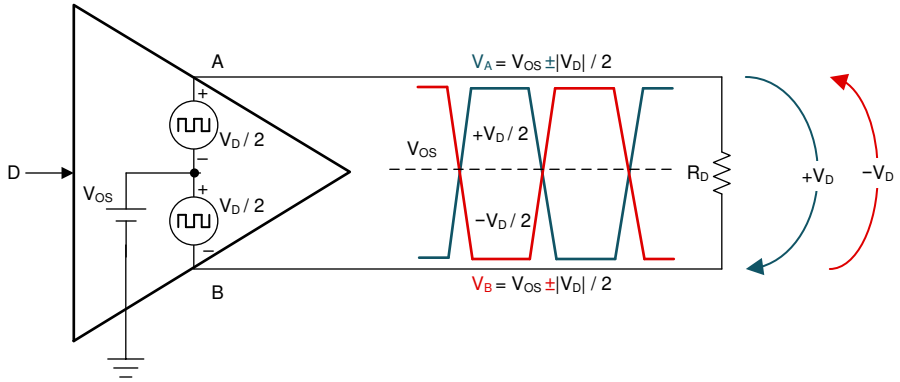

Figure 2-3. RS-485 Driver Output Waveform

The RS-485 standard specifies that a compliant driver must produce a differential output voltage greater than 1.5 V with a 54-Ω load. Figure 2-4 illustrates the relevant RS-485 test circuit.

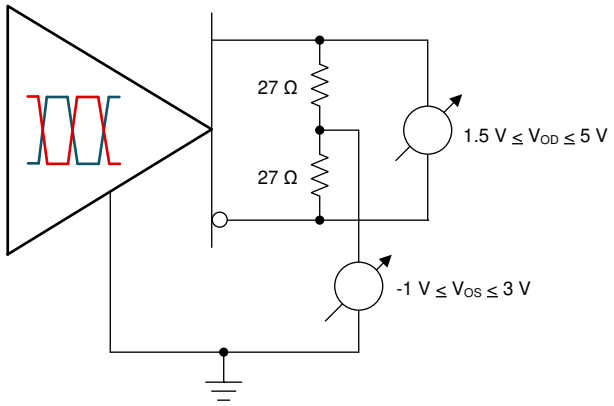

Figure 2-4. RS-485 Output Driver Test Circuit

Therefore, the on-resistance of the high- and low-side transistors must be low enough to source sufficient current to produce 1.5 V across 54 Ω. A common guideline is to assume a typical on-resistance of between 20 Ω and 30 Ω for each transistor.

Additionally, the RS-485 standard also requires that a compliant driver produce a differential output voltage greater than 1.5 V with a 60-Ω differential load and common-mode load of 375 Ω from each of the A and B outputs to –7 V to 12 V. Figure 2-5 provides an example.

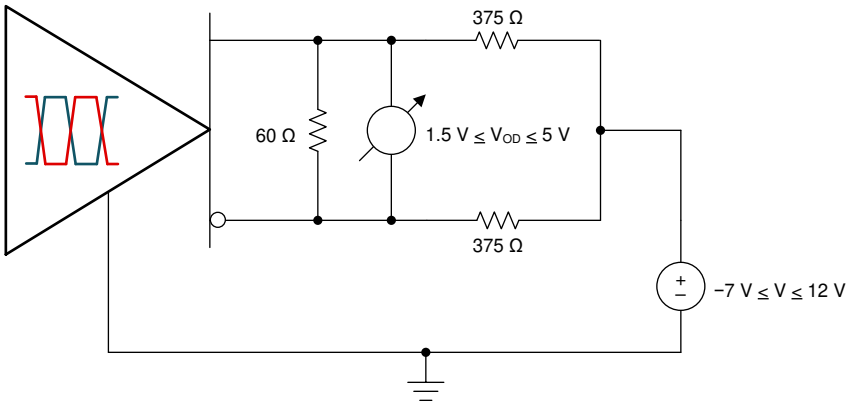

Figure 2-5. RS-485 Output Driver Test Circuit Over Common-Mode

Further, the on-resistance of each leg of the H-bridge output must be well-matched (that is, Q1 ≈ Q2, and Q3 ≈ Q4). The RS-485 standard specifies that the difference in magnitude of V_{OD} when the output is positive and V_{OD} when the output is negative must be less than 200 mV. When each leg of the H-bridge output is perfectly matched, this value, denoted as $\Delta|V_{OD}|$ in the data sheet, is zero. For the THVD2450, $\Delta|V_{OD}|$ has a maximum value of 50 mV. Large imbalances in V_{OD} for different logic states result in increased common-mode noise and higher levels of radiated electromagnetic interference (EMI).

A final important characteristic of any RS-485 driver is its output rise and fall time, which is determined by a separate circuit that controls the switching of transistors Q1, Q2, Q3, and Q4 (see Figure 2-2). The output rise and fall time limits the maximum data rate at which the transceiver can operate. Typically, the rise and fall time of the driver should be no more than one-third the total bit time at a given data rate. Further, for a given data rate, a transceiver with slower rise and fall times is preferable to a transceiver with faster rise and fall times, as it will radiate less electromagnetic interference (EMI) into adjacent circuitry.

Large differential output voltage and wide common-mode range differentiate RS-485 from other signaling standards and make it suitable for use in noisy electrical environments and applications, such as industrial automation, e-metering, and motor control.

3 How to Calculate Unit Loads and the Maximum Number of Nodes on the Network

Figure 3-1 illustrates that the RS-485 is a multipoint differential bus. This means that all of the nodes on the bus share one common transmission medium, and therefore every node placed onto the bus adds a load in parallel to all of the existing network transceivers and termination resistors. As the total number of nodes increases, the loading on each and every driver increases as well.

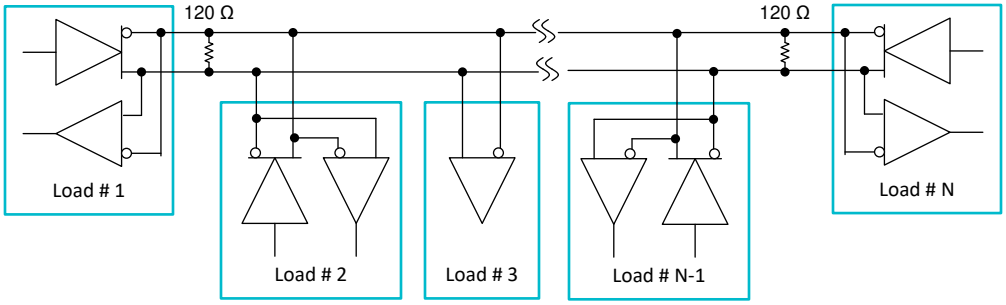

Figure 3-1. Multipoint RS-485 bus

To set practical and measurable limits for RS-485 output drivers, the Telecommunications Industry Association (TIA)/Electronic Industries Alliance (EIA)-485 standard created a hypothetical “unit load,” and then limited the maximum number of unit loads that can be presented to any driver on an RS-485 bus to 32. The standard states that a driver must be able to drive a minimum 1.5 differential signal across a maximum of 32 unit loads in parallel with two 120-Ω termination resistors.

Determine the unit-load parameter by sweeping the input voltage from –7 to 12 V on one bus pin, with the other bus pin held at ground, and then measuring the input leakage current. Measure both bus pins individually, with the transceiver both in a powered and unpowered state. As expected, the input leakage current depends on the input voltage; thus, when calculating the unit load, Equation 1 uses the worst-case ratio of input voltage to leakage current:

$$\text{Unit Load} = \text{Max}\left[\frac{V_{IN}}{\text{iLeakage}}\right] \tag{1}$$

where

- V_{IN} {–7 … + 12 V}

In Figure 3-2, the bounds of –7 and 12 V in the standard are meant to allow up to ±7 V of ground-potential difference (GPD) between a driver output and a receiver, with the output voltage of the driver varying between GND and 5 V. Therefore, –7 V represents a receiver noting a respective driver pin driving the bus low with a –7-V GPD, while 12 V represents a receiver noting a respective driver pin driving the bus high with a 7-V GPD.

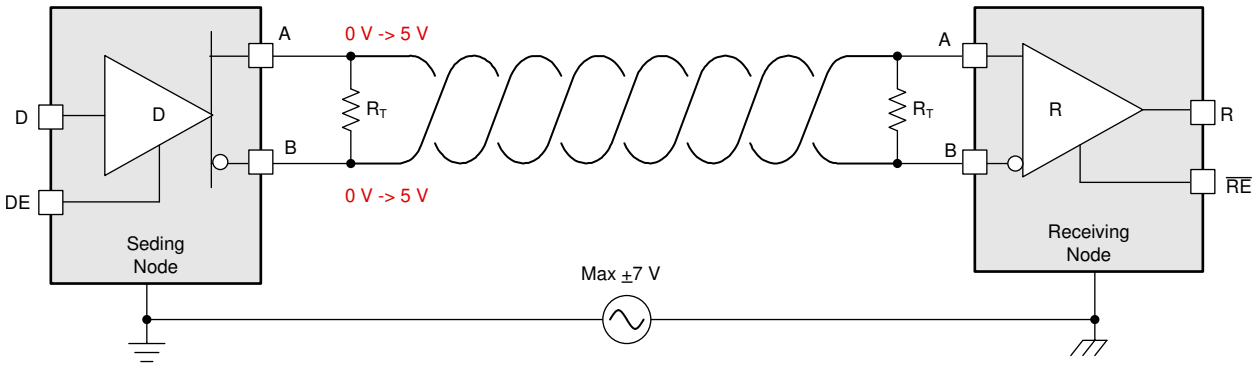

Figure 3-2. Maximum GPD of a Standard RS-485 Transceiver

One unit load is equivalent to 1 mA of input leakage current at 12 V. This load represents a single-ended load with respect to ground. Another easy way to think of the unit load is the equivalent of a 12-kΩ resistance from either the A or B bus pins (and the Y and Z pins for full-duplex transceivers) to ground.

Once the maximum ratio of input voltage to leakage current is determined, the equivalent unit load can be calculated by dividing that ratio by 12 kΩ, expressing the result in terms of a fraction of the unit load.

Using this unit-load ratio, the maximum number of any variety of transceivers that the network can handle can be calculated. For example, when considering the THVD1520 RS-485 transceiver, which has a one-eighth unit-load input impedance, you would be able to place a theoretical maximum of 256 nodes on the network, as shown in Equation 2:

$$\#\ \text{of Nodes} = \frac{32}{\text{Equivalent Unit Loading}} = \frac{32}{1/8} = 256\ \text{Nodes} \tag{2}$$

Table 3-1 shows the relationship between unit load, bus leakage current, equivalent input resistance, and the maximum number of devices that can be on the network for a few typical unit loads.

Table 3-1. Unit-Load Characteristics

Unit Load	Bus Leakage Current at 12 V	Equivalent Input Resistance	Maximum Nodes on One Network
1	1 mA	12 kΩ	32
1/2	500 µA	24 kΩ	64
1/4	250 µA	48 kΩ	128
1/8	125 µA	96 kΩ	256

Recall from Section 2, the common-mode load for an RS-485 driver-output test circuit is 375 Ω; see Figure 3-3. This is because it is the equivalent of 32 unit loads (12 kΩ) in parallel.

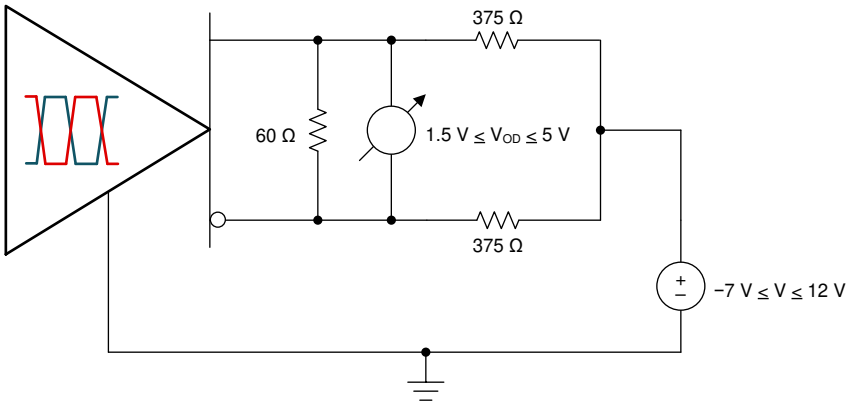

Figure 3-3. RS-485 Driver-Output Test Circuit With Common-Mode Load

Moreover, if you are trying to figure out how many transceivers you can place on your network, this data sheet will have a unit-load parameter or a maximum input leakage current that can be used for calculating the unit load. The smaller the unit load, the more devices you can place onto the network.

4 The RS-485 Receiver

This section discusses the RS-485 receiver and the relevant parameters in the RS-485 standard.

RS-485 transceivers such as the THVD1429 half-duplex family have an equivalent receiver input schematic like the one shown in Figure 4-1. The receiver input circuitry consists of electro-static discharge (ESD) protection, a resistor-divider network, and a biasing current, all of which play a role in shaping the magnitude and common-mode voltage that reaches the differential comparator.

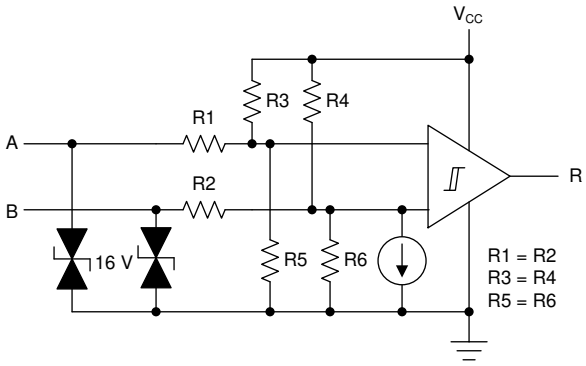

Figure 4-1. Differential Receiver Input Structure

ESD protection

The most important thing to note in terms of ESD protection for half-duplex transceivers is that the driver and receiver share the same ESD protection, saving space. But for a full-duplex transceiver, both the driver (Y and Z pins) and receiver (A and B pins) need independent ESD protection. This means that twice the area is needed to support ESD protection.

Resistor-divider network

The resistor-divider network on the A and B inputs serves two functions. The first function is to attenuate large signals that are beyond the range of the supply voltage of the receiver. This attenuation factor is necessary because the RS-485 standard states that voltages as low as –7 V and as high as 12 V can exist on the bus terminals to account for ground-potential differences that may exist between transceivers on a shared network. These high voltages need attenuation down to voltages that 3.3 V or 5 V transceivers can handle. A typical attenuation factor is on the order of 10-to-1, greatly reducing the magnitude of the voltages seen internally at the comparator.

The second important function of the resistor-divider network is to bias the bus voltages toward VCC/2. This is necessary because simply attenuating a negative signal will not bring the voltage between the local ground of the receiver and VCC. Attenuating the signal and biasing it toward VCC/2 prevents the inputs of the comparator from getting saturated; thus enabling the comparator to properly evaluate the differential voltage between the A and B terminals.

This ability to bias the voltages also allows the system to perform without a common ground connection between the remote ground of the RS-485 driver and the ground of the local RS-485 receiver. Figure 4-2 shows how an input signal is both attenuated and biased from the bus terminals to the input of the comparator through the resistor-divider network.

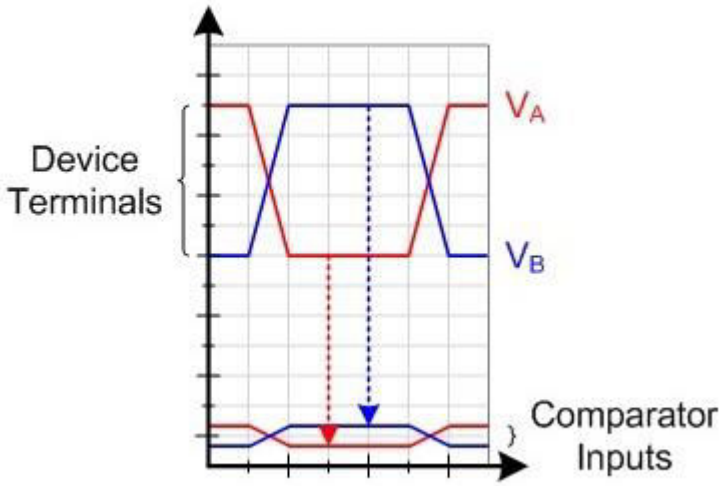

Figure 4-2. Receiver Input-Voltage Attenuation

The series combination of R1 and R3 || R5 (resistors R3 and R5 in parallel) is the primary factor that determines the input impedance of the receiver. The RS-485 standard specifies that the input leakage current of a compliant receiver must remain within the shaded region shown in Figure 4-3 when applying –7 V to 12 V to the input terminals for both powered and unpowered conditions.

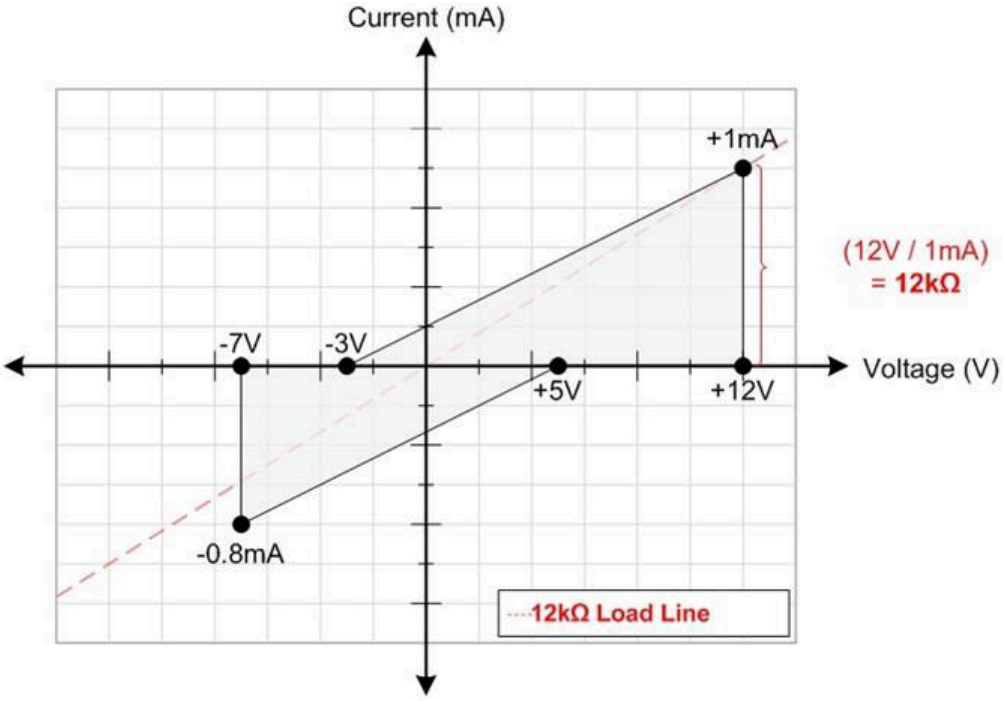

Figure 4-3. RS-485 Receiver Input I-V Characteristic

The trade-off that exists with receiver attenuator design is that in order to lower the leakage current, higher resistor values must be used, which increases the size of the resistors in the attenuator. Larger-sized components create a more expensive die and more parasitic capacitance. This stray capacitance and the input capacitance of the comparator sit in parallel to the resistance of the attenuator, creating a low-pass filter, which in turn limits the maximum bandwidth of the receiver. Therefore, there is a balance between the input leakage current and resistor values and the bandwidth and size of the attenuator. With the THVD1450 device, the highest-speed device in the THVD14xx family, it is apparent that it also has the highest bus input-leakage current due to the lower resistor-value attenuator circuit that was needed.

Biasing Current

Figure 4-4 shows the effect of the current source connected between the B input terminal of the comparator and ground. By using the superposition principle, it is evident that the current source will cause a voltage drop across R4 and R6 connected to the negative-input terminal of the comparator. This creates a fail-safe bias voltage that causes the negative terminal to have a lower voltage than the positive terminal and the output of the comparator to be in a known high state when applying a 0-V differential voltage to the A and B pins.

This fail-safe biasing helps ensure that the R output will be high in the presence of bus idle or bus short-circuit conditions. In the VIT numbers for the THVD1451 family, the positive threshold has a typical value of –100 mV and the negative threshold is typically –130 mV. Without fail-safe biasing, transceiver thresholds would be centered around 0 V and in an indeterminate state with a 0-V differential input voltage.

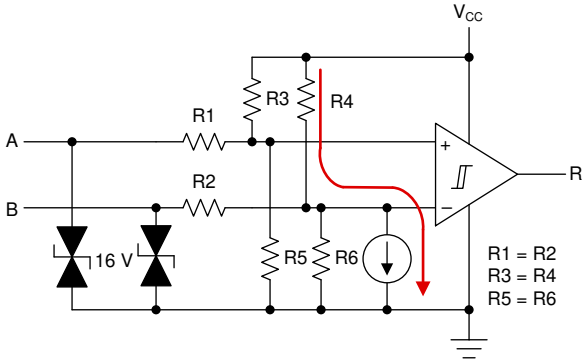

Figure 4-4. Effect of the Offset Bias Current

In summary, understanding the basic input structures of an RS-485 receiver helps recognize important receiver electrical specifications like input-leakage current and positive and negative input thresholds.

5 Two Methods to Fail-Safe Bias the Network

This section explores two common methods for handling idle bus conditions so a logical state on the bus is ensured.

Because RS-485 is a multipoint topology network and is not able to handle contention, there will be times where all RS-485 transceivers on the bus are presenting high impedance and no logical state is being actively driven. Most commonly, this will occur between when one node finishes transmitting a message and the next node begins transmitting a message. During these times, the bus will have a 0-V differential signal due to the installed termination resistors. Per the Electronic Industries Alliance (EIA)-485 standard, the input thresholds of an RS-485 receiver are logically high for differential voltages ≥ +200 mV and logically low for differential voltages ≤ –200 mV. This means that there is a 400-mV indeterminate state for differential input voltages, as shown in Figure 5-1.

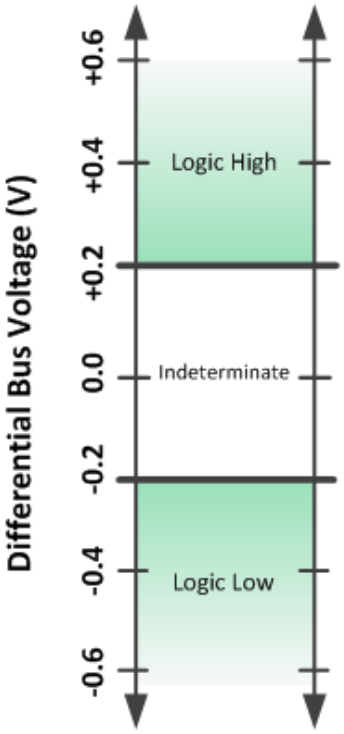

Figure 5-1. RS-485 Receiver Input Thresholds

The two most common methods of handling this indeterminate state are to either select receivers that have built-in fail-safe input thresholds or use additional external resistors to create an external bias on the idle bus. Both methods ensure a logical high state on the bus, which corresponds to a positive differential voltage.

Section 4 discussed how to achieve a built-in fail-safe input bias. The quick explanation is that an internal bias current created inside the attenuation network then creates a voltage difference at the input of the comparator of the receiver. The benefit of this solution is that it has no effect on the loading of all of the transceivers on the network. The caveat is that every single node on the network must have this feature built-in. For existing installations, or installations using previously designed modules that may be hard to update, this may not be a realistic option.

The second way to handle idle bus conditions is to use two external resistors: one from the A terminal to VCC and the other from B terminal to ground. See the two red resistors in Figure 5-2.

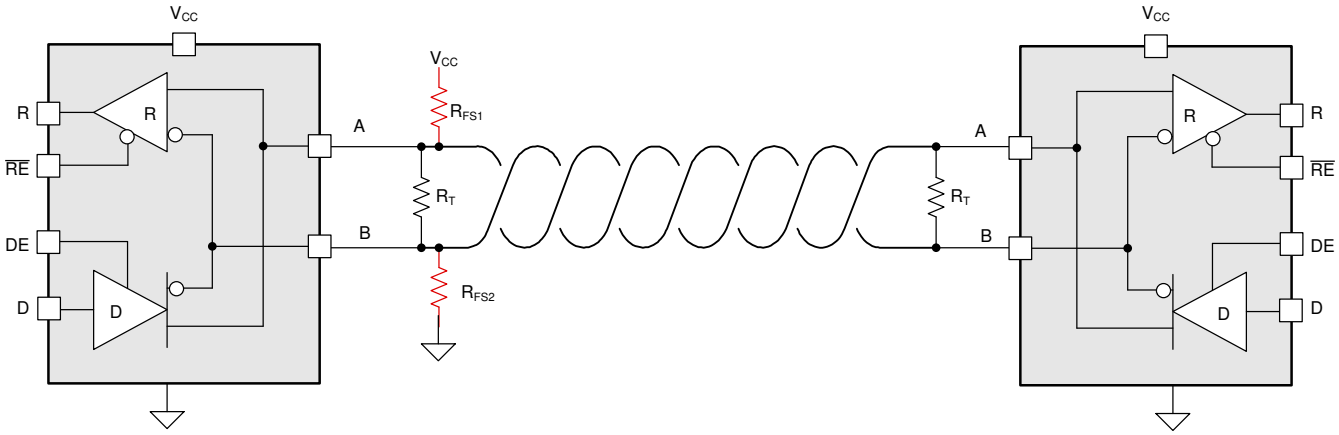

Figure 5-2. Fail-Safe Resistor Placement

As R_{FS1} shows, the two parallel termination resistors (R_T) and (R_{FS2}) create a simple voltage divider circuit. The resistors only need to be installed in one node on the entire network, typically on the leader node. Additionally, R_{FS1} and R_{FS2} are set equal to each other so that the common mode is balanced between VCC and ground.

Equation 3 is the simplest way to calculate the value of these fail-safe resistors. Take the minimum input voltage that results in a known state (200 mV), the equivalent termination resistors in parallel (60 Ω) and the minimum VCC for the node that will have the fail-safe resistors populated (use 4.5 V) and solve the simple voltage-divider equation:

$$V_{FS} = V_{CC,min}\left(\frac{Req}{R_{FS1} + R_{eq} + R_{FS2}}\right) \tag{3}$$

Substituting V_{FS} = 200 mV, R_{eq} = 60 Ω and setting $R_{FS1} + R_{FS2} = 2 \times R_{FS}$ (since they are set equal to each other), provides:

$$0.2 = 4.5 \times \left(\frac{60}{2 \times R_{FS} + 60}\right) >> R_{FS} = 645\ \Omega \tag{4}$$

This shows that the benefit to this solution only takes two resistors to accomplish, and it works for all nodes on a network. The caveat is that the two 645-Ω resistors create a common-mode load. Recall from Section 3, each RS-485 driver is required to handle a 375-Ω common-mode load (32 unit loads in parallel), as shown in Figure 5-3.

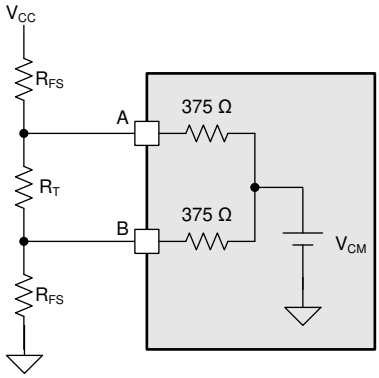

Figure 5-3. Thirty-Two Unit Loads in Parallel Presenting a Common-Mode Load

The issue is that the fail-safe resistors alone are presenting a common-mode load of 645 Ω. It is now important to calculate what additional common-mode load may be present in parallel before a common-mode loading of 375 Ω is present:

$$375 = \frac{1}{\frac{1}{R_{CM}} + \frac{1}{645}} \rightarrow \text{RCM} \approx 8963\ \Omega \tag{5}$$

Since each unit load can be approximated by a 12-kΩ common-mode load, calculate the maximum number of unit loads in parallel that can be used before presenting a common-mode load of less than 896 Ω:

$$896 < \frac{12000}{n_{UL}} \rightarrow n_{UL} > 13.4 \tag{6}$$

This means that the fail-safe resistors place a common-mode loading equivalent to 18.6 (32 – 13.4) unit loads, thereby drastically reducing the total number of allowable nodes on the network. Both methods of handling idle bus conditions have pros and cons, so it is up the designer to decide which method works best for their application.

6 When Termination is Necessary, and How to do it Properly

Many signal integrity and communication issues with RS-485 networks stem from terminations, either from a lack of termination or improper termination. This section discusses when not terminating your RS-485 network works, and when termination is required, and how to use standard (parallel) terminations and alternating current (AC) termination networks.

As shown in Section 5, the driver of an RS-485 transceiver must be able to drive 1.5 V across 32 unit loads and two 120-Ω terminations. Not included in that section is the fact that the 120-Ω value for termination resistors stems from what is known as the differential-mode characteristic impedance of the twisted-pair bus wires. Simply put, the wire gauge, insulation type and thickness, and number of twists per unit length all contribute to an impedance that high-speed data signals “detect". This impedance is denoted in ohms and typically ranges from 100 Ω to 150 Ω for twisted-pair cables. The writers of the RS-485 standard choose 120 Ω as the nominal characteristic impedance; therefore, to match this impedance the termination resistors also have a default value of 120 Ω.

Why termination networks exist

Matching the characteristic impedance of the cabling to the termination network enables the receiver on the end of the bus to determine the maximum signal power. By leaving a transmission line unterminated, or terminated with some value unequal to the impedance of the cable, a mismatch is introduced that creates reflections at the ends of the network. A reflection is where some of the energy of the signal literally returns back up the line, which can then constructively or destructively interfere with the next bits propagating down the bus. A destructive example is if the reflected signal which bounces back is out of phase with the incoming signal, resulting in the receiver detecting a smaller incoming signal. If the mismatch is large enough, the energy reflected back can cause subsequent bits to be misinterpreted and incorrectly decoded by the receiver.

Equation 7 shows that for the reflection coefficient to approach zero, the input impedance, Z_L, needs to match the source impedance, Z_S. If there is a large discrepancy in load and source impedance, almost the entire signal can reflect.

$$r = \frac{Z_L - Z_S}{Z_L + Z_S} \tag{7}$$

For optimal signal integrity, it is always best to match the AC line impedance with a termination of equal value. There is a reason that all designers would not choose to do this. Because adding termination networks adds cost to the overall system, and these termination networks also add a parallel load to the drivers, causing larger steady-state load currents. In power-sensitive applications where lowering power consumption is critical (such as in battery-powered applications), one option to save power is to leave the bus unterminated. The next section discusses when removing termination is a viable option.

Networks that do not need termination

One situation which does not need termination networks is when the two-way loop time of the network is much greater than a single bit time (approximately < 0.1 × two-way loop delay). In such scenarios, the reflections will lose energy each time they reach an end of the network.

As Figure 6-1 shows, the amplitude of the reflections will continue to decay each time the signal reflects at the end of the cable. Figure 6-1 shows three round trips for the signal and a total of six reflections.

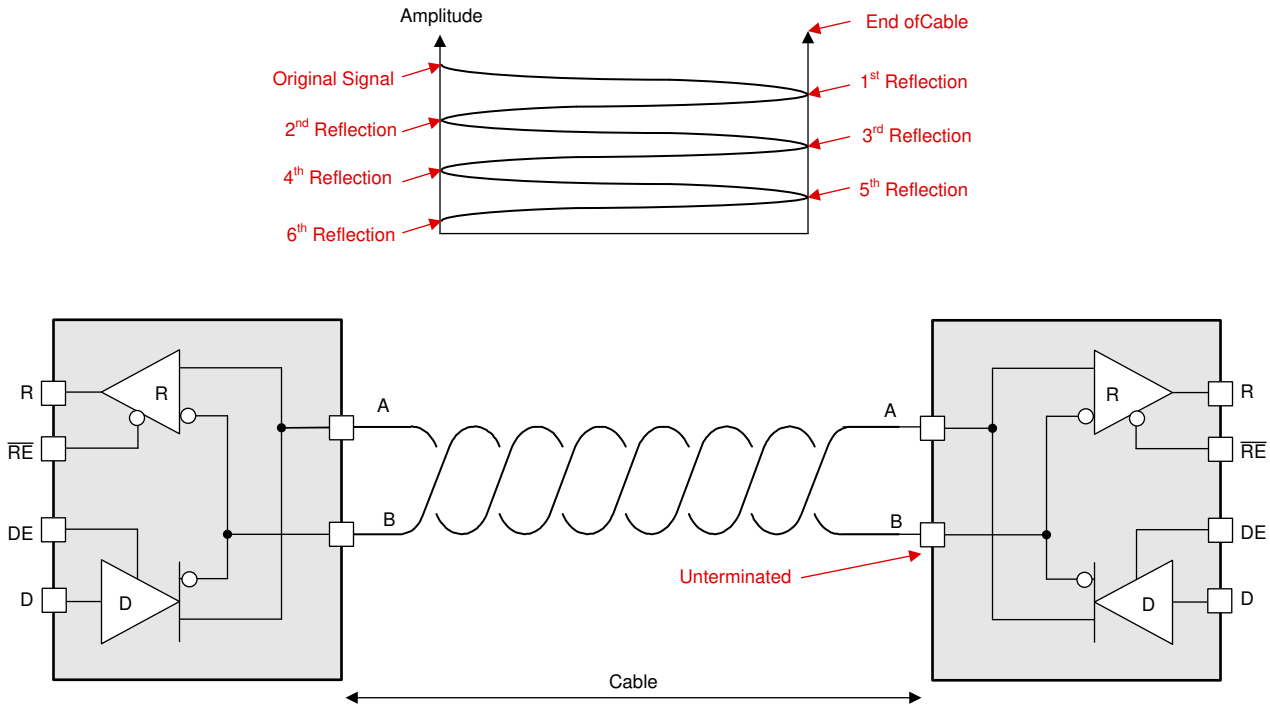

Figure 6-1. Amplitude of Reflection Decay Each Time a Reflection Occurs

Estimating that the unterminated end of the bus has a 96-kΩ input impedance (a one-eighth unit load), and the source impedance of the driver is 60 Ω, the signal reflections would decay according to the calculations listed in Table 6-1.

Table 6-1. Example Signal-Decay Calculations

Signal	Percentage of Signal	Calculation $\left(\frac{Z_L - Z_S}{Z_L + Z_S}\right)$
Original signal	100%	
After first reflection	99.75%	$1 \times \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = 0.9975$
After second reflection	–33.24%	$0.9975 \times \left(\frac{60 - 120}{60 + 120}\right) = -0.3324$
After third reflection	–33.16%	$-0.3324 \times \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = -0.3317$
After fourth reflection	11.05%	$-0.3317 \times \left(\frac{60 - 120}{60 + 120}\right) = 0.1106$
After fifth reflection	11.02%	$0.1106 \times \left(\frac{96{,}000 - 120}{96{,}000 + 120}\right) = 0.1102$
After sixth reflection	–3.68%	$0.1102 \times \left(\frac{60 - 120}{60 + 120}\right) = -0.0368$

As Table 6-1 shows, by the time the signal reflects for the sixth time, it has decayed to under 4% of its original magnitude. After this point the reflections are no longer capable of causing signal-integrity issues. Since the sample point of a bit typically occurs between 50%–75% of the way through the bit, make sure that these three round-trip delays occur before the sample point.

Networks that need termination

For applications where the bit time is not substantially longer than the loop time of the cable, termination is crucial for minimizing reflections. The most basic termination networks, which are known as standard termination or parallel termination networks, consist of a single resistor (Figure 6-2).

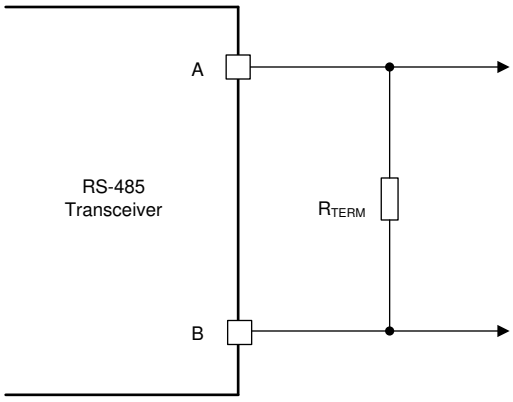

Figure 6-2. Standard Termination Network

For standard termination, match the termination resistor value with the differential-mode characteristic impedance of the cabling on both ends of the network. This ensures the proper termination of signals traveling in both directions on the bus. As previously mentioned, the major drawback for this type of termination scheme is that whenever the driver is active, the resistors are placing a direct current (DC) load on the driver.

Using AC terminations helps alleviate this power dissipation without having as long of a bit-time requirement with respect to bus length. Figure 6-3 shows an AC termination scheme.

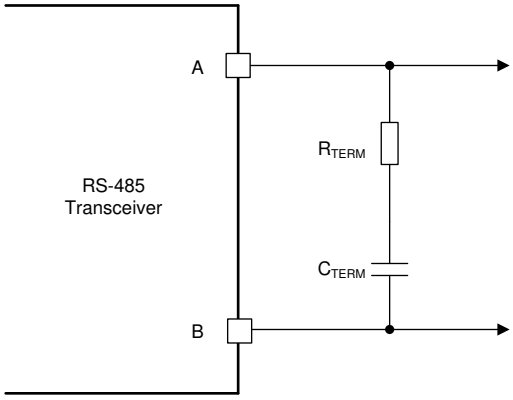

Figure 6-3. AC Termination Network

Since current typically flows from one side of an RS-485 driver through the termination network, then through the other side of the driver, by placing a series capacitor the steady state current goes to zero. The two caveats of this type of termination are that it requires one extra component on each termination network, and the series resistor and capacitor introduce a resistor-capacitor (RC) delay. The RC time constant will slow the rising and falling edge of the differential signal and limit the maximum data rate of the network.

Table 6-2. Summary of Termination Techniques

Termination Network	Power Dissipation	Data Rate	Signal Integrity
No termination	Low	Low	Good at low data rates, poor at high data rates
Standard termination	High	High	Great
AC termination	Low	Medium	Good

For optimal signal integrity, it is always best to match the differential-mode characteristic impedance of the cable with a termination of equal impedance. But if the proper steps are taken, it is also possible to successfully implement AC terminations or avoid termination altogether.

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