Application Report

TLIN10283-Q1 and TLIN10285-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Richard Hubbard

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1 TLIN10283-Q1 and TLIN10285-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1.1 Overview

This document contains information for TLIN10283-Q1 and TLIN10285-Q1 which are local interconnect network (LIN) transcievers with integrated LDO in 8-pin SOIC (D) package, 8-pin HSOIC (DDA) package and 8-pin VSON (DRB) package to aid in a functional safety system design.

Available Information:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

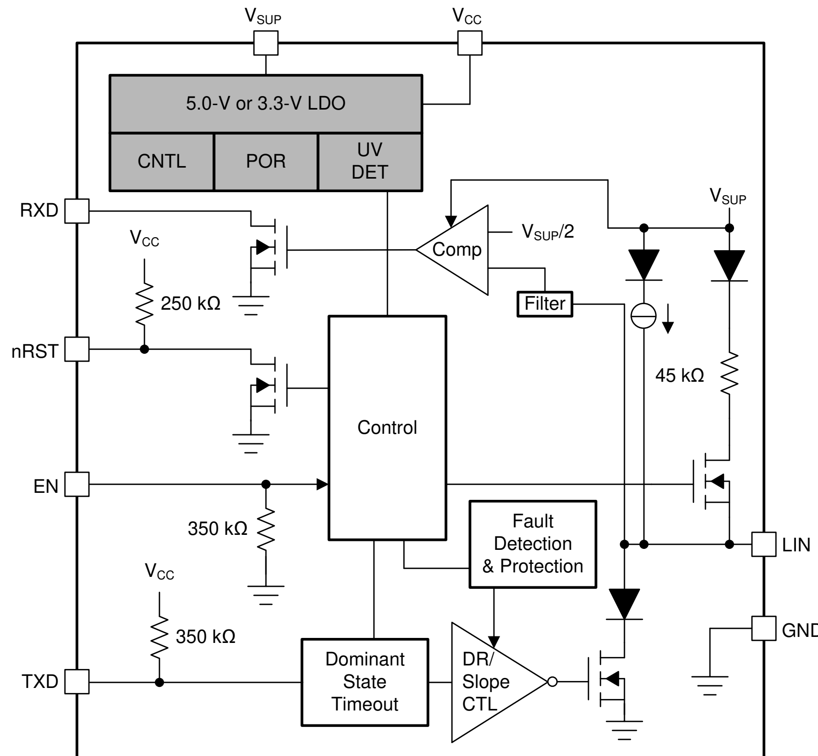

Figure 1-1. Functional Block Diagram

TLIN10283-Q1 and TLIN10285-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

1.2 Functional Safety Failure In Time (FIT) Rates by Package

This section provides Functional Safety Failure In Time (FIT) rates for the 8-pin SOIC (D), 8-pin HSOIC (DDA) and 8-pin VSON (DRB) packages of the TLIN10283-Q1 and TLIN10285-Q1 devices based on two different industry-wide reliability standards:

- Table 1-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11, full load
- Table 1-2 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11, 80% load
- Table 1-3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11, Full Load

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 8-pin HSOIC (DDA)	FIT (Failures Per 10^9 Hours) 8-pin VSON (DRB)
Total Component FIT Rate	24	23	22
Die FIT Rate	15	14	17

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Table 1-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11, Full Load (continued)

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 8-pin HSOIC (DDA)	FIT (Failures Per 10^9 Hours) 8-pin VSON (DRB)
Package FIT Rate	9	9	5

The failure rate and mission profile information in Table 1-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW for 8-pin SOIC (D) package
- Power dissipation: 1400 mW for 8-pin HSOIC (DDA) and 8-pin VSON (DRB) packages
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- Electircal overstress (EOS) FIT rate assumed: 0 FIT

Table 1-2. Component Failure Rates Per IEC TR 63380 / ISO 26262 Part 11, 80% Load

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D)	FIT (Failures Per 10^9 Hours) 8-pin HSOIC (DDA)	FIT (Failures Per 10^9 Hours) 8-pin VSON (DRB)
Total Component FIT Rate	19	20	18
Die FIT Rate	11	12	14
Package FIT Rate	8	8	4

The failure rate and mission profile information in Table 1-2 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 400 mW for 8-pin SOIC (D) package
- Power dissipation: 1260 mW for 8-pin HSOIC (DDA) and 8-pin VSON (DRB) packages
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- Electircal overstress (EOS) FIT rate assumed: 0 FIT

Table 1-3. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 1-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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1.3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLIN10283-Q1 and TLIN10285-Q1 in Table 1-4 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 1-4. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Transmitter fail	45%
Receiver fail	5%
LDO fail	20%
Logic or IO cell fail	10%
Global power or state control fail	20%

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1.4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the 8-pin SOIC (D), 8-pin HSOIC (DDA) and 8-pin VSON (DRB) packages of the TLIN10283-Q1 and TLIN10285-Q1 devices. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 1-6)
- Pin open-circuited (see Table 1-7)
- Pin short-circuited to an adjacent pin (see Table 1-8)
- Pin short-circuited to V_{SUP} (see Table 1-9)
- Pin short-circuited to V_{CC} (see Table 1-10)

Table 1-6 through Table 1-10 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 1-5.

Table 1-5. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

1.4.1 8-pin SOIC (D), VSON (DRB) and HSOIC (DDA) Packages

Figure 1-2 shows the pin diagram for the 8-pin SOIC (D) package. Figure 1-3 shows the pin diagram for the 8-pin VSON (DRB) package. Figure 1-4 shows the pin diagram for the 8-pin HSOIC (DDA) package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TLIN10283-Q1 and TLIN10285-Q1 datasheet.

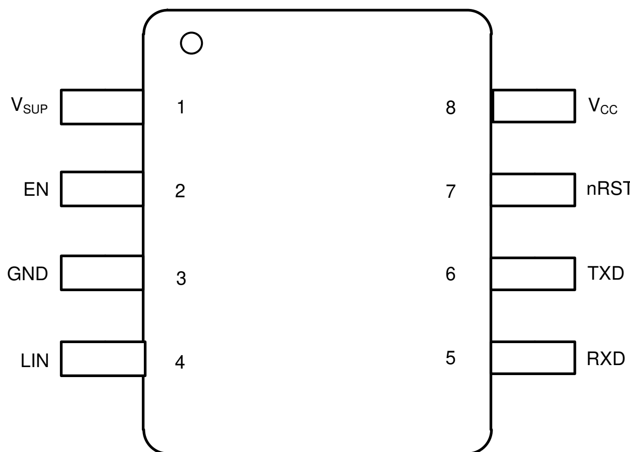

Figure 1-2. Pin Diagram (SOIC (D) Package)

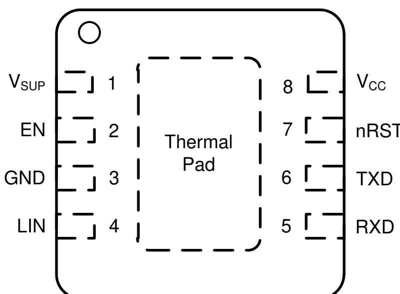

Figure 1-3. Pin Diagram (VSON (DRB) Package)

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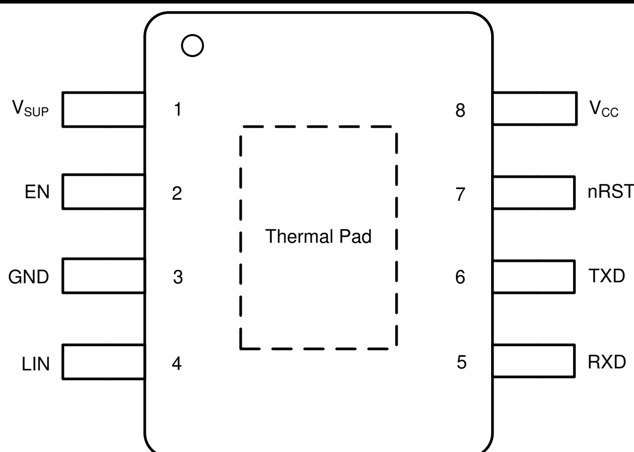

Figure 1-4. Pin Diagram (HSOIC (DDA) Package)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions within recommended operating conditions
- V_{CC} = 4.9 to 5.1V for TLIN10285-Q1
- V_{CC} = 3.23 to 3.37V for TLIN10283-Q1
- V_{SUP} = see recommended conditions in device data sheet

Table 1-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{SUP}	1	Device is unpowered and will not function	A
EN	2	Device may only operate in Standby mode after power-on. If the short occurs in Normal mode, the part would then be forced to enter SLP (TXD=dominant) or STBY (TXD=recessive) based on the state of TXD when the shorting occurred. The short to GND condition would disable LIN communication.	B
GND	3	None	D
LIN	4	LIN bus biased dominant, no LIN communication possible	B
RXD	5	RXD biased dominant, no communication from LIN bus to MCU possible	B
TXD	6	TXD biased dominant, no communication from MCU to LIN possible	B
nRST	7	nRST biased low causing the MCU to be in reset if connected in this manner	B
V_{CC}	8	Excessive current draw from V_{CC}. Thermal shut down will happen quickly.	A

Note

The DRB and DDA packages include a thermal pad.

Table 1-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure EffectClass
V_{SUP}	1	Device is unpowered and will not function	B
EN	2	Biased low due to internal pull-down so device in standby mode	B
GND	3	Device is unpowered and will not function	B
LIN	4	No LIN communication possible	B
RXD	5	No communication from LIN bus to MCU possible	B
TXD	6	No communication from MCU to LIN bus possible	B
nRST	7	No nRST output to MCU indicating a UV_{CC} event	C
V_{CC}	8	LDO unable to power external circuits	C

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Note

The DRB and DDA packages include a thermal pad.

Table 1-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
V_{SUP}	1	EN	EN pin absolute max will be exceeded	A
EN	2	GND	EN biased to ground. See EN shorted to GND	B
GND	3	LIN	LIN biased dominant. See LIN shorted to GND	B
RXD	5	TXD	Communication between MCU and LIN bus disrupted	B
TXD	6	nRST	TXD biased recessive unless UV_{CC} event and then biased dominant, MCU to LIN bus communication not possible	B
nRST	7	V_{CC}	nRST internally connected to V_{CC} but a UV_{CC} event may not be provided to MCU in timely manner	C

Note

The DRB and DDA packages include a thermal pad. There is a chance the thermal pad is soldered down could short to any pin on device. What the thermal pad is soldered to determines the behavior. Example: if soldered to a ground plane then the adjacent pins would behave as if shorted to ground.

Table 1-9. Pin FMA for Device Pins Short-Circuited to V_{SUP}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	2	Absolute max voltage exceeded	A
GND	3	Device will not function	A
LIN	4	Device biased recessive, no bus communication possible	B
RXD	5	Absolute max voltage exceeded	A
TXD	6	Absolute max voltage exceeded	A
nRST	7	Absolute max voltage exceeded	A
V_{CC}	8	Absolute max voltage exceeded	A

Note

The DRB and DDA packages include a thermal pad.

Table 1-10. Pin FMA for Device Pins Short-Circuited to V_{CC} (LDO Output)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure EffectClass
V_{SUP}	1	Absolute max voltage exceeded on V_{CC}	A
EN	2	EN biased high, mode change may not be possible	B
GND	3	Device will not function	A
LIN	4	Absolute max voltage exceeded on V_{CC}, no bus communication	A
RXD	5	RXD biased recessive, no communication to MCU	B
TXD	6	TXD biased recessive, no communication from MCU	B
nRST	7	None - internally biased to V_{CC}	D

Note

The DRB and DDA packages include a thermal pad.

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2020	*	Initial release.

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