Application Report
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How to Design LVDS SerDes in Industrial Systems

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ABSTRACT

The purpose of this application note is to highlight the benefits of LVDS over parallel, single-ended signaling, and to present design guidelines for designing LVDS and SerDes in industrial applications.

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1 Introduction

LVDS (Low Voltage Differential Signaling) is a differential signaling technology that uses very low amplitude signals (100Mv~450mV) to transmit data through a pair of parallel PCB traces or balanced cables. The current and voltage amplitudes flowing through the two parallel differential signal lines are opposite. Noise is coupled onto both lines at the same time, but the receiving end only cares about the difference between the two signals so the noise is cancelled out. Since the electromagnetic fields around the two signal lines also cancel each other out, the differential signal transmission electromagnetic radiation is much smaller than the single-ended signal transmission electromagnetic radiation. In addition, the transmission standard adopts current mode to drive the output, so it does not generate peak signals caused by ringing and signal switching, and has good EMI (electromagnetic interference) characteristics.

Since LVDS technology reduces noise concerns, lower signal voltage amplitudes can be used. This feature is important because it makes it possible to increase the data transmission rate and reduce power consumption. Also, since the driver is a constant current source, power consumption will barely change with frequency, and the power consumption of a single channel is very low.

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2 LVDS Working Principles and Features

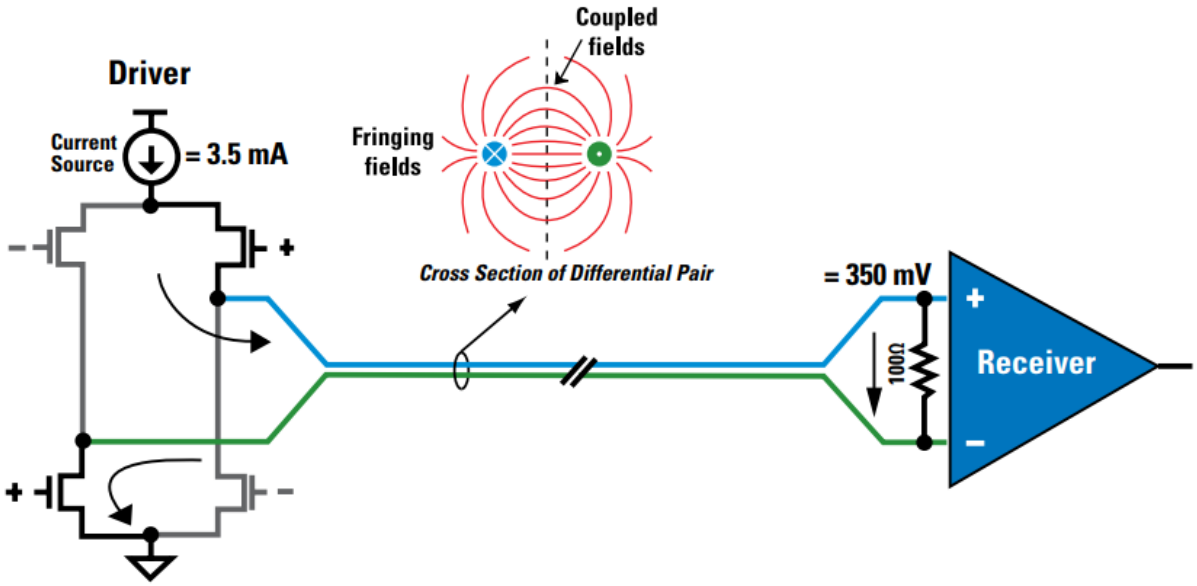

Figure 1. LVDS Driver and Receiver

Figure 1 shows a diagram of LVDS operation. The driver consists of a constant current source (usually 3.5 mA) driving a pair of differential signal lines. There is high DC input impedance at the receiver (almost no current consumption), so almost all of the driver current will flow through a 100 Ω termination resistor to generate about 350 mV at the receiver input.

LVDS technology features include:

1. High-speed transmission capabilities up to 2 Gbps
2. Low voltage, low power consumption
3. Low noise radiation
4. Significant interference immunity due to differential signaling

LVDS has many benefits over traditional single-ended signaling topologies like parallel LVTTL/LVCMOS. The main benefits include EMI (electromagnetic interference) reduction, faster data rates, extended transmission distances, and cost/convenience.

3 EMI

Electromagnetic interference is a significant issue to overcome in industrial systems. A parallel interface with multiple parallel outputs can generate quite a bit of EMI due to the amount of cables needed, the length of the cables, and cross talk between the cables. The more parallel outputs being transmitted, the more apparent the EMI generation becomes. Additionally, high data rates increase EMI generation due to faster and sharper edge rates. This EMI generation is compounded with parallel LVTTL/LVCMOS interfaces since all of the lanes would see faster/sharper edge rates with increased data rates.

EMI generation is reduced in LVDS interfaces due to the differential aspect of the technology, and the fact that it reduces the amount of outputs being transmitted. The balanced, differential lines have two equal but opposite signals. The concentric magnetic fields radiated by each of the two conductors cancel a significant portion of the emissions each of the two lines would generate on their own.

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For Generation 2 and Generation 3 LVDS SerDes (Serializer/Deserializer), another benefit is improved system reliability and reduced EMI with RBS (randomization, DC balancing, scrambling) coding. Static display images can include many of the same color bits – which can create DC wander and impact the signal quality along with creating EMI beats. The RBS encoding randomizes the data and scrambles bit positions to remove static patterns and ensure transitions, and then DC balances the signal to allow AC coupling of the link to provide isolation. The end result of this encoding is less jitter, and more spreading of the spectral content of the transmitted data for reduced EMI.

4 Data rate, Distance, and Cost/Convenience

Data rate is another benefit that LVDS has over LVTTL/LVCMOS, because data rate is very limited with parallel interfaces. As stated in Section 3, with many outputs being transmitted in parallel, the faster each signal travels, the more EMI is generated. Additionally, pair to pair skew, which significantly limits the distance the signals can travel, gets worse at faster data rates. With LVDS, the data rate is greater and the distance is extended by more than 10m. PCB design is also a lot easier since length matching consideration is reduced and there is more space to work with.

Using an LVDS interface significantly reduces the size of the PCB and connector compared to that of parallel LVTTL/LVCMOS. This reduces the cost of the entire system. Additionally, whenever maintenance is needed on these systems, the large amount of cables present in current systems that uses parallel interfaces, like LED walls for example, are difficult to debug. Also, space is limited in the area behind the LED wall so all repairs need to be done on the front side. This is not an issue with an LVDS interface since the amount of cables is reduced significantly, which makes maintenance easier and a lot more manageable.

5 How to Use LVDS SerDes in Industrial Systems

When devices exchange data, the traditional transmission standard is LVTTL, LVCMOS, or other single-ended interface standards. These communication methods are not only susceptible to interference, but their bandwidth (data transmission rate) also cannot be improved. If the user wants to increase the bandwidth, more data channels must be provided. This increases system costs, and increases complexity and introduces difficult synchronization schemes. However, if the LVDS standard is adopted, these problems can be effectively solved. To achieve this method:

- Use LVDS buffer differential design. The board-level, single-ended signal is connected using LVDS to ensure signal immunity and reliability. This scheme can improve interference immunity, as shown in Figure 2:

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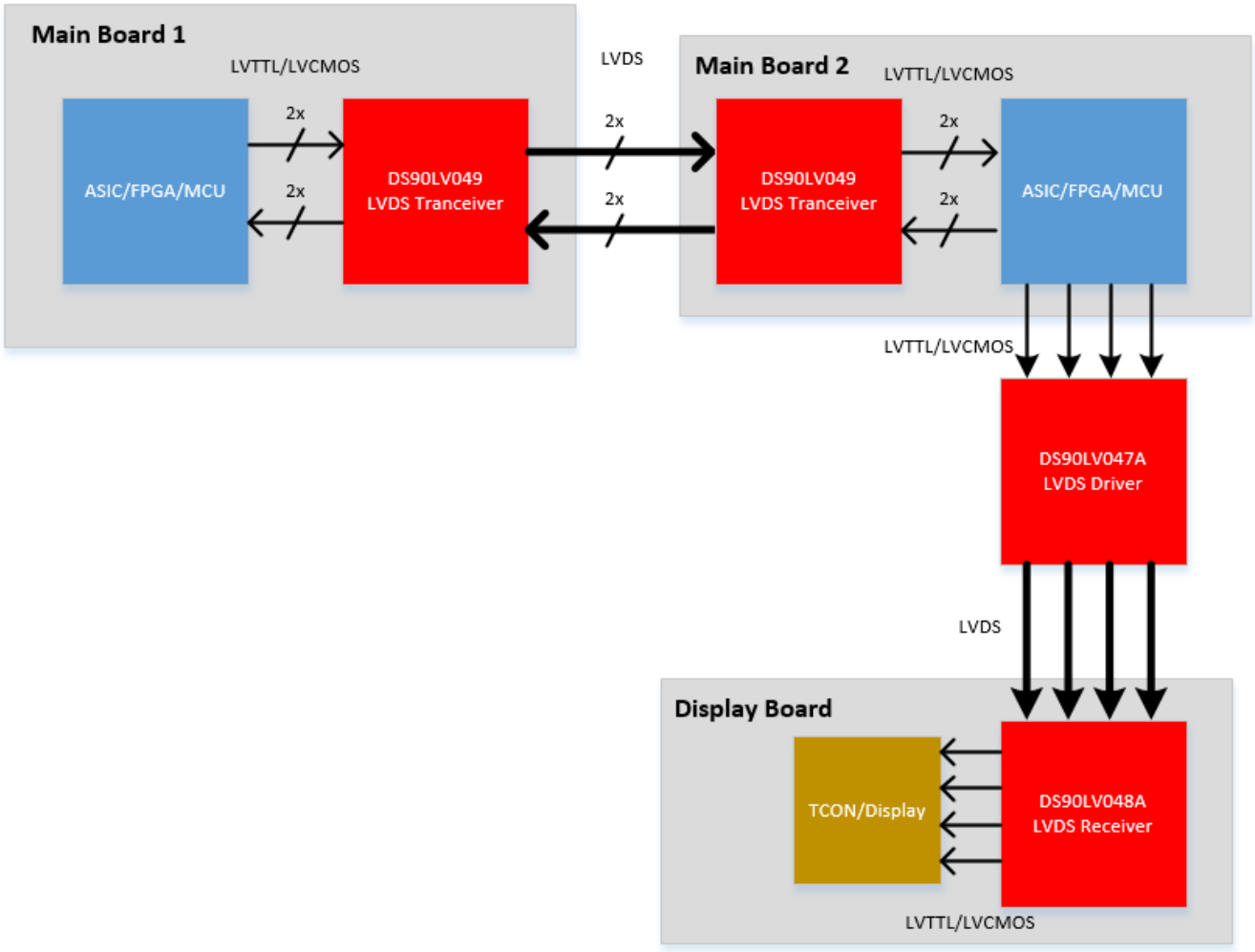

Figure 2. LVDS in Industrial Video Application

- Use LVDS SerDes design to convert parallel, single-ended signals on the board to a single twisted pair (STP) line to optimize product design. This design works for board-to-board, device-to-device links, and offers excellent interference immunity and a reduction in board size.

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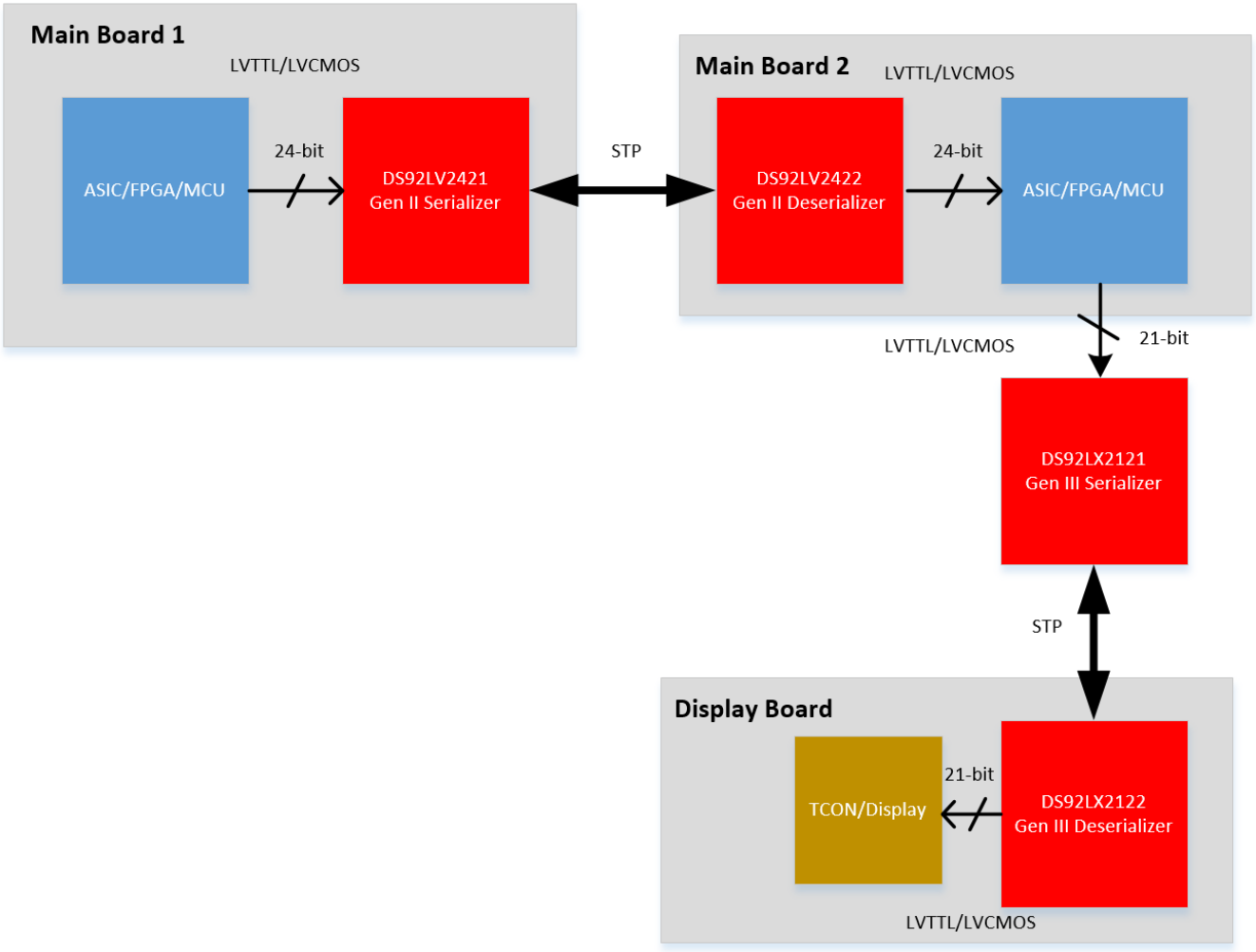

Figure 3. LVDS SerDes in Industrial Video Application

The DS92LV242x SerDes transmit and receive 24 bits of data and 3 control signals over a single twisted pair operating at up to 2.1 Gbps with embedded clock, something not feasible with traditional LVTTL.

An LED wall is an example of an industrial application where use of LVDS SerDes benefits the design.

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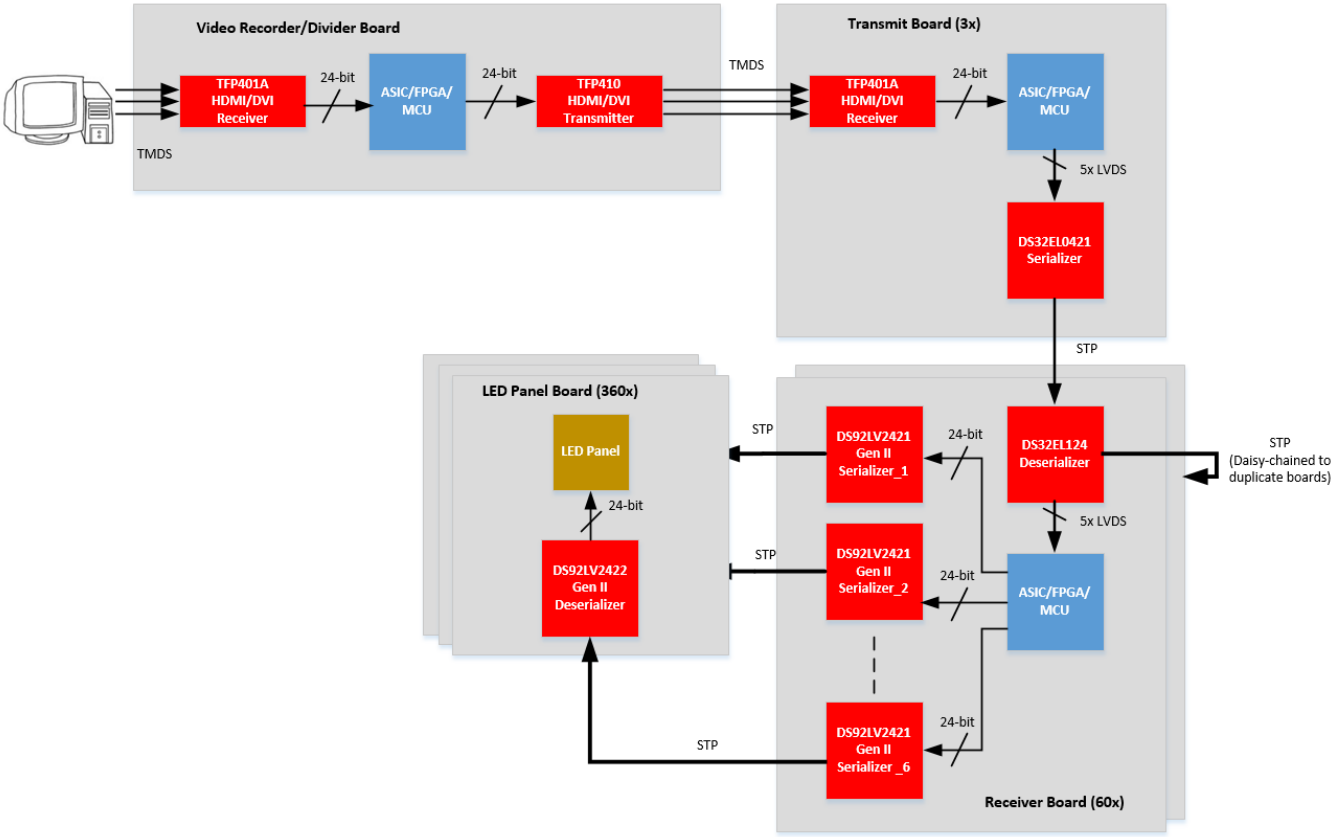

Figure 4. LVDS SerDes in LED Wall

Figure 4 is a block diagram of a typical LED wall design. In this particular design, the recorder/divider board records and divides the input HDMI/DVI into 3 outputs and sends it to 3 separate transmission boards.

The transmission boards then serialize the video data with the DS32ELX0421 serializer and send it to a DS32ELX0124 deserializer on the receiver board. The DS32ELX0421 deserializers are daisy chained so one serializer is connected to multiple deserializers by using the retimed output of the deserializer. In this example, that enables the use of 60 receiver boards.

The receiver boards then send the video data to the LED panel boards via SerDes. Each LED panel board has 1 DS92LV2422 deserializer, while each receiver board has 6 DS92LV2421 serializers. Since there are 60 receiver boards in this design, this means that there are 360 LED panel boards.

6 The LVDS SerDes Design Specifications

During the design process, consider these points:

- EMI
  - LVDS signal filters are designed primarily to address things such as clock signal and bus signal noise. RC filters should be added to the transmit side of the clock signal to minimize external radiated emissions. Differential signals should have common mode chokes to suppress common mode noise.
  - The signal interference-immune design is divided into fixed path interference and environmental interference.
- Fixed Path
  - The interference path is usually a power source or a signal line. Therefore, capacitors should be added so that the interference is shorted to ground.

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- Environmental Interference
  - This interference is caused by electromagnetic radiation from external sources in the environment. Protective measures such as adding ferrite beads and capacitors are typically used to reduce the effects of this interference.
- To reduce crosstalk between single-ended signals and LVDS signals:
  - On the same PCB layer, single-ended signals need to be separated from the LVDS signals by at least 12 mm.
  - The distance between the two conductors of a differential line should be kept to a minimum to have maximum coupling of the magnetic field lines. A standard rule is to have the distance less than the thickness of the board and less than twice the width of one conductor.
  - The distance between two adjacent differential pairs should be greater than or equal to twice the distance between the two individual conductors of a single differential pair.
- Impedance matching
  - For impedance matching, the user should follow:
    - At least a 4-layer PCB board. One layer each for LVDS signals, LVTTL/CMOS signals, power, and ground. The power and ground layers should be used to isolate the LVDS layer from the LVTTL layer.
    - The LVDS drivers and receivers should be as close as possible to the connector.
    - Place a 4.7 μF or 10 μf capacitor close to the driver and receiver Vcc pins and take into account the matching of the signal operating frequency and the capacitor optimal operating frequency.
    - Place at least a 0.1 μF and a 0.001 μf capacitor close to each of the two driver or receiver Vcc pins.
    - The power and ground lines should be as wide as possible to reduce the power return impedance.

7 Summary

LVDS signal transmission and SerDes technology meet the needs of todays high-bandwidth, low-power transmission requirements. They have various benefits over traditional, single-ended transmission technologies like LVTLL. These include EMI reduction, increased data rate, size/space advantages, design complexity, transmission distance, etc. In industrial applications like LED walls, these advantages go a long way in helping to meet design requirements.

Due to their high-speed, low-voltage characteristics, design guidelines should be followed to address signal integrity issues. Practice has proved that following these design specifications can circumvent LVDS and SerDes design problems.

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