Application Report
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TUSB1042I, TUSB546A-DCI, TUSB1046A-DCI: Enabling DCI

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ABSTRACT

Included in the TUSB1042I, TUSB546A-DCI and the TUSB1046A-DCI is an Intel proprietary closed-chassis debug interface called Direct Connect Interface (DCI). Because DCI is an Intel proprietary interface, this document will only focus on the TUSB1042I, TUSB1046A-DCI and TUSB546A-DCI hardware requirements needed to support DCI.

Contents

1 Introduction 1
2 TUSBx46 DCI Requirements 2
3 DCI Support with a I²C Master Enabled PD Controller 3
4 DCI support with a GPIO Only PD Controller 4
5 Example Software 6

List of Figures

1 DCI Configuration with I²C Master Enabled PD Controller 3
2 DCI Configuration with a GPIO Enabled PD Controller 4

List of Tables

1 TUSBx46 DCI Requirements 2
2 GPIO Control to TUSBx46 Configuration Mapping 4

Trademarks

1 Introduction

The TUSB1042I, TUSB546A-DCI and TUSB1046A-DCI is a Type-C linear redriver mux intended for Type-C source applications. The TUSB546A-DCI multiplexes between four DP1.4 lanes and USB3.1 Gen1 (5 Gbps) to a single Type-C receptacle. The TUSB1046A-DCI multiplexes between four DP1.4 lanes and USB3.1 Gen2 (10 Gbps) to a single Type-C receptacle. For the remainder of the document TUSBx46 notation will be used to describe TUSB1042I, TUSB1046A-DCI and TUSB546A-DCI.

The TUSBx46 support the Intel proprietary closed-chassis debug interface called Direct Connect Interface (DCI). When an Intel SVT Closed Chassis Adapter (SVTCCA or BSSB) is plugged into a properly designed USB-C system which uses the TUSBx46, the user can debug system issues like initial cold boot, suspend-state operation and survival, Reset-flows, and USB3 or IOSF path failures.

2 TUSBx46 DCI Requirements

Table 1 details the requirements which must be met in order for DCI to function properly. All requirements listed in the table must be met.

Table 1. TUSBx46 DCI Requirements

REQUIREMENT NO.	DESCRIPTION
1	TUSBx46 must be enabled for I^2C mode. I2C_EN (pin 17) must be either pulled up to 3.3 V through 1k (5%) resistor or left floating. 1 k resistor is required if I^2C interface is at 3.3 V LVCMOS levels.
2	TUSBx46 RX1P/N and RX2P/N must be DC-coupled to USB-C receptacle. AC-coupling capacitor on RX1P/N or RX2P/N is not allowed.
3	TUSBx46 TX2P/N and TX1P/N must be AC-coupled to USB-C receptacle. AC-coupling capacitor in the range of 75 nF to 265 nF should be used.
4	TUSBx46 DCI_CLK (pin 32) must be connected to Intel PCH GPIO pin thru a 22-Ω (1%) series resistor. Place resistor as close to TUSBx46 as possible. The Intel PCH GPIO must be configured for 3.3 V LVCMOS levels.
5	TUSBx46 DCI_DAT (pin 29) must be connected to Intel PCH GPIO pin thru a 22-Ω (1%) series resistor. Place resistor as close to TUSBx46 as possible. The Intel PCH GPIO must be configured for 3.3 V LVCMOS levels.
6	TUSBx46 SSRXP/N must be AC-coupled to PCH's USB3.1 Host SSRXP/N. AC-coupling capacitor in the range of 75 nF to 265 nF should be used.
7	TUSBx46 SSTXP/N must be AC-coupled to PCH's USB3.1 Host SSTXP/N. AC-coupling capacitor in the range of 75 nF to 265 nF should be used.
8	The TUSBx46 supports a maximum DCI clock of 133 MHz. Intel SVT CCA clock frequency must be set to less than or equal to 133 MHz. The DCI clock frequency is controlled from the HostConfig.xml file located in the C:\Intel\DAL directory.

3 DCI Support with a I²C Master Enabled PD Controller

Figure 1 details the required connections to support DCI when using a I²C Master enabled PD controller. The figure does not detail the DisplayPort and AUX/SBU connections since these functions are not needed for DCI functionality. Refer to the TUSB1046A-DCI (SLLSF13) or TUSB546A-DCI (SLLSF14) datasheet for details on DisplayPort and AUX/SBU connections.

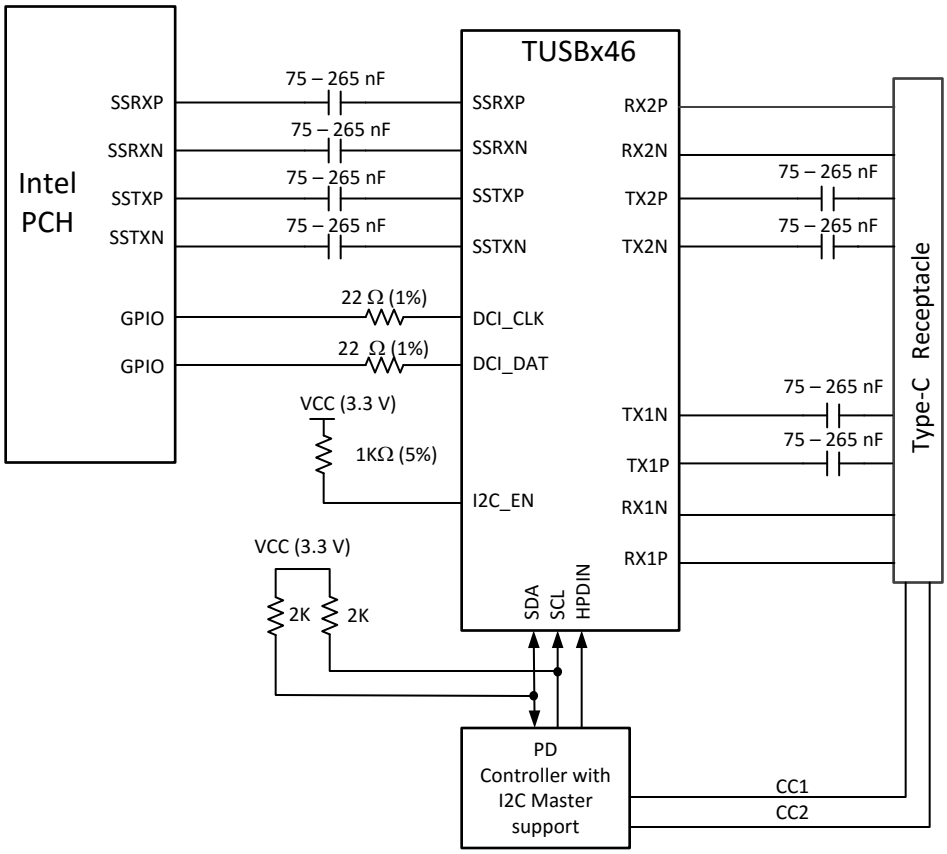

Figure 1. DCI Configuration with I²C Master Enabled PD Controller

4 DCI support with a GPIO Only PD Controller

The TUSBx46 must be enabled for I²C Mode for DCI to operate (refer to requirement #1 in Table 1). There are some PD controllers, like the Texas Instruments TPS65982, which do not support I²C master; and therefore, can only support GPIO mode. For systems which use this type of PD controller, another external MCU must be used to perform the required I²C write transactions to the TUSBx46.

Figure 2 does not detail the DisplayPort and AUX/SBU connections since these functions are not needed for DCI functionality. Refer to the TUSB1046A-DCI (SLLSF13) or TUSB546A-DCI (SLLSF14) datasheet for details on DisplayPort and AUX/SBU connections

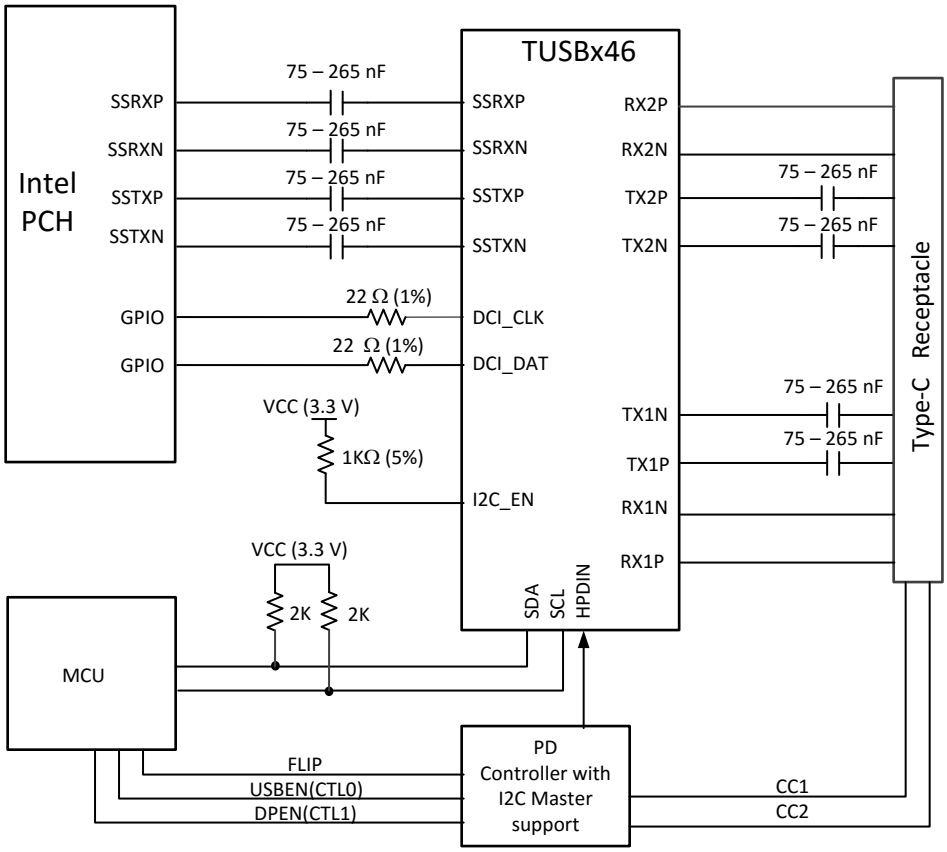

Figure 2. DCI Configuration with a GPIO Enabled PD Controller

The MCU monitors the three control signals (FLIP, USBEN, and DPEN) from the PD controller and update the TUSBx46 register 0xA as appropriate. Table 2 describes values written to the register based on state of the three control signals.

Table 2. GPIO Control to TUSBx46 Configuration Mapping

DPEN (CTL1) PIN	USBEN (CTL0) PIN	FLIP PIN	TUSBx46 Configuration	TUSBx46 Register 0x0A Bits 2:0
L	L	X	Power Down	3'b000
L	H	L	One Port USB 3.1 - No Flip	3'b001
L	H	H	One Port USB 3.1 – With Flip	3'b101
H	L	L	4 Lane DP - No Flip. Not applicable to TUSB1042I.	3'b010
H	L	H	4 Lane DP – With Flip. Not applicable to TUSB1042I.	3'b110
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip. Not applicable to TUSB1042I.	3'b011

Table 2. GPIO Control to TUSBx46 Configuration Mapping (continued)

DPEN (CTL1) PIN	USBEN (CTL0) PIN	FLIP PIN	TUSBx46 Configuration	TUSBx46 Register 0x0A Bits 2:0
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip. Not applicable to TUSB1042I.	3'b111

5 Example Software

```
// TUSBx46 Example Code
// TUSBx46 7-
bit I2C slave address is based on sampled state of pin 11 (SSEQ0/A0) and 14 (DPEQ0/A1).
//
typedef enum
{
    GENERAL_CTL  = 0x0A,
    DP10EQ_SEL   = 0x10,
    DP32EQ_SEL   = 0x11,
    AUX_SNOOP_STATUS = 0x12,
    AUX_DPLANE_CTL = 0x13,
    TYPEC_EQ_SEL = 0x20,
    SSEQ_SEL = 0x21

} csr_TUSB_reg_t;

// Initialize TUSBx46 after power-up.
// EQ level 7 is chosen as a place holder.  Customer should change value based on their system
loss.
void TUSBx46_initialization (void)
{
     csr_write(GENERAL_CTL, 0x11); //USB3.1 only, Normal Orientation, and EQ_OVERRIDE enabled.
     csr_write(DP10EQ_SEL, 0x77);  //EQ level 7 for both DP Lanes 0 and 1.
     csr_write(DP32EQ_SEL, 0x77);  //EQ level 7 for both DP Lanes 2 and 3.
     csr_write(AUX_DPLANE_CTL, 0x00);  //AUX Snoop enabled. DP lanes enabled/disabled based on
AUX snooped value.
     csr_write(TYPEC_EQ_SEL, 0x77);  //EQ level 7 for both RX1 and RX2.
     csr_write(SSEQ_SEL, 0x07);  //EQ level 7 for SSTX.
}
void TUSBx46_INTN_handler (void)
{

    if (TYPEC_STATE == USBONLY) //USB3.1 Only.
    {
       If (ORIENTATION == 0) // Normal Orientation
       {
           csr_write(GENERAL_CTL, 0x11); //USB3.1 only, Normal Orientation, and EQ_OVERRIDE
enabled.
       }
       else //FLIP Orientation
       {
           csr_write(GENERAL_CTL, 0x15); //USB3.1 only, FLIP Orientation, and EQ_OVERRIDE enabled.
       }

    }
    else if (TYPEC_STATE == USBDP) // Both USB3.1 and 2 lanes of DP.
    {
       If (ORIENTATION == 0) // Normal Orientation
       {
           csr_write(GENERAL_CTL, 0x13); //USB3.1 and DP, Normal Orientation, and EQ_OVERRIDE
enabled.
       }
       else  //FLIP Orientation
       {
           csr_write(GENERAL_CTL, 0x17); //USB3.1 and DP, FLIP Orientation, and EQ_OVERRIDE
enabled.
       }

    }
    else if (TYPEC_STATE == DPONLY) // 4 Lanes of DP.
    {
       If (ORIENTATION == 0) // Normal Orientation
       {
           csr_write(GENERAL_CTL, 0x12); //4 lanes of DP, Normal Orientation, and EQ_OVERRIDE
enabled.
```

```
            }
            else //FLIP Orientation
            {
                csr_write(GENERAL_CTL, 0x16); //4 lanes of DP, FLIP Orientation, and EQ_OVERRIDE
      enabled.
            }

        }
        else  //Unattached
        {
               csr_write(GENERAL_CTL, 0x10); //Disabled, and EQ_OVERRIDE enabled.
        }

        return;
      }
```

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