Using Signaling Rate and Transfer Rate

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ABSTRACT

This document defines data signaling rate and data transfer rate, and it demonstrates the differences between them. Taking the SN65LVDS386 and SN65LVDS387 16-channel low-voltage differential (LVDS) line drivers and receivers with random parallel data of various bandwidths as an example, this document discusses the components that make up the system timing budget and presents empirical data on crosstalk-induced jitter. It provides criteria for measurements and demonstrates the differences between signaling and transfer rates for a variety of bus widths.

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1 Introduction

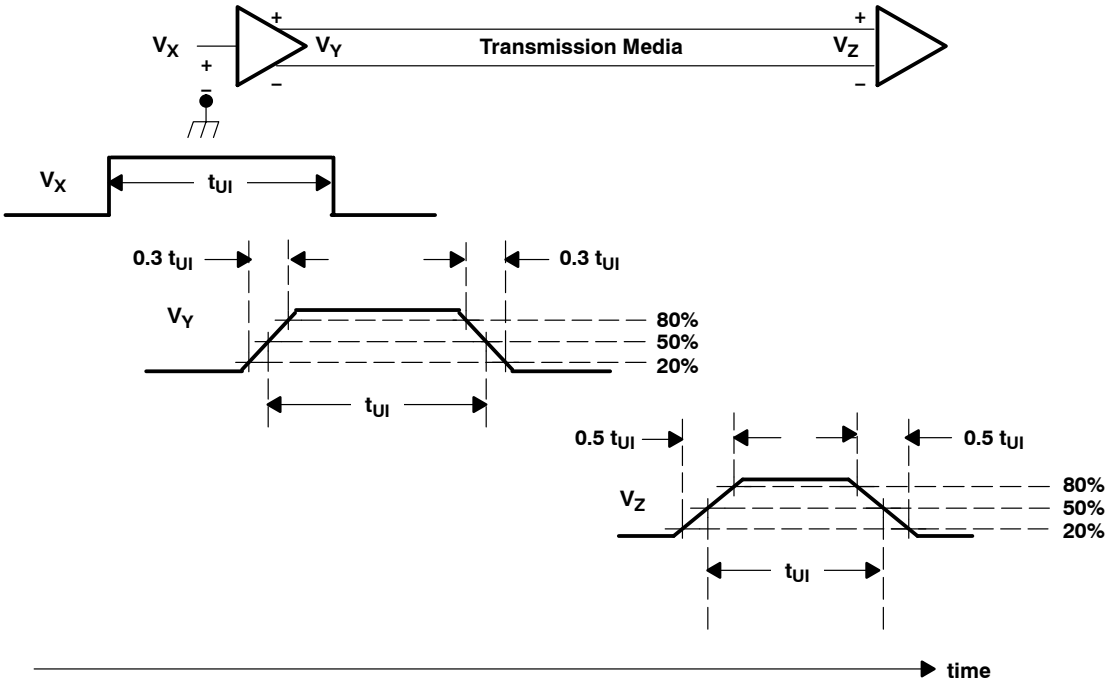
Numerous terms and units are used to quantify the ability of a data transmission circuit to move data from one point to another. At the physical layer (electrical and mechanical), data signaling rate and data transfer rate are the parameters most often used. The following sections provide basic definitions of signaling and transfer rates and demonstrate their use by describing an application of the SN65LVDS386 and SN65LVDS387 16-channel low-voltage differential signaling (LVDS) line drivers and receivers.

2 Signaling Rate

The basic functions of a line driver or line receiver are the detection of a logic state change at its input and indication of the state change at an output. The signaling rate, or data signaling rate, is simply the number of state changes made per a unit of time. It does not distinguish between data, clock, or handshaking signals, nor does it depend upon the bus architecture or protocol. It merely describes the speed at which a single bit is transmitted and received. Hence, the unit bits per second (bps) is used (bps has replaced the term baud in binary transmission systems).

Signaling rate is an important parameter when determining the bandwidth requirements of the data interchange circuit of a line driver, interconnecting media, and line receiver (see Figure 1). The input of two successive state changes forms the beginning and end of a voltage or current pulse that is successively transmitted down the circuit. As might be expected, there is a limit to how short the pulse duration can be and still be recovered successfully at the other end of the signal chain.

There must be signal quality criteria to specify or describe the minimum pulse duration or maximum signaling rate of a circuit. The quality of a binary data pulse is generally described by the amount of time spent in transition between states relative to the duration of the pulse. This criterion is often defined for specific applications or in interface standards such as TIA/EIA−644 Low-Voltage Differential Signaling. In this standard, the pulse duration is defined as the unit interval or t_{UI} and the maximum transition times as a fraction of t_{UI}. Figure 1 shows the signal quality criteria from TIA/EIA−644.



NOTE: Figure not to scale.

Figure 1. TIA/EIA-644 Driver Signal Quality Requirement and Receiver Input Recommendation

According to the TIA/EIA−644 criteria, when the signal transition time reaches 0.5 t_{UI} at the end of the transmission line, the minimum pulse duration and maximum signaling rate have been determined for a single interface circuit. When evaluating the signaling rate capability of the line circuits, a lossless line is assumed and the 0.3 t_{UI} limit is applied to both the driver and receiver. This is because the degradation of the transition time to 0.5 t_{UI} allows for losses in the transmission media and not the line circuits. The following equation restates the criteria mathematically.

$$t_{UI} \geq \frac{t_{20\% \textit{ to } 80\%}}{0.3} \text{ or } t_{UI} \geq \frac{t_{80\% \textit{ to } 20\%}}{0.3}$$

NOTE: The transition time is measured for the entire signal swing and not from the receiver threshold. For example, 0.5 t_{UI} transitions still allow the minimum duration data pulse to attain the steady-state level.

The minimum t_{UI} establishes the maximum signaling rate for a single circuit and defines the shortest period of time that the logic state may be sampled and processed. When more than one circuit and output is sampled at the same instant, another parameter is used to describe the performance and to account for other factors. This is the parallel transfer rate.

3 Transfer Rate

A common approach to increasing the rate of data transfer is to operate more than one interchange circuit simultaneously. When this is done with the same timing reference or clock, it is known as a synchronous parallel data transfer. Synchronous parallel data transfer imposes additional constraints on the period that a valid logic state may be sampled for processing. Due to this constraint, the parallel transfer rate, or simply transfer rate, is used to describe performance.

The definition of transfer rate is similar to that of signaling rate. Transfer rate includes timing effects of parallel transfers, and it is expressed in transfers per second (usually abbreviated as xfers/s or xfrs/s). It is not as important in specifying circuit bandwidth requirements as signaling rate, but it is more important than signaling rate in maintaining timing margin at the destination of the transfer. As shown in Figure 2, multiple interchange circuits produce responses slightly displaced in time at the outputs of the driver, transmission media, and line receiver. Ultimately, this acts to reduce the valid sample time from that available for a single circuit.

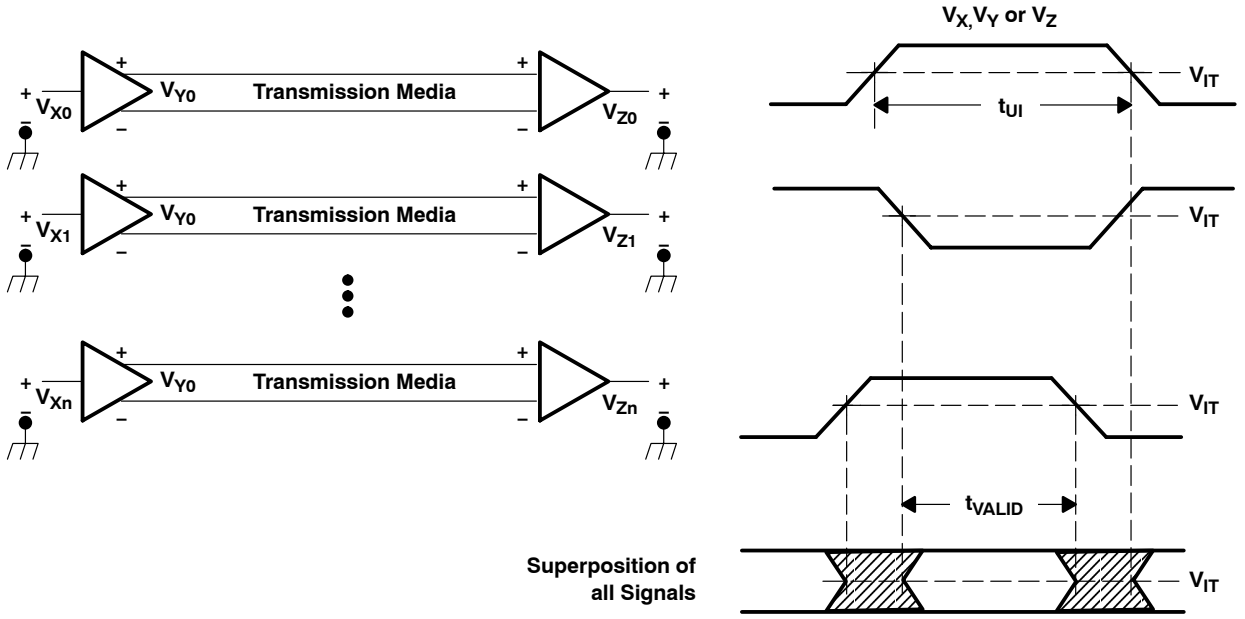


Figure 2. Parallel Operation of Data Interchange Circuits

There is no generally accepted standard for the minimum valid sample time ($t_{VALID,}$). A default of 0.4 t_{UI} is adopted here. In other words, 60% of the unit interval is allowed to be an uncertain logic state. The following equation restates the criteria mathematically.

$$t_{UI} \leq \frac{t_{VALID}}{0.4} \text{ or } t_{UI} \geq \frac{t_{INVALID}}{0.6}$$

4 Example

The following examples apply the preceding definitions to measurements of the SN65LVDS386 and SN65LVDS387 16−channel LVDS drivers and receivers. The SN65LVDS386/387 are members of TI's wide parallel LVDS devices, incorporating 16 drivers and receivers, respectively, in one single TSSOP package.

A circuit consisting of one driver of the SN65LVDS387, 0.5 m of ribbon cable, and one receiver of the SN65LVDS386 was evaluated, because the signaling rate describes the speed at which a single bit is transmitted and received. A pattern generator and a high-speed oscilloscope were used to monitor the receiver output as the signaling rate of the source was increased until the receiver output transition times were 0.3 t_{UI}. (Appendix A. Measurement Setup gives a more detailed description.)

The resultant signal from this experiment is shown in Figure 3 and reveals that, at a unit interval of 1.81 ns, the 20%-to-80% rise times are 440 ps and 0.24 t_{UI}. This is a signaling rate of 1/t_{UI} and 552 Mbps. An extrapolation of the 440 ps edge to 0.3 t_{UI} would give a maximum signaling rate of 682 Mbps under the adopted criteria and a nominal set of operating conditions. (A worst-case estimate for the signaling rate of a circuit must take into account the effects of temperature, supply voltage, and process variation.)

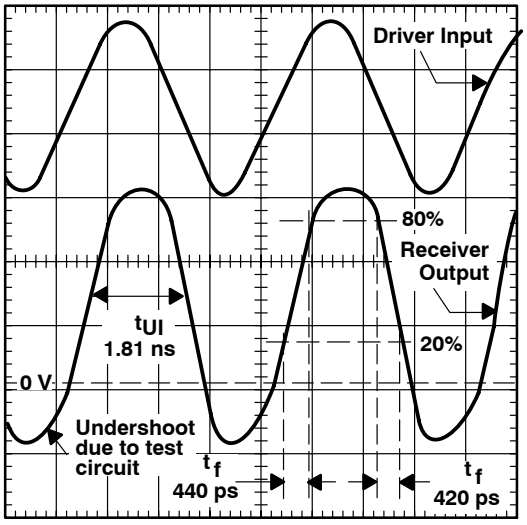


Figure 3. Typical Signals at the Maximum Signaling Rate

Using the same test setup, additional circuits were connected to determine the maximum parallel transfer rate. Pseudorandom data patterns were transmitted through four, eight, twelve, and sixteen circuits. The transfer rate was adjusted to provide t_{VALID} = 0.4 t_{UI} for each data path width.

The result of the 16-bit bus width transfer is shown in Figure 4. Due to the number of oscilloscope channels available, only four randomly selected receiver outputs (one from each bank of four) could be displayed at one time. As indicated in the figure, t_{VALID} equaled 0.4 t_{UI} at a t_{UI} of 2.86 ns. By definition, this value supports a maximum parallel transfer rate of 350 Mxfers/s. The results for this and the other bus widths are summarized in Table 1.

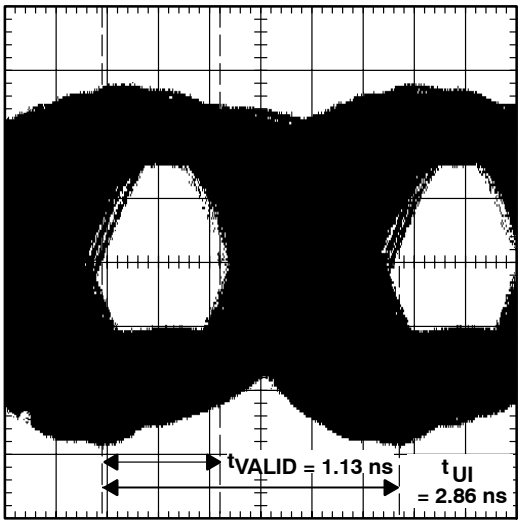


Figure 4. Overlay of Four Receiver Outputs of a 16-Circuit Random Data Transfer

Table 1. Maximum Data Transfer Rates for Various Bus Widths

NUMBER OF CIRCUITS	t_{UI} at t_{VALID}= 0.4 t_{UI}	MAXIMUM TRANSFER RATE
4	2.04 ns	490 Mxfers/s
8	2.17	460
12	2.78	360
16	2.86	350

5 Analysis

The example shows that the maximum signaling rate is higher than the maximum transfer rate and that the maximum transfer rate of a narrower bus is faster than wider bus widths. This section analyzes the causes for these phenomena.

5.1 The Components of Timing Error

When separate circuits are used, the responses of each circuit vary slightly. Some of these variations can be predicted from the specifications for data sheet parameters output skew, pulse skew, and part-to-part skew. (For definitions of these and other parameters, see reference 4). However, the degradation in the transfer rate seen in the example indicates other phenomena are involved.

It is reasonable to conclude that there is interaction between the circuits, because the only variable introduced between experiments was bus width. This phenomenon is known as crosstalk and is a common in multichannel high-speed circuits. This and other noise-induced timing errors are classified under the general category of jitter and are properly characterized using statistical techniques. A more conservative approach was used in the example by capturing the peak time displacement, regardless of its relationship to the other signals across the bus.

Another deterministic error is the driver input voltage threshold tolerance. Voltages above or below this threshold cause the subsequent circuitry to indicate the logic state. It also defines the earliest or latest instant in time that the state may be sampled and processed. Since the signal voltages do not change instantly, an error is introduced if the voltage threshold varies between circuits.

5.2 Typical vs Worst-Case Transfer Rate

Derivation of a worst-case transfer rate for a particular interface circuit is difficult without actually building and testing it. It involves a summation of all of the worst-case timing errors and setting the circuit equal to 60% of the minimum unit interval. The worst-case timing error contributed by line circuits alone may be obtained by summing the specified worst-case pulse skew, output skew, part-to-part skew (if the circuits are spread among more than one IC), and an estimate of jitter.

For our example, the data sheets for SN65LVDS387 and SN65LVDS386 specify maximum pulse skews of 500 ps and 600 ps, output skews of 150 ps and 400 ps, and part-to-part skews of 1500 ps and 1000 ps, respectively. Ignoring jitter for the moment, the sum of all these skews is 4.15 ns, indicating a minimum unit interval of 4.15 ns/0.6 or maximum transfer rate of 144 Mxfers/s. If all of the circuits are integrated on the same substrate, the part-to-part skew is eliminated and the maximum worst-case transfer rate increases to 364 Mxfers/s. This is why wide line circuits are useful.

An estimate for worst-case jitter must be empirically derived. Figure 5 shows the total jitter at the receiver output of the example test setup. Since the graphed values are of total jitter, it includes both deterministic and nondeterministic timing error. The deterministic error has already been accounted for, and, assuming the jitter for one circuit at 200 Mbps is primarily from fixed errors, this value is used as the base for determining signaling-rate and number-of-circuit dependent jitter.

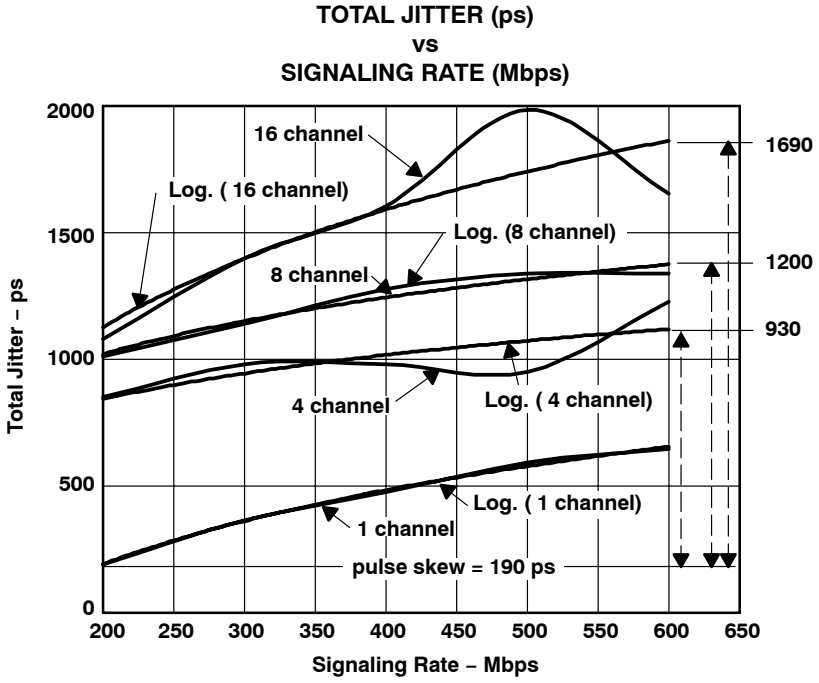


Figure 5. Jitter vs Signaling Rate and Number of Channels

Using the trended data and the worst-case difference in the curves gives nondeterministic jitter estimates of 930 ps, 1200 ps, and 1690 ps for 4-, 8-, and 16-circuit operation. The worst-case timing error is now estimated as the sum of the maximum specified timing errors and the random jitter from the example test setup at 600 Mxfers/s for four, eight, and sixteen circuits in operation. Foregoing the math details and, again, eliminating part-to-part skew gives a worst-case transfer rate of 232 Mxfers/s for 4, 210 Mxfers/s for 8, and 179 Mxfers/s for 16 circuits in operation.

6 Conclusion

Many different parameters and units are used to describe the performance of data interface circuits. Much confusion and disagreement can be avoided with a common set of definitions. The signaling rate of a data interface circuit is defined as the number of state changes per unit time while meeting a minimum signal quality criteria. Signaling rate is expressed in bits per second. The parallel transfer rate describes the performance of parallel interface circuits. Transfer rate includes timing uncertainty or error and is necessarily lower than the maximum signaling rate. Transfer rate is expressed in transfers per second.

For example, application of these definitions to the interface circuit of a SN65LVDS387 and SN65LVDS386 16-channel LVDS driver and receiver produced a maximum signaling rate of 682 Mbps. Deterministic and random timing error, in the example, limit data transfer rates to 490 Mxfers/s, 460 Mxfers/s, 360 Mxfers/s, and 350 Mxfers/s for 4, 8, 12, and 16 circuits, respectively. The worst-case maximum transfer rate over temperature, supply voltage, and process was conservatively estimated at 232 Mxfers/s, 210 Mxfers/s, and 179 Mxfers/s for 4, 8, and 16 circuits, respectively.

7 References

1. SLLS362, Data Sheet, *SN65LVDS387 16-Channel High-Speed Differential Line Driver*
2. SLLS394, Data Sheet, *SN65LVDS386 16-Channel High-Speed Differential Line Receiver*
3. TIA/EIA−644, *Electrical Characteristics of Low Voltage Differential (LVDS) Interface Circuits*
4. EIA/JESD65*, Definition of Skew Specifications for Standard Logic Devices.*

Appendix A Measurement Setup

For the measurements, several configurations have been set up with from one to sixteen channels running. The SN65LVDS387 and SN65LVDS386 evaluation boards were used. For a detailed description of these boards, consult the application report *16-Channel LVDS Driver/Receiver Evaluation Module* (#SLLU013).

The interconnecting cable was 0.5 m of twisted-pair ribbon cable. A pseudorandom bit sequence (PRBS) with a depth of 64KB was applied by the Tektronix HFS9009 pattern generator. The jitter measurements were taken at the receiver output with a Tektronix oscilloscope TDS694 with a bandwidth of 3 GHz and active probes with a 4 GHz bandwidth (P6249). The figure below shows the setup.