Practical Consideration on Choosing a Crystal for CDCE(L)9xx Family

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ABSTRACT

This Application Note focuses on the explaination of the practical use of crystals with a CDCEx9xx device. No detailed knowledge about crystals is required. A more detailed explanation is found in the Application Note SCAA085.pdf "VCXO Application Guideline for CDCE(L)9xx Family".

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1 Crystal Parameters to be Considered

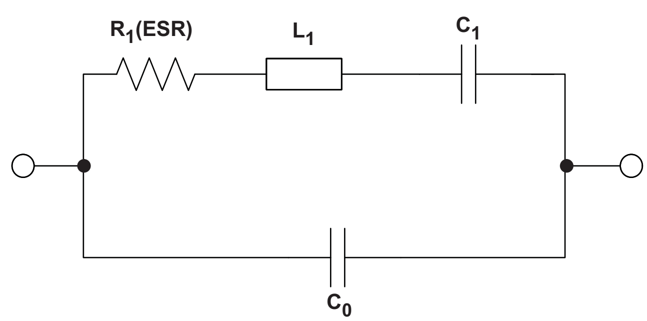

Figure 1. Equivalent Circuit of a Crystal

1.1 Crystal Load

The crystal load is one of the most basic parameters to be considered when selecting a crystal. The load capacitance is needed to build a working oscillation circuit. Therefore, it is used to fine tune the oscillation frequency. The CDCE9xx family offers build in load capacitance of up to 20pF selectable in steps of 1pF through the I^{2}C™ register 05h bits [7:3]. If a higher load is required, external capacitors can be used. Figure 2 shows the equivalent circuit of the CDCE9xx crystal stage attached to the crystal and possible external load capacitors. Possible load capacitors are switched in parallel to the internal capacitors, so the load capacitance is calculated as follows:

$$CL = \frac{CL_1 \times CL_2}{CL_1 + CL_2} \quad \text{where} \quad C_{Lx} = C_{Lxinternal} + C_{Lxexternal}\big|_{x=1,2} \tag{1}$$

I^{2}C is a trademark of Philips Electronics.

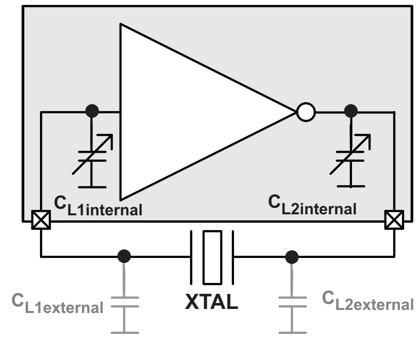

Figure 2. Equivalent Circuit of the CDCE9xx Crystal Stage With Attached Crystal and External Load Capacitors

1.2 Equivalent Series Resistance (ESR)

The ESR resembles the resistive losses of the crystal. Since the ESR attenuates a signal, it has to be overcome by the crystal stage of the attached device to start an oscillation. For the CDCE9xx Family, the maximum ESR that can be overcome is 100 Ω. Any ESR value below 100 Ω provides a stable oscillation.

Another effect of the ESR is the generation of heat due to resistive losses.

Every crystal has an absolute limit in terms of power dissipation. Exceeding this limit results in damage to the crystal, or in unwanted distortions or pertubations at the oscillation.

Besides this absolute limit, the crystal frequency drifts when the crystal is heated. In addition to the short term frequency drift, a heated crystal can age faster than a crystal at normally operation.

To reduce the heating, the crystal stage of the CDCE9xx family is specially designed for minimum heat dissipation. This means that the crystal stage itself controls the oscillation voltage to ensure an optimized working point for the crystal as well as for the crystal stage.

Therefore, a voltage measurement on the crystal or the crystal stage shows low amplitude by default. This low amplitude is intended and is normal. (see the *Measurements on the crystal* section)

The crystal stage of the CDCE9xx Family is designed to work with crystals with a maximum allowed power dissipation as low as 50µW. A crystal with maximum heat dissipation lower than 50µW can not be used. Crystals with higher maximum allowed power dissipation can be used.

1.3 Frequency

A CDCE9xx is designed to work with a crystal input frequency between 8MHz and 32MHz. It does not support 3rd overtone crystals.

1.4 Pullability

The device also supports VCXO operation. A crystal with maximum pullability should be selected. Since most vendors do not give information on the pullability of crystals on their web pages or catalogs, the vendors must be contacted for a specific crystal. To help in selecting the correct crystal for VCXO applications, the TIProClock Software for the CDCEx9xx devices has a built-in Pulling Range Calculator (under Tools/ Pulling Range calculator). For the software to work, the major parasitics of the crystal must be known. The Application Note SCAA085.pdf gives a more detailed introduction on the pullability of crystals.

2 Measurements on the Crystal

Measurements on the crystal stage are delicate and the results might not reflect the reality. If done, a probe with a high impedance and low paracitic capacitance (<0.1pF) should to be used. However, the parasitics of the probe changes the resonance frequency of the Oscillation circuit.

Measurements on the Xin Pin results in a collapse of the oscillation, only a DC signal is seen here.

Measurements on the Xout Pin usually show a low amplitude. (The reasons are explained in the Equivalent Series Resistance Section)

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