TLV320AIC3212 Applications

Reference Guide

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TLV320AIC3212 Overview

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Features

- Stereo Audio DAC with 101dB SNR
- 2.7mW Stereo 48 kHz DAC Playback
- Stereo Audio ADC with 93dB SNR
- 5.6mW Stereo 48 kHz ADC Record
- 8-192 kHz Playback and Record
- 30mW DirectPath™ Headphone Driver Eliminates Large Output DC-Blocking Capacitors
- 128mW Differential Receiver Output Driver
- Stereo Class-D Speaker Drivers
  - 1.7 W (8 Ω , 5.5 V, 10% THDN)
  - 1.4 W (8 Ω , 5.5 V, 1% THDN)
- Stereo Line Outputs
- PowerTune™ - Adjusts Power vs. SNR
- Extensive Signal Processing Options
- Eight Single-Ended or 4 Fully-Differential Analog Inputs
- Stereo Digital and Analog Microphone Inputs
- Low Power Analog Bypass Mode
- Programmable PLL, plus Low-Frequency Clocking
- Programmable 12-Bit SAR ADC
- SPI and I^2C Control Interfaces
- Three Independent Digital Audio Serial Interfaces
- 4.81 mm x 4.81 mm x 0.625 mm 81-Ball WCSP (YZF) Package

Applications

- Mobile Handsets
- Tablets/eBooks
- Portable Navigation Devices (PND)
- Portable Media Player (PMP)
- Portable Gaming Systems
- Portable Computing

The TLV320AIC3212 (sometimes referred to as the AIC3212) is a flexible, highly-integrated, low-power, low-voltage stereo audio codec with digital microphone inputs and programmable outputs, PowerTune capabilities, selectable audio-processing blocks, fixed predefined and parameterizable signal processing blocks, integrated PLL, and flexible digital audio interfaces. Extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application.

1.1 Description

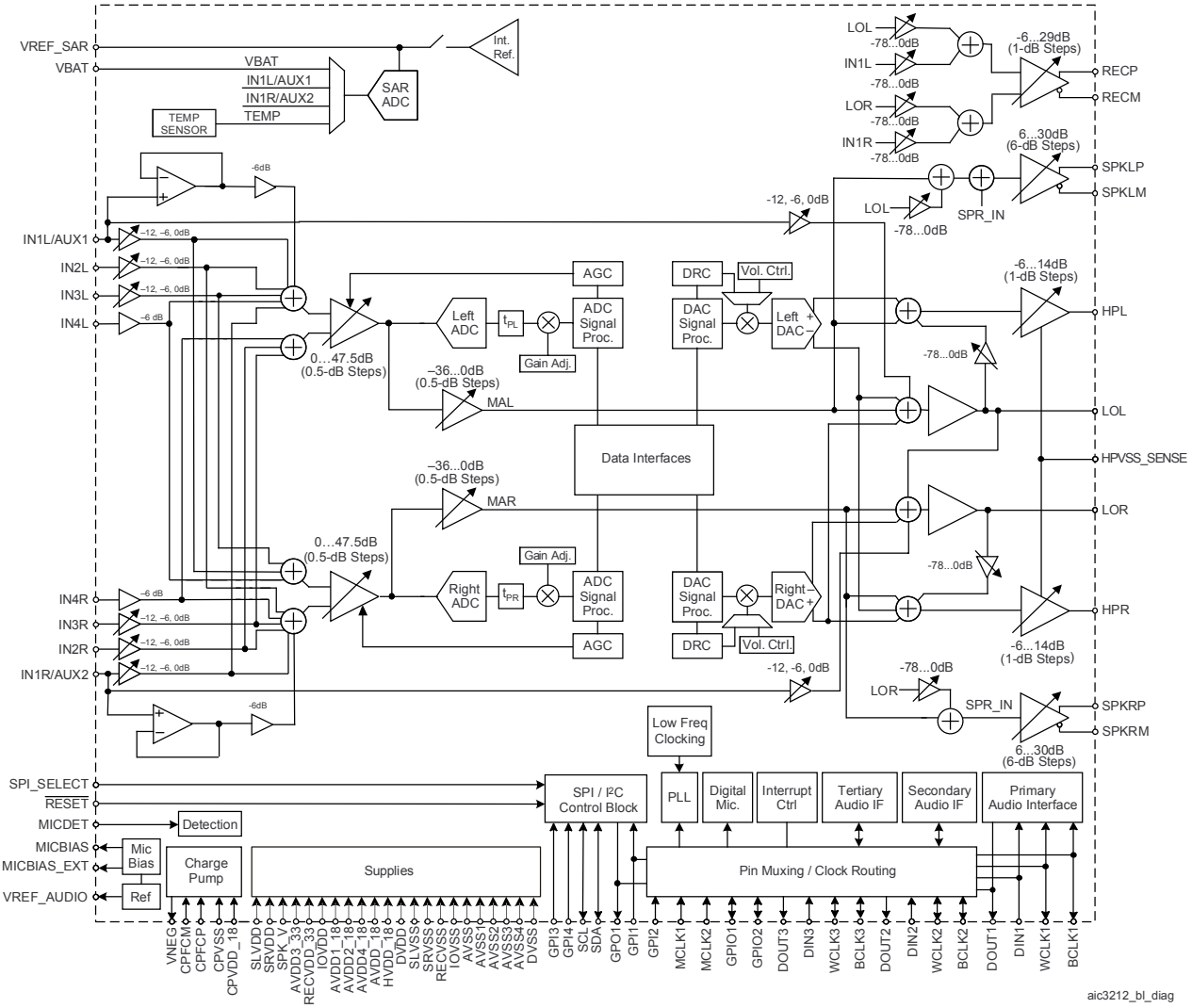


Figure 1-1. Simplified Block Diagram

Combined with the advanced PowerTune technology, the TLV320AIC3212 can operate from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The TLV320AIC3212 record path operates from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations supporting single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally-controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling, e.g. optical zooming in a digital camera. The record path can also be configured as a stereo digital microphone PDM interface typically used at 64Fs or 128Fs.

The playback path offers signal processing blocks for filtering and effects; headphone, line, receiver, and Class-D speaker outputs; flexible mixing of DAC; and analog input signals as well as programmable volume controls. The playback path contains two high-power headphone output drivers which eliminate the need for ac coupling capacitors. A built in charge pump generates the negative supply for the ground centered headphone drivers. These headphone output drivers can be configured in multiple ways, including stereo, and mono BTL. In addition, playback audio can be routed to integrated stereo Class-D speaker drivers or a differential receiver amplifier.

The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320AIC3212 can address both cases.

The required internal clock of the TLV320AIC3212 can be derived from multiple sources, including the MCLK1 pin, the MCLK2 pin, the BCLK1 pin, the BCLK2 pin, several general purpose I/O pins or the output of the internal PLL, where the input to the PLL again can be derived from similar pins. Although using the internal fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz. To enable even lower clock frequencies, an integrated low-frequency clock multiplier can also be used as an input to the PLL.

The TLV320AIC3212 has a 12-bit SAR ADC converter that supports system voltage measurements. These system voltage measurements can be fed from three dedicated analog inputs (IN1L, IN1R, or VBAT pins), or, alternatively, an on-chip temperature sensor that can be read by the SAR ADC.

The TLV320AIC3212 also features three full Digital Audio Serial Interfaces, each supporting I2S, DSP/TDM, RJF, LJF, and mono PCM formats. This enables the digital playback (DAC) and record (ADC) paths to select from three independent digital audio buses or chips.

The device is available in the 4.81 mm x 4.81 mm x 0.625 mm 81-Ball WCSP (YZF) Package.

1.2 Typical Circuit Configuration

Figure 1-2 shows a typical circuit configuration for a system utilizing TLV320AIC3212. Note that while this circuit configuration shows all three Audio Serial Interfaces connected to a single Host Processor, it is also quite common for these Audio Serial Interfaces to connect to separate devices (e.g. Host Processor on Audio Serial Interface #1, and modems and/or Bluetooth devices on the other audio serial interfaces).

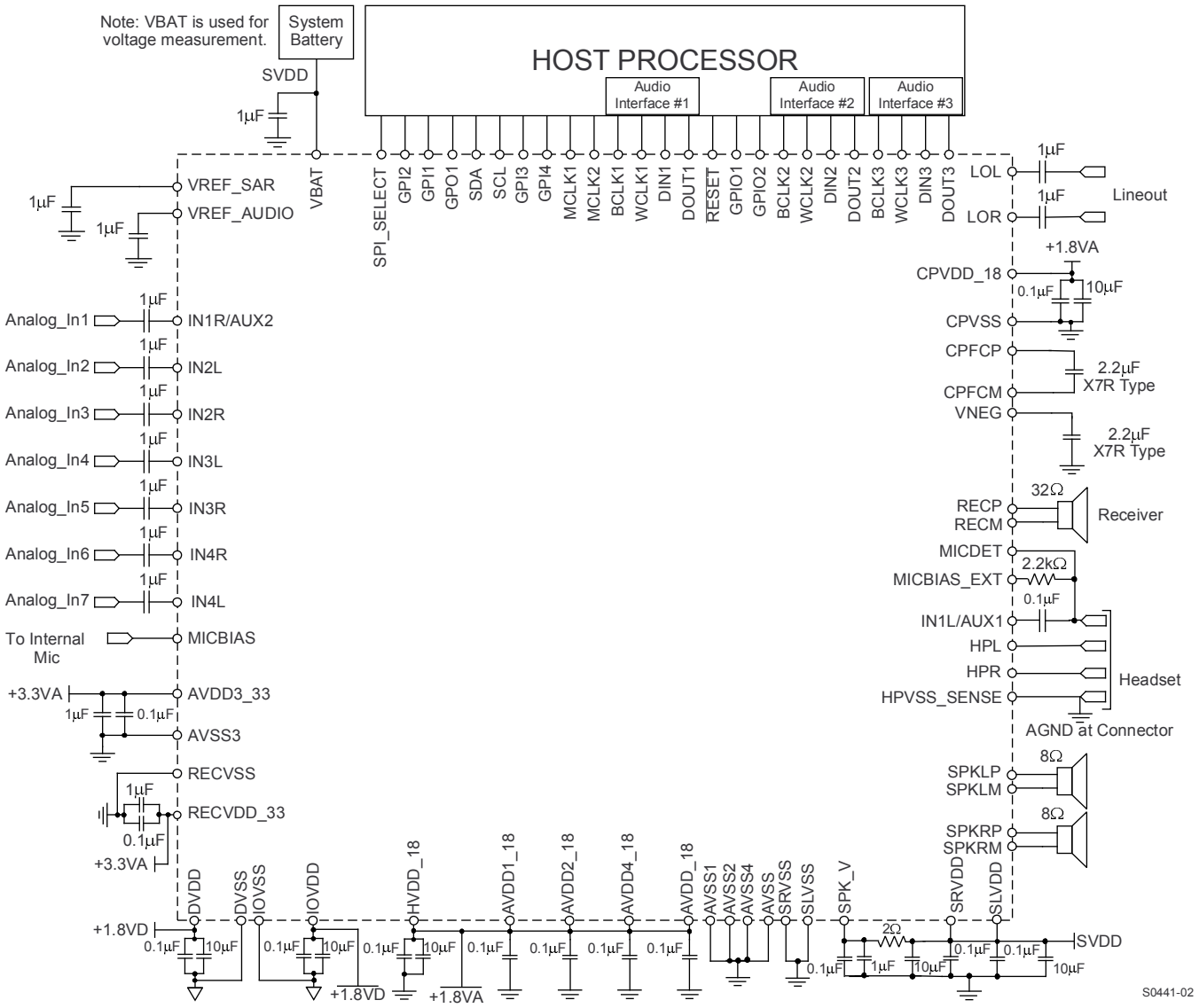


Figure 1-2. Typical Circuit Configuration

TLV320AIC3212 Application

2.1 Nomenclature

Throughout this document, references to registers for controlling the TLV320AIC3212 will utilize the following abbreviations:

Table 2-1. Abbreviations for Register References

Reference	Abbreviation	Description	Example
Book x, Page y, Register z, Bit k	Bx_Py_Rz_Dk	Single Data Bit - Refers the value of a single bit in a register	Book 0, Page 4, Register 36, Bit 0 = B0_P4_R36_D0
Book x, Page y, Register z, Bits k-m	Bx_Py_Rz_D[k:m]	Range of Data Bits - Refers to a range of data bits (inclusive)	Book 0, Page 4, Register 36, Bits 3, 2, 1, 0 = B0_P4_R36_D[3:0]
Book x, Page y, Register z	Bx_Py_Rz	One Whole Register - Refers to all eight bits in the register as a unit	Book 0, Page 4, Register 36 = B0_P4_R36
Book x, Page y, Registers z-n	Bx_Py_Rz-Rn	Range of Registers - Refers to a range of registers in the same book and page	Book 0, Page 4, Registers 36, 37, 38 = B0_P4_R36-R38

2.2 Terminal Descriptions

2.2.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are hardware-control pins $\overline{\text{RESET}}$ and SPI_SELECT pin. Depending on the state of SPI_SELECT, four pins SCL, SDA, GPO1, and GPI1 are configured for either I^2C or SPI protocol. Only in I^2C mode, GPI3 and GPI4 provide four possible I^2C addresses for the TLV320AIC3212.

Other digital IO pins can be configured for various functions via register control.

2.2.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

The possible analog routings of analog input pins to ADCs and output amplifiers as well as the routing from DACs to output amplifiers can be seen in the Analog Routing Diagram.

2.2.3 Multifunction Pins

Table 2-2 show the possible allocation of pins for specific functions.

Table 2-2. Multifunction Pin Assignments for Pins MCLK1, MCLK2, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2

		1	2	3	4	5	6	7	8	9	10
	Pin Function	**MCLK 1**	**MCLK 2**	**WCLK1**	**BCLK1**	**DIN1**	**DOUT1**	**WCLK2**	**BCLK2**	**DIN2**	**DOUT2**
A	INT1 Output						E	E	E		E
B	INT2 Output						E	E	E		E
C	SAR ADC Interrupt						E	E	E		E
D	CLOCKOUT Output			E			E	E	E		
E	ADC_MOD_CLOCK Output							E	E		E
F	Single DOUT for ASI1						E, D				
F	Single DOUT for ASI2										E, D
F	Single DOUT for ASI3										
I	General Purpose Output (via Reg)						E[1]	E	E		E
F	Single DIN for ASI1					E, D[2]					
F	Single DIN for ASI2									E, D	
F	Single DIN for ASI3										
J	Digital Mic Data		E			E				E	

(1) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if DOUT1 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time)

(2) D: Default Function

Table 2-2. Multifunction Pin Assignments for Pins MCLK1, MCLK2, WCLK1, BCLK1, DIN1, DOUT1, WCLK2, BCLK2, DIN2, and DOUT2 (continued)

		1	2	3	4	5	6	7	8	9	10
	Pin Function	**MCLK 1**	**MCLK 2**	**WCLK1**	**BCLK1**	**DIN1**	**DOUT1**	**WCLK2**	**BCLK2**	**DIN2**	**DOUT2**
K	Input to PLL_CLKIN	S(3), D	S		S(4)	S			S(4)		
L	Input to ADC_CLKIN	S(3), D	S		S(4)				S(4)		
M	Input to DAC_CLKIN	S(3), D	S		S(4)				S(4)		
N	Input to CDIV_CLKIN	S(3), D	S		S	S			S		
O	Input to LFR_CLKIN	S(3), D	S	S				S	S	S	
P	Input to HF_CLK	S(3)									
Q	Input to REF_1MHz_CLK	S(3)									
R	General Purpose Input (via Reg)					E		E	E	E	
T	WCLK Output for ASI1			E							
U	WCLK Input for ASI1			S, D							
V	BCLK Output for ASI1				E						
W	BCLK Input for ASI1				S(4), D						
X	WCLK Output for ASI2							E			
Y	WCLK Input for ASI2							S, D			
Z	BCLK Output for ASI2								E		
AA	BCLK Input for ASI2								S(4), D		
BB	WCLK Output for ASI3										
CC	WCLK Input for ASI3										
DD	BCLK Output for ASI3										
EE	BCLK Input for ASI3										

(3) S(3): The MCLK1 pin could be chosen to drive the PLL, ADC Clock, DAC Clock, CDIV Clock, LFR Clock, HF Clock, and REF_1MHz_CLK inputs **simultaneously**

(4) S(4): The BCLK1 or BCLK2 pins could be chosen to drive the PLL, ADC Clock, DAC Clock, and audio interface bit clock inputs **simultaneously**

Table 2-3. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4

		11	12	13	14	15	16	17	18	19	20	21
	Pin Function	**WCLK 3**	**BCLK 3**	**DIN3**	**DOUT 3**	**GPIO1**	**GPIO2**	**GPO1/ MISO (1)**	**GPI1/ SCLK (1)**	**GPI2**	**GPI3 (2)**	**GPI4 (2)**
A	INT1 Output					E	E	E				
B	INT2 Output					E	E	E				
C	SAR ADC Interrupt					E	E	E				
D	CLOCKOUT Output					E	E	E				
E	ADC_MOD_CLOCK Output					E	E	E				
F	Single DOUT for ASI1							E				
F	Single DOUT for ASI2											
F	Single DOUT for ASI3				E, D							

(1) GPO1 and GPI1 can only be utilized for functions defined in this table when part utilizes I^2C for control. In SPI mode, these pins serve as the MISO and SCLK, respectively.

(2) GPI3 and GPI4 can only be utilized for functions defined in this table when part utilizes SPI for control. In I^2C mode, these pins serve as I^2C address pins.

Table 2-3. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4 (continued)

		11	12	13	14	15	16	17	18	19	20	21
	Pin Function	**WCLK 3**	**BCLK 3**	**DIN3**	**DOUT 3**	**GPIO1**	**GPIO2**	**GPO1/ MISO (1)**	**GPI1/ SCLK (1)**	**GPI2**	**GPI3 (2)**	**GPI4 (2)**
I	General Purpose Output (via Reg)	E(3)	E		E	E	E	E				
F	Single DIN for ASI1									E		
F	Single DIN for ASI2											
F	Single DIN for ASI3			E, D								
J	Digital Mic Data					E	E		E	E		
K	Input to PLL_CLKIN					S(4)	S(4)		S(4)	S(4)		
L	Input to ADC_CLKIN					S(4)	S(4)		S(4)	S(4)		
M	Input to DAC_CLKIN					S(4)	S(4)		S(4)	S(4)		
N	Input to CDIV_CLKIN								S	S		
O	Input to LFR_CLKIN	S	S			S	S		S	S		
P	Input to HF_CLK											
Q	Input to REF_1MHz_CLK											
R	General Purpose Input (via Reg)	E	E	E		E	E		E	E		
T	WCLK Output for ASI1				E	E						
U	WCLK Input for ASI1					E						
V	BCLK Output for ASI1						E					
W	BCLK Input for ASI1						E					
X	WCLK Output for ASI2											
Y	WCLK Input for ASI2											
Z	BCLK Output for ASI2											
AA	BCLK Input for ASI2											
BB	WCLK Output for ASI3	E										
CC	WCLK Input for ASI3	S, D(5)										
DD	BCLK Output for ASI3		E									
EE	BCLK Input for ASI3		S, D									
FF	ADC BCLK Input for ASI1					E	E		E	E	E	E
GG	ADC WCLK Input for ASI1					E	E		E	E	E	E
HH	ADC BCLK Output for ASI1					E	E					
II	ADC WCLK Output for ASI1					E	E					
JJ	ADC BCLK Input for ASI2					E	E		E	E	E	E
KK	ADC WCLK Input for ASI2					E	E		E	E	E	E

(3) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin (e.g. if WCLK3 has been allocated for General Purpose Output, it cannot be used as the ASI3 WCLK output at the same time)

(4) S(4): The GPIO1, GPIO2, GPI1, or GPI2 pins could be chosen to drive the PLL, ADC Clock, and DAC Clock inputs **simultaneously**

(5) D: Default Function

Table 2-3. Multifunction Pin Assignments for Pins WCLK3, BCLK3, DIN3, DOUT3, GPIO1, GPIO2, GPO1, GPI1, GPI2, GPI3, and GPI4 (continued)

		11	12	13	14	15	16	17	18	19	20	21
	Pin Function	**WCLK 3**	**BCLK 3**	**DIN3**	**DOUT 3**	**GPIO1**	**GPIO2**	**GPO1/ MISO (1)**	**GPI1/ SCLK (1)**	**GPI2**	**GPI3 (2)**	**GPI4 (2)**
LL	ADC BCLK Output for ASI2					E	E					
MM	ADC WCLK Output for ASI2					E	E					
NN	ADC BCLK Input for ASI3					E	E		E	E	E	E
OO	ADC WCLK Input for ASI3					E	E		E	E	E	E
PP	ADC BCLK Output for ASI3					E	E					
QQ	ADC WCLK Output for ASI3					E	E					

2.2.3.1 Register Settings for Multifunction Pins

Table 2-4 summarizes the register settings that must be applied to configure the pin assignments for general inputs and outputs, interrupts, clocking outputs, and digital microphones. In Table 2-4, the letter/number combination represents the row and the column number from Table 2-2 and Table 2-3 in bold type.

Please be aware that more settings may be necessary to obtain a full functionality matching the application requirement.

Table 2-4. Multifunction Pin Register Configuration - General Inputs/Outputs, Interrupts, Clocking Outputs, Digital Microphones

	Description	Required Register Setting		Description	Required Register Setting
A6	INT1 Output on DOUT1	B0_P4_R67_D[4:1]=0100	I6	General Purpose Output on DOUT1	B0_P4_R67_D[4:1]=0010
A7	INT1 Output on WCLK2	B0_P4_R69_D[5:2]=0101	I7	General Purpose Output on WCLK2	B0_P4_R69_D[5:2]=0011
A8	INT1 Output on BCLK2	B0_P4_R70_D[5:2]=0101	I8	General Purpose Output on BCLK2	B0_P4_R70_D[5:2]=0011
A10	INT1 Output on DOUT2	B0_P4_R71_D[4:1]=0100	I10	General Purpose Output on DOUT2	B0_P4_R71_D[4:1]=0010
A15	INT1 Output on GPIO1	B0_P4_R86_D[6:2]=00101	I11	General Purpose Output on WCLK3	B0_P4_R73_D[5:2]=0011
A16	INT1 Output on GPIO2	B0_P4_R87_D[6:2]=00101	I12	General Purpose Output on BCLK3	B0_P4_R74_D[5:2]=0011
A17	INT1 Output on GPO1	B0_P4_R96_D[4:1]=0100	I14	General Purpose Output on DOUT3	B0_P4_R75_D[4:1]=0010
B6	INT2 Output on DOUT1	B0_P4_R67_D[4:1]=0101	I15	General Purpose Output on GPIO1	B0_P4_R86_D[6:2]=00011
B7	INT2 Output on WCLK2	B0_P4_R69_D[5:2]=0110	I16	General Purpose Output on GPIO2	B0_P4_R87_D[6:2]=00011
B8	INT2 Output on BCLK2	B0_P4_R70_D[5:2]=0110	I17	General Purpose Output on GPO1	B0_P4_R96_D[4:1]=0010
B10	INT2 Output on DOUT2	B0_P4_R71_D[4:1]=0101	J2	Digital Mic Data on MCLK2	B0_P4_R82_D[5:4]=01; B0_P4_R101_D[4:0]=0011 0 or 01100 or 10001 or 10101 or 110x0 or 11011
B15	INT2 Output on GPIO1	B0_P4_R86_D[6:2]=00110	J5	Digital Mic Data on DIN1	B0_P4_R68_D[6:5]=01; B0_P4_R101_D[4:0] =00010 or 01000 or 01101 or 1001x or 1010x
B16	INT2 Output on GPIO2	B0_P4_R87_D[6:2]=00110	J9	Digital Mic Data on DIN2	B0_P4_R72_D[6:5]=01; B0_P4_R101_D[4:0]=0001 1 or 01110 or 01001 or 10010 or 1011x or 11000
B17	INT2 Output on GPO1	B0_P4_R96_D[4:1]=0101	J15	Digital Mic Data on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R101_D[4:0]=0010 0 or 01111 or 01010 or 10011 or 10110 or 11001 or 11010
C6	SAR ADC Interrupt on DOUT1	B0_P4_R67_D[4:1]=0110	J16	Digital Mic Data on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R101_D[4:0]=0010 1 or 01011 or 10000 or 10100 or 10111 or 11001 or 11011
C7	SAR ADC Interrupt on WCLK2	B0_P4_R69_D[5:2]=1100	J18	Digital Mic Data on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R101_D[4:0]=0000 0 or 00111 or 0100x or 0101x or 01100

Table 2-4. Multifunction Pin Register Configuration - General Inputs/Outputs, Interrupts, Clocking Outputs, Digital Microphones (continued)

	Description	Required Register Setting		Description	Required Register Setting
C8	SAR ADC Interrupt on BCLK2	B0_P4_R70_D[5:2]=1100	J19	Digital Mic Data on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R101_D[4:0]=0000 1 or 0111x or 00111 or 01101 or 1000x
C10	SAR ADC Interrupt on DOUT2	B0_P4_R71_D[4:1]=0110	R5	General Purpose Input on DIN1	B0_P4_R68_D[6:5]=01
C15	SAR ADC Interrupt on GPIO1	B0_P4_R86_D[6:2]=01100	R7	General Purpose Input on WCLK2	B0_P4_R69_D[5:2]=0010
C16	SAR ADC Interrupt on GPIO2	B0_P4_R87_D[6:2]=01100	R8	General Purpose Input on BCLK2	B0_P4_R70_D[5:2]=0010
C17	SAR ADC Interrupt on GPO1	Pg 4, Reg 96, D(4:1)=1100	R5	General Purpose Input on DIN1	B0_P4_R68_D[6:5]=01
D3	CLOCKOUT Output on WCLK1	B0_P4_R65_D[5:2]=0100	R9	General Purpose Input on DIN2	B0_P4_R72_D[6:5]=01
D6	CLOCKOUT Output on DOUT1	B0_P4_R67_D[4:1]=0011	R13	General Purpose Input on DIN3	B0_P4_R76_D[6:5]=01
D7	CLOCKOUT Output on WCLK2	B0_P4_R69_D[5:2]=0100	R11	General Purpose Input on WCLK3	B0_P4_R73_D[5:2]=0010
D8	CLOCKOUT Output on BCLK2	B0_P4_R70_D[5:2]=0100	R12	General Purpose Input on BCLK3	B0_P4_R74_D[5:2]=0010
D15	CLOCKOUT Output on GPIO1	B0_P4_R86_D[6:2]=00100; B0_P4_R10_D[7:5]≠011	R13	General Purpose Input on DIN3	B0_P4_R76_D[6:5]=01
D16	CLOCKOUT Output on GPIO2	B0_P4_R87_D[6:2]=00100; B0_P4_R10_D[4:2]≠011	R15	General Purpose Input on GPIO1	B0_P4_R86_D[6:2]=00001
D17	CLOCKOUT Output on GPO1	B0_P4_R96_D[4:1]=0011	R16	General Purpose Input on GPIO2	B0_P4_R87_D[6:2]=00001
E7	ADC_MOD_CLOCK Output on WCLK2	B0_P4_R69_D[5:2]=1010	R18	General Purpose Input on GPI1	B0_P4_R91_D[2:1]=01
E8	ADC_MOD_CLOCK Output on BCLK2	B0_P4_R70_D[5:2]=1010	R19	General Purpose Input on GPI2	B0_P4_R92_D[5:4]=01
E10	ADC_MOD_CLOCK Output on DOUT2	B0_P4_R71_D[4:1]=1010			
E15	ADC_MOD_CLOCK Output on GPIO1	B0_P4_R86_D[6:2]=01010			
E16	ADC_MOD_CLOCK Output on GPIO2	B0_P4_R87_D[6:2]=01010			
E17	ADC_MOD_CLOCK Output on GPO1	B0_P4_R96_D[4:1]=0111			

Table 2-5 summarizes the register settings that must be applied to configure the pin assignments for clocking inputs to the device. In Table 2-5, the letter/number combination represents the row and the column number from Table 2-2 and Table 2-3 in bold type.

Please be aware that more settings may be necessary to obtain a full functionality matching the application requirement.

Table 2-5. Multifunction Pin Register Configuration - Clocking Inputs

	Description	Required Register Setting		Description	Required Register Setting
K1	Input to PLL_CLKIN from MCLK1	B0_P0_R5_D[5:2]=0000	N1	Input to CDIV_CLKIN from MCLK1	B0_P0_R21_D[3:0]=0000
K2	Input to PLL_CLKIN from MCLK2	B0_P0_R5_D[5:2]=1001; B0_P4_R82_D[5:4]=01	N2	Input to CDIV_CLKIN from MCLK2	B0_P0_R21_D[3:0]=1100; B0_P4_R82_D[5:4]=01
K4	Input to PLL_CLKIN from BCLK1	B0_P0_R5_D[5:2]=0001	N4	Input to CDIV_CLKIN from BCLK1	B0_P0_R21_D[3:0]=0001

Table 2-5. Multifunction Pin Register Configuration - Clocking Inputs (continued)

	Description	Required Register Setting		Description	Required Register Setting
K5	Input to PLL_CLKIN from DIN1	B0_P0_R5_D[5:2]=0011; B0_P4_R68_D[6:5]=01	N5	Input to CDIV_CLKIN from DIN1	B0_P0_R21_D[3:0]=0010; B0_P4_R68_D[6:5]=01
K8	Input to PLL_CLKIN from BCLK2	B0_P0_R5_D[5:2]=0100; B0_P4_R70_D[5:2]=0010	N8	Input to CDIV_CLKIN from BCLK2	B0_P0_R21_D[3:0]=1000; B0_P4_R70_D[5:2]=0010
K15	Input to PLL_CLKIN from GPIO1	B0_P0_R5_D[5:2]=0010; B0_P4_R86_D[6:2]=00001	N18	Input to CDIV_CLKIN from GPI1	B0_P0_R21_D[3:0]=1001; B0_P4_R91_D[2:1]=01
K16	Input to PLL_CLKIN from GPIO2	B0_P0_R5_D[5:2]=0111; B0_P4_R87_D[6:2]=00001	N19	Input to CDIV_CLKIN from GPI2	B0_P0_R21_D[3:0]=1101; B0_P4_R92_D[5:4]=01
K18	Input to PLL_CLKIN from GPI1	B0_P0_R5_D[5:2]=0101; B0_P4_R91_D[2:1]=01	O1	Input to LFR_CLKIN from MCLK1	B0_P0_R24_D[7:4]=0000
K19	Input to PLL_CLKIN from GPI2	B0_P0_R5_D[5:2]=1000; B0_P4_R92_D[5:4]=01	O2	Input to LFR_CLKIN from MCLK2	B0_P0_R24_D[7:4]=0111; B0_P4_R82_D[5:4]=01
L1	Input to ADC_CLKIN from MCLK1	B0_P0_R4_D[3:0]=0000	O3	Input to LFR_CLKIN from WCLK1	B0_P0_R24_D[7:4]=0001
L2	Input to ADC_CLKIN from MCLK2	B0_P0_R4_D[3:0]=1000; B0_P4_R82_D[5:4]=01	O7	Input to LFR_CLKIN from WCLK2	B0_P0_R24_D[7:4]=0011; B0_P4_R69_D[5:2]=0010
L4	Input to ADC_CLKIN from BCLK1	B0_P0_R4_D[3:0]=0001	O8	Input to LFR_CLKIN from BCLK2	B0_P0_R24_D[7:4]=0100; B0_P4_R70_D[5:2]=0010
L8	Input to ADC_CLKIN from BCLK2	B0_P0_R4_D[3:0]=0100; B0_P4_R70_D[5:2]=0010	O9	Input to LFR_CLKIN from DIN2	B0_P0_R24_D[7:4]=0110; B0_P4_R72_D[6:5]=01
L15	Input to ADC_CLKIN from GPIO1	B0_P0_R4_D[3:0]=0010; B0_P4_R86_D[6:2]=00001	O11	Input to LFR_CLKIN from WCLK3	B0_P0_R24_D[7:4]=1010; B0_P4_R73_D[5:2]=0010
L16	Input to ADC_CLKIN from GPIO2	B0_P0_R4_D[3:0]=1001; B0_P4_R87_D[6:2]=00001	O12	Input to LFR_CLKIN from BCLK3	B0_P0_R24_D[7:4]=1011; B0_P4_R74_D[5:2]=0010
L18	Input to ADC_CLKIN from GPI1	B0_P0_R4_D[3:0]=0101; B0_P4_R91_D[2:1]=01	O15	Input to LFR_CLKIN from GPIO1	B0_P0_R24_D[7:4]=0010; B0_P4_R86_D[6:2]=00001
L19	Input to ADC_CLKIN from GPI2	B0_P0_R4_D[3:0]=1010; B0_P4_R92_D[5:4]=01	O16	Input to LFR_CLKIN from GPIO2	B0_P0_R24_D[7:4]=1000; B0_P4_R87_D[6:2]=00001
M1	Input to DAC_CLKIN from MCLK1	B0_P0_R4_D[7:4]=0000	O18	Input to LFR_CLKIN from GPI1	B0_P0_R24_D[7:4]=0101; B0_P4_R91_D[2:1]=01
M2	Input to DAC_CLKIN from MCLK2	B0_P0_R4_D[7:4]=1000; B0_P4_R82_D[5:4]=01	O19	Input to LFR_CLKIN from GPI2	B0_P0_R24_D[7:4]=1001; B0_P4_R92_D[5:4]=01
M4	Input to DAC_CLKIN from BCLK1	B0_P0_R4_D[7:4]=0001	P1	Input to HF_CLK from MCLK1	B0_P0_R24_D[3:0]=0000
M8	Input to DAC_CLKIN from BCLK2	B0_P0_R4_D[7:4]=0100; B0_P4_R70_D[5:2]=0010	Q1	Input to REF_1MHz_CLK from MCLK1	B0_P0_R23_D7=1
M15	Input to DAC_CLKIN from GPIO1	B0_P0_R4_D[7:4]=0010; B0_P4_R86_D[6:2]=00001			
M16	Input to DAC_CLKIN from GPIO2	B0_P0_R4_D[7:4]=1001; B0_P4_R87_D[6:2]=00001			
M18	Input to DAC_CLKIN from GPI1	B0_P0_R4_D[7:4]=0101; B0_P4_R91_D[2:1]=01			
M19	Input to DAC_CLKIN from GPI2	B0_P0_R4_D[7:4]=1010; B0_P4_R92_D[5:4]=01			

Table 2-6 summarizes the register settings that must be applied to configure the pin assignments for the audio serial interfaces. In Table 2-6, the letter/number combination represents the row and the column number from Table 2-2 and Table 2-3 in bold type.

Please be aware that more settings may be necessary to obtain a full audio serial interface definition matching the application requirement (e.g. B0_P4_R1-R16 for Audio Serial Interface #1, B0_P4_R17-R32 for Audio Serial Interface #2, and B0_P4_R33-R48 for Audio Serial Interface #3).

Table 2-6. Multifunction Pin Register Configuration - Audio Serial Interfaces

	Description	Required Register Setting		Description	Required Register Setting
F6	Single Stereo ASI1 DOUT on DOUT1	B0_P4_R67_D[4:1]=0001; B0_P4_R6_D[3:0]=0000; B0_P4_R6_D7=0	HH15	ASI1 ADC BCLK Output on GPIO1	B0_P4_R86_D[6:2]=10001; B0_P4_R16_D[2:0]=001
F5	Single Stereo ASI1 DIN on DIN1	B0_P4_R68_D[6:5]=01; B0_P4_R5_D[4:0]=00000; B0_P4_R6_D7=0; B0_P4_R118_D[5:4]=00	HH16	ASI1 ADC BCLK Output on GPIO2	B0_P4_R87_D[6:2]=10001; B0_P4_R16_D[2:0]=010
F17	Single Stereo ASI1 DOUT on GPO1	B0_P4_R96_D[4:1]=1111; B0_P4_R6_D[3:0]=1100; B0_P4_R6_D7=0	II15	ASI1 ADC WCLK Output on GPIO1	B0_P4_R86_D[6:2]=10000; B0_P4_R16_D[6:4]=001
F19	Single Stereo ASI1 DIN on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R5_D[4:0]=01011; B0_P4_R6_D7=0	II16	ASI1 ADC WCLK Output on GPIO2	B0_P4_R87_D[6:2]=10000; B0_P4_R16_D[6:4]=010
F9	Single Stereo ASI2 DIN on DIN2	B0_P4_R72_D[6:5]=01; B0_P4_R24_D[7:4]=0101; B0_P4_R118_D[3:2]=01	JJ15	ASI2 ADC BCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R32_D[2:0]=001
F10	Single Stereo ASI2 DOUT on DOUT2	B0_P4_R71_D[4:1]=0001; B0_P4_R23_D[2:0]=101	JJ16	ASI2 ADC BCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R32_D[2:0]=010
F13	Single Stereo ASI3 DIN on DIN3	B0_P4_R76_D[6:5]=01; B0_P4_R40_D[7:4]=0101; B0_P4_R118_D[1:0]=10	JJ18	ASI2 ADC BCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R32_D[2:0]=011
F14	Single Stereo ASI3 DOUT on DOUT3	B0_P4_R75_D[4:1]=0001; B0_P4_R39_D[2:0]=110	JJ19	ASI2 ADC BCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R32_D[2:0]=100
T3	ASI1 WCLK Output on WCLK1	B0_P4_R65_D[5:2]=0001; B0_P4_R10_D[7:5]=001	JJ20	ASI2 ADC BCLK Input on GPI3	SPI Mode Only; B0_P4_R32_D[2:0]=101
T14	ASI1 WCLK Output on DOUT3	B0_P4_R75_D[4:1]=1110; B0_P4_R10_D[7:5]=100	JJ21	ASI2 ADC BCLK Input on GPI4	SPI Mode Only; B0_P4_R32_D[2:0]=110
T15	ASI1 WCLK Output on GPIO1	B0_P4_R86_D[6:2]=00100; B0_P4_R10_D[7:5]=011	KK15	ASI2 ADC WCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R32_D[6:4]=001
U3	ASI1 WCLK Input on WCLK1	B0_P4_R65_D[5:2]=0001; B0_P4_R10_D[7:5]=000	KK16	ASI2 ADC WCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R32_D[2:0]=010
U15	ASI1 WCLK Input on GPIO1	B0_P4_R86_D[6:2]=00100; B0_P4_R10_D[7:5]=010	KK18	ASI2 ADC WCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R32_D[6:4]=011
V4	ASI1 BCLK Output on BCLK1	B0_P4_R10_D[4:2]=001	KK19	ASI2 ADC WCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R32_D[6:4]=100
V16	ASI1 BCLK Output on GPIO2	B0_P4_R87_D[6:2]=00100; B0_P4_R10_D[4:2]=011	KK20	ASI2 ADC WCLK Input on GPI3	SPI Mode Only; B0_P4_R32_D[6:4]=101
W4	ASI1 BCLK Input on BCLK1	B0_P4_R10_D[4:2]=000	KK21	ASI2 ADC WCLK Input on GPI4	SPI Mode Only; B0_P4_R32_D[6:4]=110
W16	ASI1 BCLK Input on GPIO2	B0_P4_R87_D[6:2]=00100; B0_P4_R10_D[4:2]=010	LL15	ASI2 ADC BCLK Output on GPIO1	B0_P4_R86_D[6:2]=10011; B0_P4_R32_D[2:0]=001
X7	ASI2 WCLK Output on WCLK2	B0_P4_R69_D[5:2]=0001; B0_P4_R26_D5=1	LL16	ASI2 ADC BCLK Output on GPIO2	B0_P4_R87_D[6:2]=10011; B0_P4_R32_D[2:0]=010
Y7	ASI2 WCLK Input on WCLK2	B0_P4_R69_D[5:2]=0001; B0_P4_R26_D5=0	MM15	ASI2 ADC WCLK Output on GPIO1	B0_P4_R86_D[6:2]=10010; B0_P4_R32_D[6:4]=001
Z8	ASI2 BCLK Output on BCLK2	B0_P4_R70_D[5:2]=0001; B0_P4_R26_D2=1	MM16	ASI2 ADC WCLK Output on GPIO2	B0_P4_R87_D[6:2]=10010; B0_P4_R32_D[6:4]=010
AA8	ASI2 BCLK Input on BCLK2	B0_P4_R70_D[5:2]=0001; B0_P4_R26_D2=0	NN15	ASI3 ADC BCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R48_D[2:0]=001
BB11	ASI3 WCLK Output on WCLK3	B0_P4_R73_D[5:2]=0001; B0_P4_R42_D5=1	NN16	ASI3 ADC BCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R48_D[2:0]=010
CC11	ASI3 WCLK Input on WCLK3	B0_P4_R73_D[5:2]=0001; B0_P4_R42_D5=0	NN18	ASI3 ADC BCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R48_D[2:0]=011
DD12	ASI3 BCLK Output on BCLK3	B0_P4_R74_D[5:2]=0001; B0_P4_R42_D2=1	NN19	ASI3 ADC BCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R48_D[2:0]=100
EE12	ASI3 BCLK Input on BCLK3	B0_P4_R74_D[5:2]=0001; B0_P4_R42_D2=0	NN20	ASI3 ADC BCLK Input on GPI3	SPI Mode Only; B0_P4_R48_D[2:0]=101

Table 2-6. Multifunction Pin Register Configuration - Audio Serial Interfaces (continued)

	Description	Required Register Setting		Description	Required Register Setting
FF15	ASI1 ADC BCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R16_D[2:0]=001	NN21	ASI3 ADC BCLK Input on GPI4	SPI Mode Only; B0_P4_R48_D[2:0]=110
FF16	ASI1 ADC BCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R16_D[2:0]=010	OO15	ASI3 ADC WCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R48_D[6:4]=001
FF18	ASI1 ADC BCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R16_D[2:0]=011	OO16	ASI3 ADC WCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R48_D[2:0]=010
FF19	ASI1 ADC BCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R16_D[2:0]=100	OO18	ASI3 ADC WCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R48_D[6:4]=011
FF20	ASI1 ADC BCLK Input on GPI3	SPI Mode Only; B0_P4_R16_D[2:0]=101	OO19	ASI3 ADC WCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R48_D[6:4]=100
FF21	ASI1 ADC BCLK Input on GPI4	SPI Mode Only; B0_P4_R16_D[2:0]=110	OO20	ASI3 ADC WCLK Input on GPI3	SPI Mode Only; B0_P4_R48_D[6:4]=101
GG15	ASI1 ADC WCLK Input on GPIO1	B0_P4_R86_D[6:2]=00001; B0_P4_R16_D[6:4]=001	OO21	ASI3 ADC WCLK Input on GPI4	SPI Mode Only; B0_P4_R32_D[6:4]=110
GG16	ASI1 ADC WCLK Input on GPIO2	B0_P4_R87_D[6:2]=00001; B0_P4_R16_D[6:4]=010	PP15	ASI3 ADC BCLK Output on GPIO1	B0_P4_R86_D[6:2]=10101; B0_P4_R48_D[2:0]=001
GG18	ASI1 ADC WCLK Input on GPI1	B0_P4_R91_D[2:1]=01; B0_P4_R16_D[6:4]=011	PP16	ASI3 ADC BCLK Output on GPIO2	B0_P4_R87_D[6:2]=10101; B0_P4_R48_D[2:0]=010
GG19	ASI1 ADC WCLK Input on GPI2	B0_P4_R92_D[5:4]=01; B0_P4_R16_D[6:4]=100	QQ15	ASI3 ADC WCLK Output on GPIO1	B0_P4_R86_D[6:2]=10100; B0_P4_R48_D[6:4]=001
GG20	ASI1 ADC WCLK Input on GPI3	SPI Mode Only; B0_P4_R16_D[6:4]=101	QQ16	ASI3 ADC WCLK Output on GPIO2	B0_P4_R87_D[6:2]=10100; B0_P4_R48_D[6:4]=010
GG21	ASI1 ADC WCLK Input on GPI4	SPI Mode Only; B0_P4_R16_D[6:4]=110			

2.3 Analog Audio I/O

The analog I/O path of the TLV320AIC3212 features a large set of options for signal conditioning as well as signal routing:

- 8 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Recording Mute function
- Automatic gain control (AGC)
- Built in microphone bias
- Stereo digital microphone interface
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode for Recording and Playback
- 2 Headphone Amplifiers
  - Inputs from DAC, Line Output, and/or Analog Bypass Through Mixer Amplifiers (MAL/MAR)
- 2 Line-Out Amplifiers
  - Inputs from DAC, Direct Analog Bypass from IN1L/IN1R, and/or Analog Bypass Through Mixer Amplifiers (MAL/MAR)
- 2 Class-D Amplifiers
  - Inputs from Line Output and/or Analog Bypass Through Mixer Amplifiers (MAL/MAR)

- 1 Differential Receiver Amplifier
  - Inputs from Line Output and/or Direct Analog Bypass from IN1L/IN1R
- Playback Mute function
- Dynamic range compression (DRC)

2.3.1 Analog Low Power Bypass

The TLV320AIC3212 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode. In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the left lineout amplifier (LOL) and IN1R to LOR. Additionally, line-level signals can be routed directly from these analog inputs to the differential receiver amplifier, which outputs on RECP and RECM.

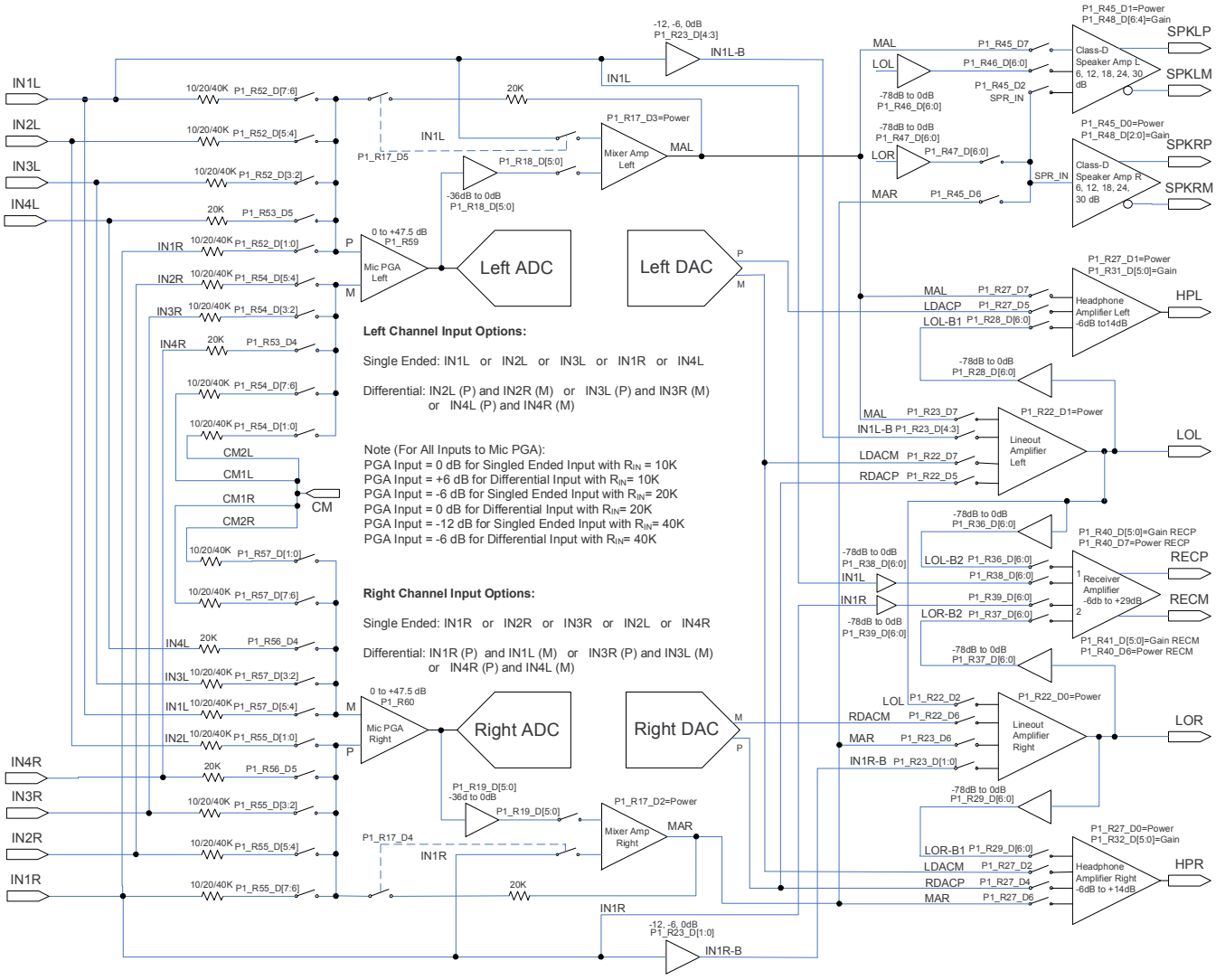


Figure 2-1. Analog Routing Diagram

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1L to the positive input on differential receiver amplifier (RECP) and IN1R to RECM, with gain control of -78dB to 0dB. This is configured on B0_P1_R38_D[6:0] for the left channel and B0_P1_R39_D[6:0] for the right channel.

To use the mixer amplifiers, power them on via B0_P1_R17_D[3:2].

Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended DC-coupled headphone configurations. An integral charge pump generates the negative supply required to operate the headphone drivers in dc-coupled mode, where the common mode of the output signal is made equal to the ground of the headphone load using a ground-sense circuit. Operation of headphone drivers in dc-coupled (ground centered mode) eliminates the need for large dc-blocking capacitors.

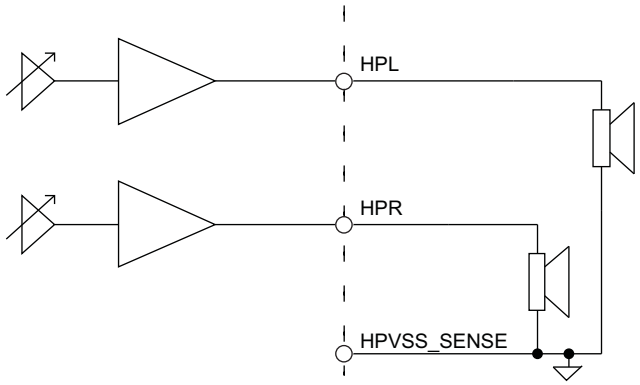


Figure 2-2. TLV320AIC3212 Ground-Centered Headphone Output

Alternatively the headphone amplifier can also be operated in a unipolar circuit configuration using DC blocking capacitors.

2.3.2 Using the Headphone Amplifier

The headphone drivers are capable of driving a mixed combination of DAC signal, left and right ADC PGA signal, and LOL and LOR output signals by configuring B0_P1_R27-R29. The ADC PGA signals can be attenuated up to 36dB before routing to headphone drivers by configuring B0_P1_R18 and B0_P1_R19. The line-output signals can be attenuated up to 78dB before routing to headphone drivers by configuring B0_P1_R28 and B0_P1_R29. The level of the DAC signal can be controlled using the digital volume control of the DAC by configuring B0_P0_R64-R66. To control the output-voltage swing of headphone drivers, the headphone driver volume control provides a range of –6.0dB to +14.0dB in steps of 1dB. These can be configured by programming B0_P1_R27, B0_P1_R31, and B0_P1_R32. In addition, finer volume controls are also available when routing LOL or LOR to the headphone drivers by controlling B0_P1_R27-R28. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Register B0_P1_R9_D[6:5] allows the headphone output stage to be scaled to tradeoff power delivered vs quiescent power consumption. (1)

2.3.3 Ground-Centered Headphone Amplifier Configuration

Among the other advantages of the ground-centered connection is inherent freedom from turn-on transients that can cause audible pops, sometimes at uncomfortable volumes.

2.3.3.1 Circuit Topology

The power supply hook up scheme for the ground centered configuration is shown in HVDD_18 pin supplies the positive side of the headphone amplifier. CPVDD_18 pin supplies the charge pump which in turn supplies the negative side of the headphone amplifier. Two capacitors are required for the charge pump circuit to work. These capacitors should be X7R rated.

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

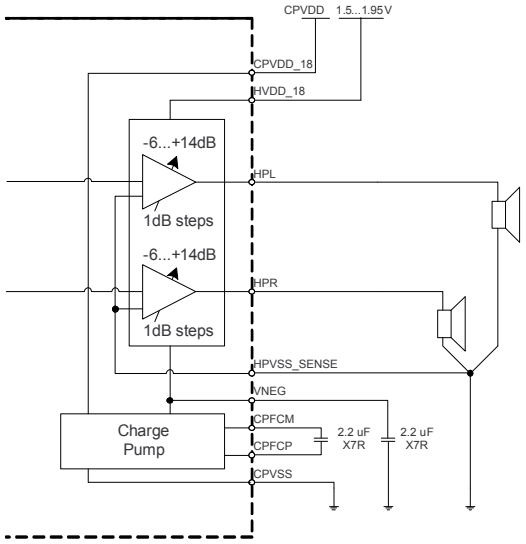


Figure 2-3. Ground-Centered Headphone Connections

2.3.3.2 Charge Pump Setup and Operation

The built in charge pump draws charge from the CPVDD_18 supply, and by switching the external capacitor between CPFCP and CPFCM, generates the negative voltage on VNEG pin. The charge-pump circuit uses the principles of switched-capacitor charge conservation to generate the VNEG supply in a very efficient fashion.

To turn on the charge pump circuit when headphone drivers are powered, program B0_P1_R35_D[1:0] to '"00". When the charge pump circuit is disabled, VNEG acts as a ground terminal, allowing unipolar configuration of the headphone amps. By default, the charge pump is disabled. The switching rate of the charge pump can be controlled by B0_P1_R33. Because the charge pump can demand significant inrush currents from the supply, it is important to have a capacitor connected in close proximity to the CPVDD_18 and CPVSS pins of the device. At 500kHz clock rate this requires approximately a 10µF capacitor. The ESR and ESL of the capacitor must be low to allow fast switching currents.

The ground-centered mode of operation is enabled by configuring B0_P1_R31_D7 to "1". Note that the HPL and HPR gain settings are ganged in Ground-Cetered Mode of operation (B0_P1_R32_D7 = "1"). The HPL and HPR gain settings cannot be ganged if using the Stereo Unipolar Configuration.

2.3.3.3 Output Power Optimization

The device can be optimized for a specific output-power range. The charge pump and the headphone driver circuitry can be reduced in power so less overall power is consumed. The headphone driver power can be programmed in B0_P1_R9. The control of charge pump switching current is programmed in B0_P1_R34_D[4:2].

2.3.3.4 Offset Correction and Start-Up

The TLV320AIC3212 offers an offset-correction scheme that is based on calibration during power up. This scheme minimizes the differences in DC voltage between HPVSS_SENSE and HPL/HPR outputs.

The offset calibration happens after the headphones are powered up in ground-centered configuration. All other headphone configurations like signal routings, gain settings and mute removal must be configured before headphone powerup. Any change in these settings while the headphones are powered up may result in additional offsets and are best avoided.

The offset-calibration block has a few programmable parameters that the user must control. The user can either choose to calibrate the offset only for the selected input routing or all input configurations. The calibration data is stored in internal memory until the next hardware reset or until AVDDx power is removed.

Programming B0_P1_R34_D[1:0] as "10" causes the offset to be calibrated for the selected input mode. Programming B0_P1_R34_D[1:0] as “11” causes the offset to be calibrated for all possible configurations. All related blocks must be powered while doing offset correction.

Programming B0_P1_R34_D[1:0] as “00” (default) disables the offset correction block. While the offset is being calibrated, no signal should be applied to the headphone amplifier, i.e. the DAC should be kept muted and analog bypass routing should be kept at the highest attenuation.

2.3.3.5 Ground-Centered Headphone Setup

There are four practical device setups for ground-centered operation, shown in Table 2-7:

Table 2-7. Ground-Centered Headphone Setup Performance Options

Audio Output Power		High Performance			Low Power Consumption		
		16Ω	32Ω	600Ω	16Ω	32Ω	600Ω
High	SNR	94 dB	97 dB	98 dB	91 dB	94 dB	95 dB
	Output Power	25 mW	22 mW	1.4mW	24 mW	23 mW	1.5mW
	Idle Power Consumption	23 mW	21 mW	19mW	20 mW	15 mW	12 mW
		High-Output, High-Performance Setup			High-Output, Low-Power Setup		
Medium	SNR	92.5 dB	93 dB	93.5 dB	80.5 dB	85.5 dB	85.5 dB
	Output Power	16 mW	8.5 mW	0.5 mW	0.9 mW	1.5mW	0.1 mW
	Idle Power Consumption	14 mW	12 mW	9.7 mW	8.0 mW	6.6mW	5.1 mW
		Medium-Output, High-Performance Setup			Medium-Output, Low-Power Setup		

High Audio Output Power, High Performance Setup

This setup describes the register programming necessary to configure the device for a combination of high audio output power and high performance. To achieve this combination the parameters must be programmed to the values in Table 2-8. For the full setup script, see Section 4.1.1.

Table 2-8. Setup A - High Audio Output Power, High Performance

Parameter	Value	Programming
CM	0.9	B0_P1_R8_D2 = "0"
PTM	PTM_P3	B0_P1_R3_D[4:2] = "000", B0_P1_R4_D[4:2] = "000"
Processing Block	1 to 6,22,23,24	B0_P0_R60_D[4:0]
DAC OSR	128	B0_P0_R13 = 0x00, B0_P0_R14 = 0x80
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	5dB	B0_P1_R31 = 0x85, B0_P1_R32 = 0x85
DVDD	1.8	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.8	Apply 1.8 to 1.95V

High Audio Output Power, Low Power Consumption Setup

This setup describes the register programming necessary to configure the device for a combination of high audio output power and low power consumption. To achieve this combination the parameters must be programmed to the values in Table 2-9. For the full setup script, see Section 4.1.2.

Table 2-9. Setup B - High Audio Output Power, Low Power Consumption

Parameter	Value	Programming
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P2	B0_P1_R3_D[4:2] = "001", B0_P1_R4_D[4:2] = "001"
Processing Block	7 to 16	B0_P0_R60_D[4:0]
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	12dB	B0_P1_R31 = 0x8c, B0_P1_R32 = 0x8c
DVDD	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.8	Apply 1.5 to 1.95V

Medium Audio Output Power, High Performance Setup

This setup describes the register programming necessary to configure the device for a combination of medium audio output power and high performance. To achieve this combination the parameters must be programmed to the values in Table 2-10. For the full setup script, see Section 4.1.3.

Table 2-10. Setup C - Medium Audio Output Power, High Performance

Parameter	Value	Programming
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P2	B0_P1_R3_D[4:2] = "001", B0_P1_R4_D[4:2] = "001"
Processing Block	7 to 16	B0_P0_R60_D[4:0]
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	100	B0_P1_R9_D[6:5] = "00"
Gain	7dB	B0_P1_R31 = 0x87, B0_P1_R32 = 0x87
DVDD	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.5	Apply 1.8 to 1.95V

Lowest Power Consumption, Medium Audio Output Power Setup

This setup describes the register programming necessary to configure the device for a combination of medium audio output power and lowest power consumption. To achieve this combination the parameters must be programmed to the values in Table 2-11. For the full setup script, see Section 4.1.4.

Table 2-11. Setup D - Lowest Power Consumption, Medium Audio Output Power

Parameter	Value	Programming
CM	0.75	B0_P1_R8_D2 = "1"
PTM	PTM_P1	B0_P1_R3_D[4:2] = "010", B0_P1_R4_D[4:2] = "010"
Processing Block	26	B0_P0_R60_D[4:0] = "1 1010"
DAC OSR	64	B0_P0_R13 = 0x00, B0_P0_R14 = 0x40
HP sizing	25	B0_P1_R9_D[6:5] = "11"
Gain	10dB	B0_P1_R31 = 0x8a , B0_P1_R32 = 0x8a
DVdd	1.26	Apply 1.26 to 1.95V
AVDDx_18, HVDD_18, CPVDD_18	1.5	Apply 1.5 to 1.95V

2.3.4 Stereo Unipolar Configuration

2.3.4.1 Circuit Topology

The power supply hook up scheme for the unipolar configuration is shown in Figure 2-4. HVDD_18 pin supplies the positive side of the headphone amplifier. The negative side is connected to ground potential (VNEG). It is recommended to connect the CPVDD_18 pin to DVdd, although the charge pump *must not* be enabled while the device is connected in unipolar configuration.

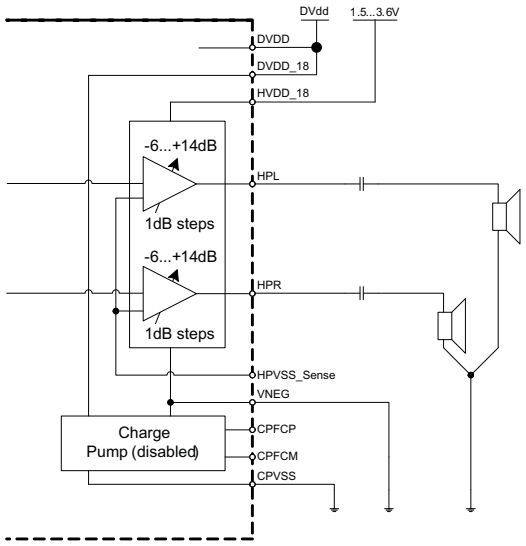


Figure 2-4. Unipolar Stereo Headphone Circuit

The left and right DAC channels are routed to the corresponding left and right headphone amplifier. This configuration is also used to drive line-level loads. To enable cap-coupled mode, B0_P1_R31_D7 should be set to 0. Note that the recommended range for the HVDD_18 supply in cap-coupled mode (1.65V-3.6V) is different than the recommended range for the default ground-centered configuration (1.5V-1.95V). In cap-coupled mode only, the Headphone output common mode can be controlled by changing B0_P1_R8_D[4:3].

2.3.4.2 Unipolar Turn-On Transient (Pop) Reduction

The TLV320AIC3212 headphone drivers also support pop-free operation in unipolar, ac-coupled configuration. Because the HPL and HPR are high-power drivers, pop can result due to sudden transient changes in the output drivers if care is not taken. The most critical care is required while using the drivers as stereo single-ended capacitively-coupled drivers as shown in Figure 2-4. The output drivers achieve pop-free power-up by using slow power-up modes. Conceptually, the circuit during power-up can be visualized as

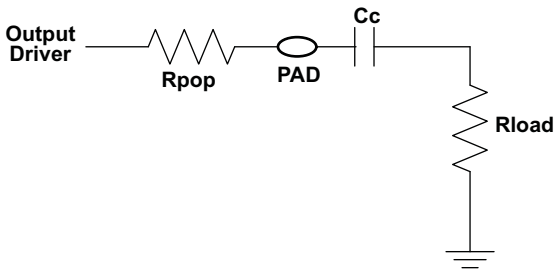


Figure 2-5. Conceptual Circuit for Pop-Free Power-up

The value of R_{pop} can be chosen by setting register B0_P1_R11_D[1:0].

Table 2-12. R_{pop} Values (External C_c = 47uF)

B0_P1_R11_D[1:0]	R_{pop} Value
10	2 kΩ
01	6 kΩ
00	25 kΩ

To minimize audible artifacts, two parameters can be adjusted to match application requirements. The voltage V_{load} across R_{load} at the beginning of slow charging should not be more than a few mV. At that time the voltage across R_{load} can be determined as:

$$V_{load} = \frac{R_{load}}{R_{load} + R_{pop}} \times V_{cm} \quad (1)$$

For a typical R_{load} of 32Ω, R_{pop} of 6 kΩ or 25 kΩ will deliver good results (see Table 2-12 for register settings).

According to the conceptual circuit in Figure 2-5, the voltage on PAD will exponentially settle to the output common-mode voltage based on the value of R_{pop} and C_c. Thus, the output drivers must be in slow power-up mode for time T, such that at the end of the slow power-on period, the voltage on V_{pad} is very close to the common-mode voltage. The TLV320AIC3212 allows the time T to be adjusted to allow for a wide range of R_{load} and C_c by programming B0_P1_R11_D[5:2]. For the time adjustments, the value of C_c is assumed to be 47µF. N=5 is expected to yield good results.

B0_P1_R11_D[5:2]	Slow Charging Time = N * RC_Time_Constant (for R_{pop} and C_c = 47µF)
0000	N=0
0001	N=0.5
0010	N=0.625
0011	N=0.75
0100	N=0.875
0101	N=1.0
0110	N=2.0
0111	N=3.0
1000	N=4.0
1001	N=5.0 (Typical Value)
1010	N=6.0
1011	N=7.0
1100	N=8.0
1101	N=16 (Not valid for R_{pop}=25kΩ)
1110	N=24 (Not valid for R_{pop}=25kΩ)
1111	N=32 (Not valid for R_{pop}=25kΩ)

Again, for example, for R_{load}=32Ω, C_c=47µF and common mode of 0.9V, the number of time constants required for pop-free operation is 5 or 6. A higher or lower C_c value will require higher or lower value for N.

During the slow-charging period, no signal is routed to the output driver. Therefore, choosing a larger than necessary value of N results in a delay from power-up to signal at output. At the same time, choosing N to be smaller than the optimal value results in poor pop performance at power-up.

The signals being routed to headphone drivers (e.g. DAC and IN) often have DC offsets due to less-than-ideal processing. As a result, when these signals are routed to output drivers, the offset voltage causes a pop. To improve the pop-performance in such situations, a feature is provided to soft-step the DC-offset. At the beginning of the signal routing, a high-value attenuation can be applied which can be progressively reduced in steps until the desired gain in the channel is reached. The time interval between each of these gain changes can be controlled by programming B0_P1_R11_D[7:6]. This gain soft-stepping is applied only during the initial routing of the signal to the output driver and not during subsequent gain changes.

B0_P1_R11_D[7:6]	Soft-stepping Step Time During initial signal routing
00	0 ms (soft-stepping disabled)
01	50ms
10	100ms
11	200ms

It is recommended to use the following sequence for achieving optimal pop performance at power-up:

1. Choose the value of R_{pop}, N (time constants) and soft-stepping step time for slow power-up.
2. Choose the configuration for output drivers, including common modes and output stage power connections
3. Select the signals to be routed to headphones.
4. Power-up the blocks driving signals into HPL and HPR, but keep it muted
5. Unmute HPL and HPR and set the desired gain setting.
6. Power-on the HPL and HPR drivers.
7. Unmute the block driving signals to HPL and HPR after the Driver PGA flags are set to indicate completion of soft-stepping after power-up. These flags can be read from B0_P1_R63_D[7:6].

It is important to configure the Headphone Output driver depop control registers before powering up the headphone; these register contents should not be changed when the headphone drivers are powered up.

Before powering down the HPL and HPR drivers, it is recommended that user read back the flags in B0_P1_R63. For example. before powering down the HPL driver, ensure that bit B0_P1_R63_D7 = 1 and bit B0_P1_R64_D7 = 1 if LOL is routed to HPL and bit B0_P1_R65_D5 = 1 if the Left Mixer is routed to HPL. The output driver should be powered down only after a steady-state power-up condition has been achieved. This steady state power-up condition also must be satisfied for changing the HPL/R driver mute control (setting both B0_P1_R31_D[5:0] and B0_P1_R32_D[5:0] to "11 1001"), i.e. muting and unmuting should be done after the gain and volume controls associated with routing to HPL/R finished soft-stepping.

In the differential configuration of HPL and HPR, when no coupling capacitor is used, the slow charging method for pop-free performance need not be used. In the differential load configuration for HPL and HPR, it is recommended to not use the output driver MUTE feature, because a pop may result.

During the power-down state, the headphone outputs are weakly pulled to ground using an approximately 50kΩ resistor to ground, to maintain the output voltage on HPL and HPR pins.

2.3.5 Mono Differential DAC to Mono Differential Headphone Output

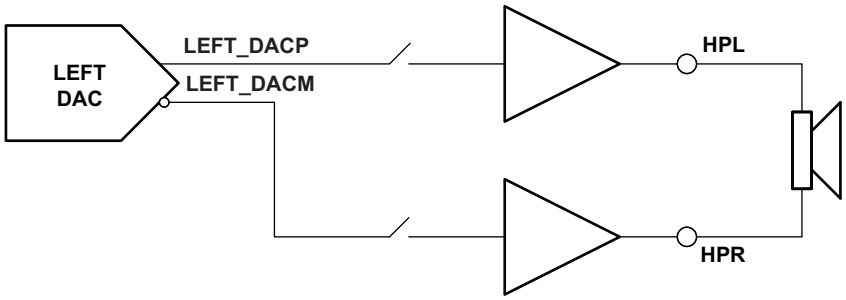


Figure 2-6. Low Power Mono DAC to Differential Headphone

This configuration, available in unipolar configuration of the HP amplifier supplies, supports the routing of the two differential outputs of the mono, left channel DAC to the headphone amplifiers in differential mode (B0_P1_R27_D5 = 1 and B0_P1_R27_D2 = 1).

2.3.6 Stereo Line Outputs

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common mode of line level drivers can be configured to equal the analog input common-mode setting, either 0.75V or 0.9V. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal, and signal mixing is register-programmable.

2.3.7 Line Out Amplifier Configurations

Signal mixing can be configured by programming B0_P1_R22 and B0_P1_R23. To route the output of Left DAC and Right DAC for stereo single-ended output, as shown in Figure 2-7, LDACM can be routed to LOL driver by setting B0_P1_R22_D7 = '1', and RDACM can be routed to LOR driver by setting B0_P1_R22_D6 = '1'. Alternatively, stereo single-ended signals can also be routed through the mixer amplifiers by configuring B0_P1_R23_D[7:6]. For lowest-power operation, stereo single-ended signals can also be routed in direct pin bypass with possible gains of 0dB, -6dB, or -12dB by configuring B0_P1_R23_D[4:3] and B0_P1_R23_D[1:0]. While each of these two bypass cases could be utilized in a stereo single-ended configuration, a mono differential input signal could also be utilized.

The output of the stereo line out drivers can also be routed to the stereo headphones drivers, with 0dB to -72dB gain controls in steps of 0.5dB on each headphone channel. This enables the DAC output or bypass signals to be simultaneously played back to the stereo headphone drivers as well as stereo line- level drivers. This routing and volume control is achieved in B0_P1_R28 and B0_P1_R29.

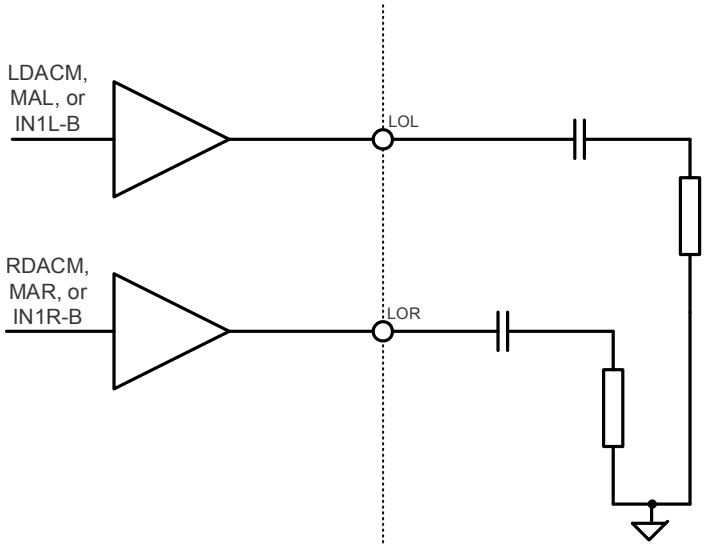


Figure 2-7. Stereo Single-Ended Line-out

Additionally, the two line-level drivers can be configured to act as a mono differential line level driver by routing the output of LOL to LOR (B0_P1_R22_D2 = '1'). This differential signal takes either LDACM, MAL, or IN1L-B as a single-ended mono signal and creates a differential mono output signal on LOL and LOR.

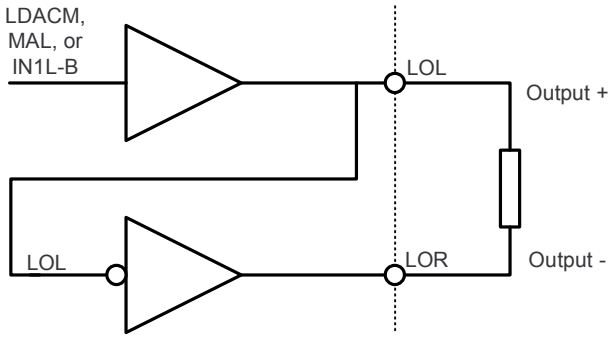


Figure 2-8. Single Channel Input to Differential Line-out

For digital outputs from the DAC, the two line-level drivers can be fed the differential output signal from the Right DAC by configuring B0_P1_R22_D5 = '1'.

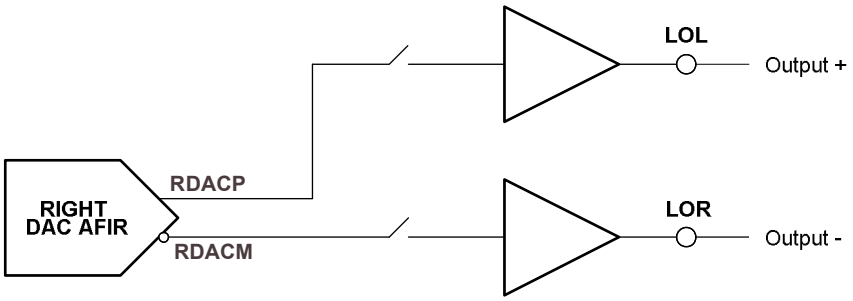


Figure 2-9. Mono DAC Output to Differential Line-out

2.3.8 Differential Receiver Output

The differential receiver amplifier output spans the RECP and RECM pins and can drive a 32Ω receiver driver. With output common-mode setting of 1.65V and RECVDD_33 supply at 3.3V, the receiver driver can drive up to a 1Vrms output signal. With the RECVDD_33 supply at 3.3V, the receiver driver can deliver greater than 128mW into a 32Ω BTL load. If desired, the RECVDD_33 supply can be set to 1.8V, at which the driver can deliver about 40mW into the 32Ω BTL load.

The differential receiver driver is capable of driving a mixed combination of DAC signal through the Line Out amplifiers and the line-bypass from analog input IN1L and IN1R. Routing and volume level setting of the IN1L and IN1R input signals to the Positive and Negative driver is controlled by B0_P1_R38 and B0_P1_R39 respectively. These two registers enable fine tuning of the inputs to the receiver driver by allowing up to 78dB of attenuation. A single volume control can be utilized for both inputs by setting B0_P1_R39_D7. Routing and volume level setting of the LOL and LOR signals to the positive and negative inputs of the differential receiver driver is controlled by B0_P1_R36 and B0_P1_R37 respectively. These two registers enable fine tuning of the separate positive and negative differential signals by allowing up to 78dB of attenuation. A single volume control can be utilized for both inputs by setting B0_P1_R37_D7.

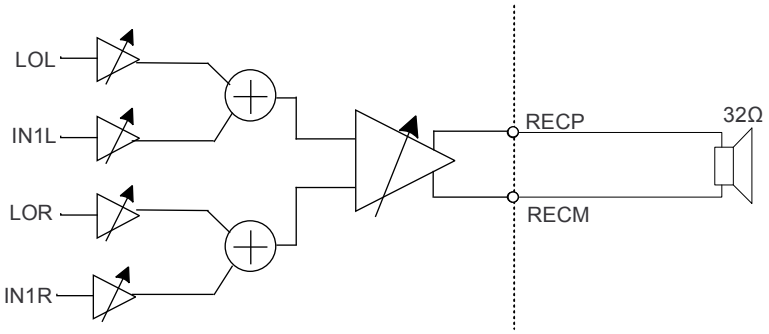


Figure 2-10. Receiver Differential Output

The receiver driver can be powered on by writing 11 to B0_P1_R40_D[7:6]. The positive driver gain and muting can be controlled by writing to B0_P1_R40_D[5:0], and the negative driver gain can be controlled by writing to B0_P1_R41_D[5:0], with each amplifier providing -6dB to 29dB gains in steps of 1dB. A single volume control can be utilized for the differential receiver output drivers by setting B0_P1_R41_D7 to '1'.

The TLV320AIC3212 has an overcurrent/short-circuit protection feature for the receiver drivers that is always enabled to provide protection. If the output is shorted, this overcurrent condition either shuts down the output stage (if B0_P1_R10_D0 = 1) or starts to limit the amount of current (if B0_P1_R10_D0 = 0). The default condition for the receiver driver is current-limiting mode. In case of a short circuit, for automatic latching shutdown, the output is disabled and a status flag is provided as read-only bits B0_P0_R44_D7 for RECP and on B0_P0_R44_D6 for RECM.

The receiver driver also has an offset calibration for minimizing start-up transients. By default, this feature is enabled for every power-up by setting B0_P1_R42_D[4:3] to '01'. The status of the offset calibration can be read this the Receiver Offset Calibration Flag (B0_P1_R42_D7). Offset calibration should only be disabled if utilized this driver as a second single-ended headphone configuration (i.e. should be utilized in differential receiver configuration).

2.3.9 Example Setup for Differential Receiver Routing

The following script shows an example setup for how to route to the Differential Receiver Driver. For full scripts, see the example scripts in Section 4.3.1.

- Route Left DAC to LOL to Input 1 of Receiver Driver
- Route Right DAC to LOR to Input 2 of Receiver Driver
- Output Common Mode of 1.65V (assumes 3.3V
- Single Volume Control for LOL/LOR into Receiver Driver
- Single Volume Control for Receiver Driver Differential Output

Script

```
#Ensure on Page 0 of current Book
w 30 00 00
#Go to Book 0
w 30 FF 00
#Go to Page 0
w 30 00 00
# Power up the Left and Right DAC Channels
w 30 3f c0
# Unmute the DAC digital volume control
w 30 40 00
# Select Page 1
w 30 00 01
# Enable Right DAC differential to LOL/R routing and power-up LOL/R
w 30 16 63
# Set output common mode for drivers (REC) to 1.65V assuming RECVDD_33 = 3.3
w 30 08 03
```

```
# Set routing of LOL to RECP to 0dB
w 30 24 00
# Set routing of LOR to RECM to follow LOL->RECP setting
w 30 25 80
# Set offset callibration scheme for RECP/M
w 30 2A 04
# Use Single Volume Control for Differential Receiver
w 30 29 80
# Power up the RECP and RECM drivers with gain set to 0 dB
w 30 28 C0
```

2.3.10 Stereo Class-D Speaker Outputs

The integrated Class-D stereo speaker drivers (SPKLP/SPKLN and SPKRP/SPKRN) are capable of driving two 8Ω differential loads. The speaker drivers can be powered directly from the power supply (2.7V to 5.5V) on the SLVDD and SRVDD pins, however the voltage (including spike voltage) must be limited below the Absolute Maximum Voltage of 6.0V.

The speaker drivers are capable of supplying 750 mW per channel at 10% THD+N with a 3.6-V power supply and 1.46W per channel at 10% THD+N with a 5.0V power supply. Separate left and right channels can be sent to each Class-D driver through the Lineout signal path, or from the mixer amplifiers in the ADC bypass. If only one speaker is being utilized for playback, the analog mixer before the Left Speaker amplifier can sum the left and right audio signals for monophonic playback.

The speaker drivers are capable of driving a mixed combination of DAC signal through the Line Out amplifiers and the left and right ADC PGA signal. The ADC PGA signals can be routed to the speaker drivers by setting B0_P1_R45_D7 (Left Mixer amplifier to Left Speaker) and B0_P1_R45_D6 (Right Mixer amplifier to Right Speaker), and these signals can be attenuated up to 36dB before this routing to the speakers by configuring B0_P1_R18 and B0_P1_R19. Routing and volume level setting of the LOL and LOR signals to the Left and Right speaker driver is controlled by B0_P1_R46 and B0_P1_R47 respectively. These two registers enable fine tuning of the separate stereo speaker signals by allowing up to 78dB of attenuation. To play the stereo DAC signals through the Line Out amplifiers to the speakers, the DAC signals should be routed to the LOL/LOR drivers by setting B0_P1_R22_D[7:6]. The level of these DAC signal can also be controlled using the digital volume control of the DAC signal (B0_P0_R65 and B0_P0_R66). The same monophonic signal (from LOR or MAR) can also be sent to both speakers by setting B0_P1_R45_D2.

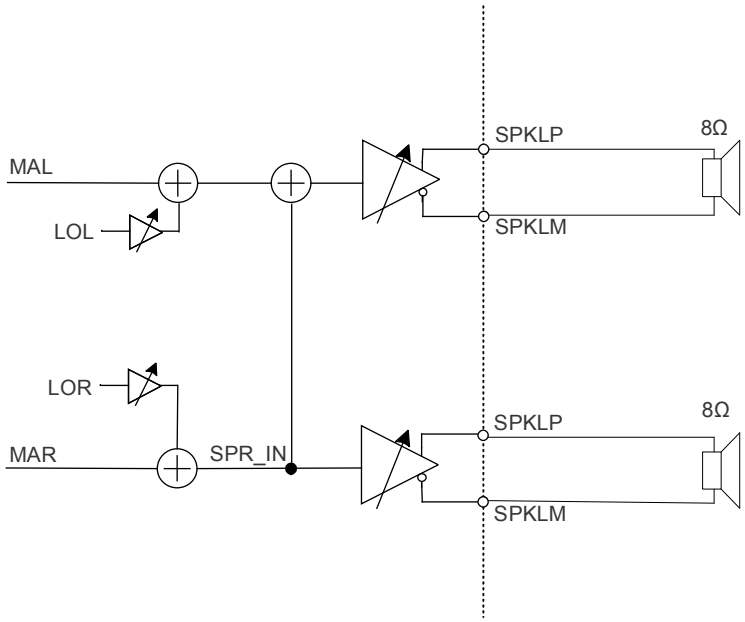


Figure 2-11. Stereo Speaker Outputs

The left class-D speaker driver can be powered on by writing to B0_P1_R45_D1. The right class-D speaker driver can be powered on by writing to B0_P1_R45_D0. The left-output driver gain can be controlled by writing to B0_P1_R48_D[6:4], and it can be muted by writing '000' to these bits. The right-output driver gain can be controlled by writing to B0_P1_R48_D[2:0], and it can also be muted by writing '000' to these bit locations.

The TLV320AIC3212 has a short-circuit protection feature for the speaker drivers that is always enabled to provide protection. If the output is shorted, the output stage shuts down on the overcurrent condition. (Current limiting is not an available option for the higher-current speaker driver output stage.) In case of a short circuit on either channel, the output is disabled and a status flag is provided as a read-only bit on B0_P0_R44_D7 for SPKL and on B0_P0_R44_D6 for SPKR. If shutdown occurs due to an overcurrent condition, then the device requires a reset to re-enable the output stage. Resetting can be done in two ways. First, the device master reset can be used, which requires either toggling the RESET pin or using the software reset. If master reset is used, it resets all of the registers. Second, a dedicated speaker power-stage reset can be used that keeps all of the other device settings. The speaker power-stage reset is done by setting B0_P1_R45_D1 for SPKLP and SPKLM and by setting B0_P1_R45_D0 for SPKRP and SPKRM. If the fault condition has been removed, then the device returns to normal operation. If the fault is still present, then another shutdown occurs. Repeated resetting (more than three times) is not recommended, as this could lead to overheating.

The TLV320AIC3212 has a overtemperature thermal protection (OTP) feature for the speaker drivers which is always enabled to provide protection. If the device is overheated, then the output stops switching. When the device cools down, the device resumes switching. An overtemperature status flag is provided as a read-only bit on B0_P0_R45_D7, and this status flag can be routed to INT1 interrupt (B0_P0_R48_D1 = '1') or INT2 interrupt (B0_P0_R49_D1 = '1'). The OTP feature is for self-protection of the device. If die temperature can be controlled at the system/board level, then overtemperature does not occur.

To minimize battery current leakage, the SLVDD and SRVDD voltage levels should not be less than the AVDDx_18 voltage levels.

2.3.11 Example Setup for Stereo Class-D Routing

The following script shows an example setup for how to route to the Class-D Speaker Drivers. For full scripts, see the example scripts in Section 4.4.

- Route Left DAC to LOL to Left Class-D Speaker Driver
- Route Right DAC to LOR to Right Class-D Speaker Driver
- No attenuation on LOL input to Left Class-D Driver (0dB)
- No attenuation on LOR input to Right Class-D Driver (0dB)
- Left and Right Class-D Speaker Drivers set to 6dB gain

Script

```
#Ensure on Page 0 of current Book
w 30 00 00
#Go to Book 0
w 30 FF 00
#Go to Page 1
w 30 00 01
#Enable DAC to LOL/R routing and power-up LOL/R
w 30 16 c3
# Route LOL to SPK-Left @ 0dB
w 30 2E 00
# Route LOR to SPK-Right @ 0dB
w 30 2F 00
# Set Left Speaker Gain @ 6dB, Right Speaker Gain @ 6dB
w 30 30 11
# Power-up Stereo Speaker
w 30 2D 03

# Select Page 0
w 30 00 00
# Power up the Left and Right DAC Channels
w 30 3f c0
```

```
# Unmute the DAC digital volume control
w 30 40 00
```

2.4 ADC

The TLV320AIC3212 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3212 features a large set of options for signal conditioning as well as signal routing:

- 2 ADCs
- 8 analog inputs which can be mixed and/or multiplexed in single-ended and/or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Fine gain adjust of digital channels with 0.1 dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function
- Automatic gain control (AGC)

In addition to the standard set of ADC features the TLV320AIC3212 also offers the following special functions:

- Built in microphone biases
- Stereo digital microphone interface
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog anti-aliasing filtering are very relaxed. The TLV320AIC3212 integrates a second order analog anti-aliasing filter with 28-dB attenuation at 6MHz. This filter, combined with the digital decimation filter, provides sufficient anti-aliasing filtering without requiring additional external components.

2.4.1 ADC Signal Routing

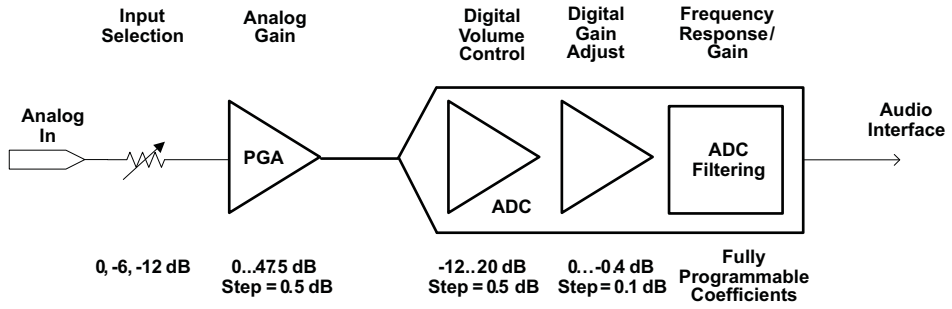
As shown in Figure 2-1, the TLV320AIC3212 includes eight analog inputs which can be configured as either 4 stereo single-ended pairs or 4 fully-differential pairs. These pins connect through series resistors and switches to the virtual ground terminals of two fully-differential amplifiers (one per ADC/PGA channel). By turning on only one set of switches per amplifier at a time, the inputs can be effectively multiplexed to each ADC PGA channel. By turning on multiple sets of switches per amplifier at a time, audio sources can be mixed. The TLV320AIC3212 supports the ability to mix up to five single-ended analog inputs or up to three fully-differential analog inputs into each ADC PGA channel.

In most applications, high input impedance is desired for analog inputs. However when used in conjunction with high gain as in the case of microphone inputs, the higher input impedance results in higher noise or lower dynamic range. The TLV320AIC3212 allows the user the flexibility of choosing the input impedance from 10kΩ, 20kΩ and 40kΩ. When multiple inputs are mixed together, by choosing different input impedances, level adjustment can be achieved. For example, if one input is selected with 10kΩ input impedance and the second input is selected with 20kΩ input impedance, then the second input is attenuated by half as compared to the first input. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting. Also, note that this input level configurability is available on IN1L, IN1R, IN2L, IN2R, IN3L, and IN3R; for IN4L and IN4R, this input impedance is fixed at 20kΩ.

Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the system designer is advised to take adequate precautions to avoid such a saturation from occurring. In general, the mixed signal should not exceed 0dB.

Typically, voice or audio signal inputs are capacitively coupled to the device. This allows the device to independently set the common mode of the input signals to values chosen by register control of B0_P1_R8_D2 to either 0.9V or 0.75V. The correct value maximizes the dynamic range across the entire analog-supply range. Failure to capacitively connect the input to the device can cause high offset due to mismatch in source common-mode and device common-mode setting. In extreme cases it could also saturate the analog channel, causing distortion.

2.4.2 ADC Gain Setting



When the gain of the ADC Channel is kept at 0dB and the common mode set to 0.75V, a single-ended input of $0.375V_{RMS}$ results in a full-scale digital signal at the output of ADC channel. Similarly, when the gain is kept at 0dB, and common mode is set to 0.9V, a single-ended input of $0.5V_{RMS}$ results in a full-scale digital signal at the output of the ADC channel. However various block functions control the gain through the channel. The gain applied by the PGA is described in Table 2-13. Additionally, the digital volume control adjusts the gain through the channel as described in Section 2.4.2.2. A finer level of gain is controlled by fine gain control as described in Section 2.4.2.3. The decimation filters A, B and C along with the delta-sigma modulator contribute to a DC gain of 1.0 through the channel.

2.4.2.1 Analog Programmable Gain Amplifier (PGA)

The TLV320AIC3212 features a built-in low-noise PGA for boosting low-level signals, such as direct microphone inputs, to full-scale to achieve high SNR. This PGA can provide a gain in the range of 0dB to 47.5dB for single-ended inputs or 6dB to 53.5dB for fully-differential inputs (gain calculated w.r.t. input impedance setting of 10kΩ, 20kΩ input impedance will result in 6dB lower and 40kΩ will result in 12dB lower gain). This gain can be user controlled by writing to B0_P1_R59 and B0_P1_R60. In the AGC mode this gain can also be automatically controlled by the built-in hardware AGC.

Table 2-13. Analog PGA vs Input Configuration

Book 0, Page 1, Register 59, D[6:0] (B0_P1_R59_D[6:0]) Book 0, Page 1, Register 60, D[6:0] B0_P1_R60_D[6:0]	EFFECTIVE GAIN APPLIED BY PGA					
	SINGLE-ENDED			DIFFERENTIAL		
	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K	R_{IN} = 10K	R_{IN} = 20K	R_{IN} = 40K
000 0000	0 dB	–6 dB	-12 dB	6.0 dB	0 dB	–6.0 dB
000 0001	0.5 dB	–5.5 dB	–11.5 dB	6.5 dB	0.5 dB	-5.5 dB
000 0010	1.0 dB	–5.0 dB	–11.0 dB	7.0 dB	7.5 dB	–5.0 dB
…	…	…	…	…	…	…
101 1110	47.0 dB	41.0 dB	35.0 dB	53.0 dB	47.0 dB	41.0 dB
101 1111	47.5 dB	41.5 dB	35.5 dB	53.5 dB	47.5 dB	41.5 dB

The gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register value (see registers B0_P0_R81_D[1:0]). This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and at power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag B0_P0_R36_D7 and B0_P0_R36_D3 is set whenever the gain applied by the PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming B0_P0_R81_D[1:0].

2.4.2.2 Digital Volume Control

The TLV320AIC3212 also has a digital volume-control block with a range from -12dB to +20dB in steps of 0.5dB. It is set by programming B0_P0_R83 and B0_P0_R84 respectively for left and right channels.

Table 2-14. Digital Volume Control for ADC

Desired Gain dB	Left / Right Channel B0_P0_R83 and B0_P0_R84, D[6:0]
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (Default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, the soft-stepping feature is used to avoid audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured via B0_P0_R81_D[1:0], and is common to soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to -12.0dB before powering down. Due to the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320AIC3212 gives feedback to the user, through read-only flags B0_P0_R36_D7 for Left Channel and B0_P0_R36_D3 for the right channel.

2.4.2.3 Fine Digital Gain Adjustment

Additionally, the gains in each of the channels is finely adjustable in steps of 0.1dB. This is useful when trying to match the gain between channels. By programming B0_P0_R82, the gain can be adjusted from 0dB to -0.4dB in steps of 0.1dB. This feature, in combination with the regular digital volume control allows the gains through the left and right channels be matched in the range of -0.5dB to +0.5dB with a resolution of 0.1dB.

2.4.2.4 AGC

The TLV320AIC3212 includes Automatic Gain Control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Since the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

1. **Target Level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC3212 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the TLV320AIC3212 reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.
2. **Attack Time** determines how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. Wide range of attack time programmability is supported in terms of number of samples (i.e. number of ADC sample frequency clock cycles).
3. **Decay Time** determines how quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. Wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample frequency clock cycles).
4. **Gain Hysteresis** is the hysteresis applied to the required gain calculated by the AGC function while changing its mode of operation from attack to decay or vice-versa. For example, while attacking the input signal, if the current applied gain by the AGC is *x*dB, and suddenly because of input level going down, the new calculated required gain is *y*dB, then this gain is applied provided *y* is greater than *x* by the value set in Gain Hysteresis. This feature avoids the condition when the AGC function can fluctuate between a very narrow band of gains leading to audible artifacts. The Gain Hysteresis can be adjusted or disabled by the user.
5. **Noise threshold** determines the level below which if the input signal level falls, the AGC considers it as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every FS and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise is not 'gained up' in the absence of speech. Noise threshold level in the AGC algorithm is programmable from -30dB to -90 dB of full-scale. When AGC Noise Threshold is set to –70dB, –80db, or –90dB, the microphone input Max PGA applicable setting must be greater than or equal to 11.5dB, 21.5dB, or 31.5dB respectively. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When utilizing the AGC noise threshold, it is recommended to configure the 1st order IIR filter as a high-pass filter to achieve best performance. The noise (or silence) detection feature can be entirely disabled by the user.
6. **Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA can be programmed from 0 dB to 58 dB in steps of 0.5 dB.
7. **Hysteresis**, as the name suggests, determines a window around the Noise Threshold which must be exceeded to either detect that the recorded signal is indeed noise or signal. If initially the energy of the recorded signal is greater than the Noise Threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the Noise Threshold by a value given by Hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the Noise Threshold by a value given by the Hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is very close to the Noise threshold) a non-zero hysteresis value should be chosen. The Hysteresis feature can also be disabled.
8. **Debounce Time (Noise and Signal)** determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set Noise Threshold, then the AGC does not increase the input gain to achieve the Target Level. However, to handle audible artifacts which can occur when the energy of the input signal is very close to the Noise Threshold, the AGC checks if the energy of the recorded signal is less than the Noise Threshold for a time greater than the Noise Debounce Time. Similarly the AGC starts increasing the input-signal gain to reach the Target Level when the calculated energy of the input signal is greater than the Noise Threshold. Again, to avoid audible artifacts when the input-signal energy is very close to Noise Threshold, the energy of the input signal needs to continuously exceed the Noise Threshold value for the Signal Debounce Time. If the debounce times are kept very small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the Debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to Noise Threshold. Both noise and signal debounce time can be disabled.
9. The **AGC Noise Threshold Flag** is a read-only flag indicating that the input signal has levels lower

than the Noise Threshold, and thus is detected as noise (or silence). In such a condition the AGC applies a gain of 0 dB.

10. **Gain Applied by AGC** is a ready-only register setting which gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This, along with the Target Setting, can be used to determine the input signal level. In a steady state situation
Target Level (dB) = Gain Applied by AGC (dB) + Input Signal Level (dB)
When the AGC noise threshold flag is set, then the status of gain applied by AGC should be ignored.
11. The **AGC Saturation Flag** is a read-only flag indicating that the ADC output signal has not reached its Target Level. However, the AGC is unable to increase the gain further because the required gain is higher than the Maximum Allowed PGA gain. Such a situation can happen when the input signal has very low energy and the Noise Threshold is also set very low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.
12. The **ADC Saturation Flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC Target Level is kept very high and the energy in the input signal increases faster than the Attack Time.
13. An **AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low pass filter is in the form of a first-order IIR filter. Three 8-bit registers are used to form the 24-bit digital coefficient as shown on the register map. In this way, a total of 9 registers are programmed to form the 3 IIR coefficients. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (2)$$

Where:

Coefficient N0 can be programmed by writing into B40_P1_R12, B40_P1_R13, and B40_P1_R14.
Coefficient N1 can be programmed by writing into B40_P1_R16, B40_P1_R17, and B40_P1_R18.
Coefficient D1 can be programmed by writing into B40_P1_R20, B40_P1_R21, and B40_P1_R22.
N0, N1 and D1 are 24-bit 2's complement numbers and their default values implement a low-pass filter with cut-off at 0.002735*ADC_FS .

See Table 2-15 for various AGC programming options. AGC can be used only if analog microphone input is routed to the ADC channel.

Table 2-15. AGC Parameter Settings

Function	Control Register Left ADC	Control Register Right ADC	Bit(s)
AGC enable	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D7
Target Level	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D[6:4]
Gain Hysteresis	Book 0, Page 0, Register 86 (B0_P0_R86)	Book 0, Page 0, Register 94 (B0_P0_R94)	D[1:0]
Hysteresis	Book 0, Page 0, Register 87 (B0_P0_R87)	Book 0, Page 0, Register 95 (B0_P0_R95)	D[7:6]
Noise threshold	Book 0, Page 0, Register 87 (B0_P0_R87)	Book 0, Page 0, Register 95 (B0_P0_R95)	D[5:1]
Max PGA applicable	Book 0, Page 0, Register 88 (B0_P0_R88)	Book 0, Page 0, Register 96 (B0_P0_R96)	D[6:0]
Time constants (attack time)	Book 0, Page 0, Register 89 (B0_P0_R89)	Book 0, Page 0, Register 97 (B0_P0_R97)	D[7:0]
Time constants(decay time)	Book 0, Page 0, Register 90 (B0_P0_R90)	Book 0, Page 0, Register 98 (B0_P0_R98)	D[7:0]
Debounce time (Noise)	Book 0, Page 0, Register 91 (B0_P0_R91)	Book 0, Page 0, Register 99 (B0_P0_R99)	D[4:0]
Debounce time (Signal)	Book 0, Page 0, Register 92 (B0_P0_R92)	Book 0, Page 0, Register 100 (B0_P0_R100)	D[3:0]

Table 2-15. AGC Parameter Settings (continued)

Function	Control Register Left ADC	Control Register Right ADC	Bit(s)
Gain applied by AGC	Book 0, Page 0, Register 93 (B0_P0_R93)	Book 0, Page 0, Register 101 (B0_P0_R101)	D[7:0] (Read Only)
AGC Noise Threshold Flag	Book 0, Page 0, Register 45 (B0_P0_R45) (sticky flag), Book 0, Page 0, Register 47 (B0_P0_R47) (non-sticky flag)	Book 0, Page 0, Register 45 (B0_P0_R45) (sticky flag), Book 0, Page 0, Register 47 (B0_P0_R47) (non-sticky flag)	D[6:5] (Read Only)
AGC Saturation flag	Book 0, Page 0, Register 36 (B0_P0_R36) (sticky flag)	Book 0, Page 0, Register 36 (B0_P0_R36) (sticky flag)	D5, D1 (Read Only)
ADC Saturation flag	Book 0, Page 0, Register 42 (B0_P0_R42) (sticky flag), Book 0, Page 0, Register 43 (B0_P0_R43) (non-sticky flag)	Book 0, Page 0, Register 42 (B0_P0_R42) (sticky flag), Book 0, Page 0, Register 43 (B0_P0_R43) (non-sticky flag)	D[3:2] (Read Only)

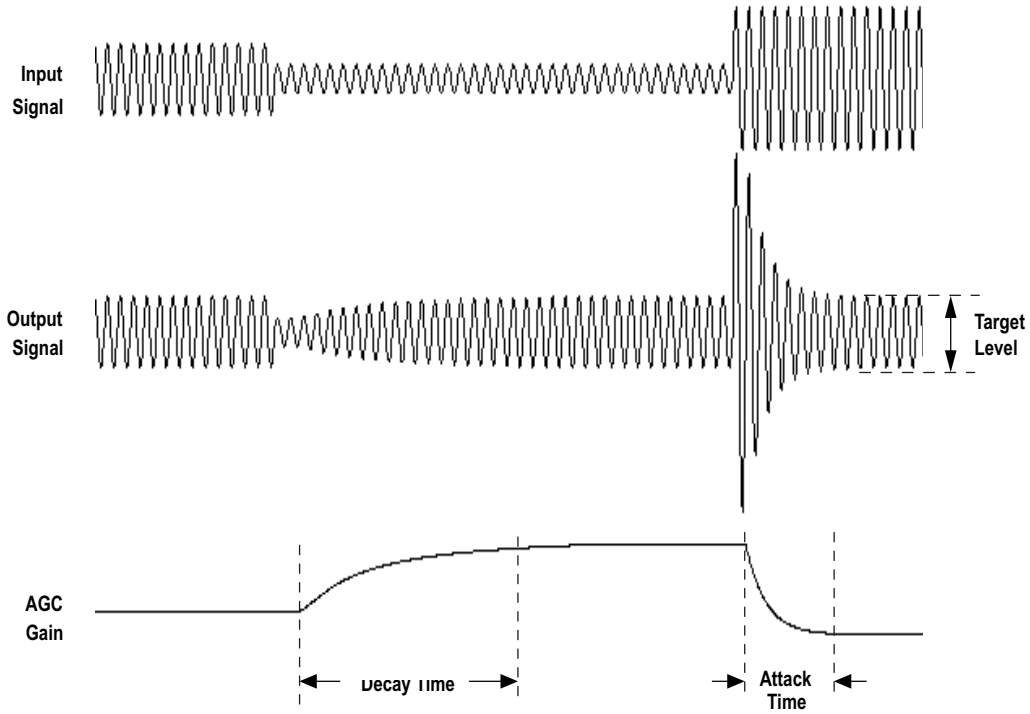


Figure 2-12. AGC Characteristics

2.4.3 ADC Decimation Filtering and Signal Processing Overview

The TLV320AIC3212 ADC channel includes a built-in digital decimation filter to process the oversampled data from the to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

ADC Processing Blocks

The TLV320AIC3212 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Decreasing the use of signal-processing capabilities reduces the power consumed by the device. Table 2-16 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low-group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user programmable coefficients.

Table 2-16. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1[(1)]	Stereo	A	Yes	0	No	128,64,32,16,8,4	7
PRB_R2	Stereo	A	Yes	5	No	128,64,32,16,8,4	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64,32,16,8,4	8
PRB_R4	Left	A	Yes	0	No	128,64,32,16,8,4	4
PRB_R5	Left	A	Yes	5	No	128,64,32,16,8,4	4
PRB_R6	Left	A	Yes	0	25-Tap	128,64,32,16,8,4	4
PRB_R7	Stereo	B	Yes	0	No	64,32,16,8,4,2	3
PRB_R8	Stereo	B	Yes	3	No	64,32,16,8,4,2	4
PRB_R9	Stereo	B	Yes	0	17-Tap	64,32,16,8,4,2	4
PRB_R10	Left	B	Yes	0	No	64,32,16,8,4,2	2
PRB_R11	Left	B	Yes	3	No	64,32,16,8,4,2	2
PRB_R12	Left	B	Yes	0	17-Tap	64,32,16,8,4,2	2
PRB_R13	Stereo	C	Yes	0	No	32,16,8,4,2,1	3
PRB_R14	Stereo	C	Yes	5	No	32,16,8,4,2,1	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32,16,8,4,2,1	4
PRB_R16	Left	C	Yes	0	No	32,16,8,4,2,1	2
PRB_R17	Left	C	Yes	5	No	32,16,8,4,2,1	2
PRB_R18	Left	C	Yes	0	25-Tap	32,16,8,4,2,1	2

(1) Default

2.4.3.1 Signal Processing Blocks – Details

2.4.3.1.1 1st order IIR, AGC, Filter A

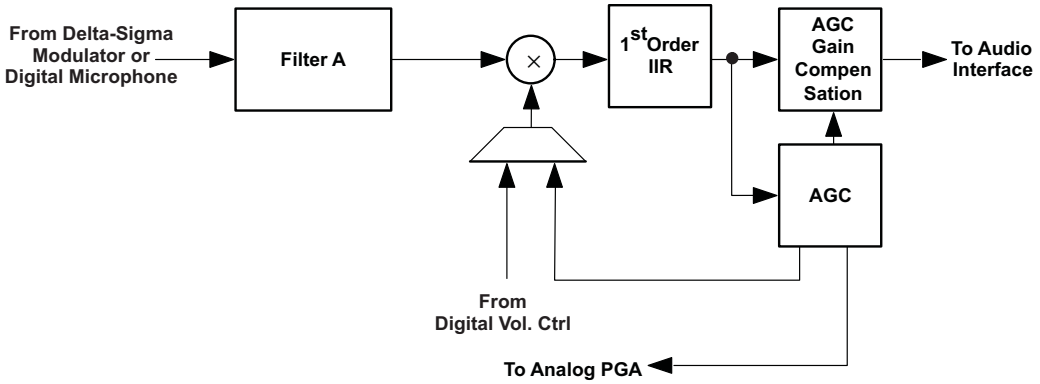


Figure 2-13. Signal Chain for PRB_R1 and PRB_R4

2.4.3.1.2 5 Biquads, 1st order IIR, AGC, Filter A

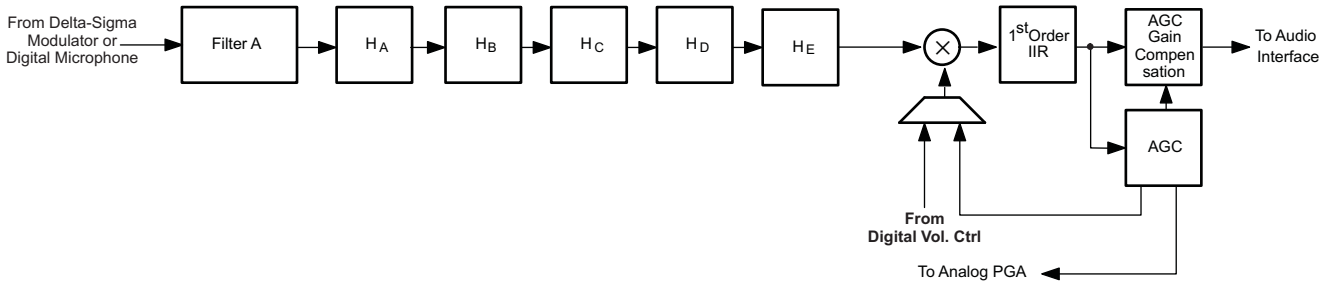


Figure 2-14. Signal Chain PRB_R2 and PRB_R5

2.4.3.1.3 25 Tap FIR, 1st order IIR, AGC, Filter A

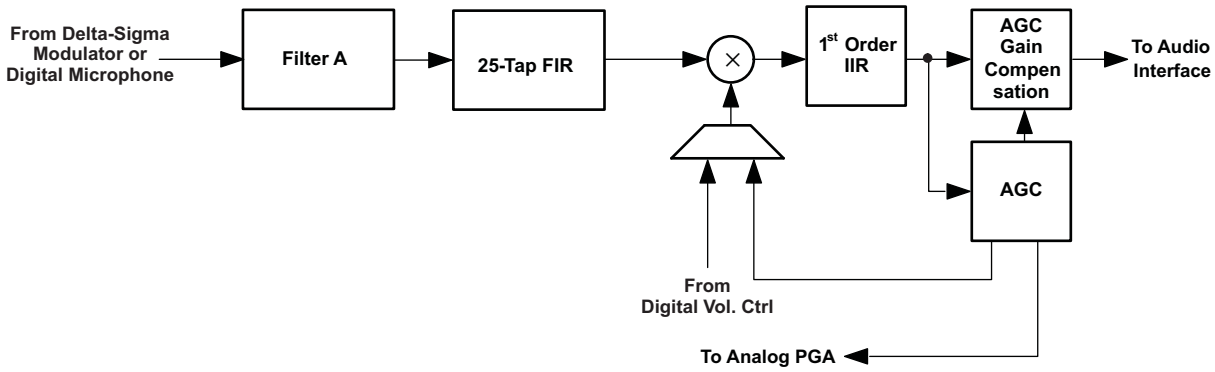


Figure 2-15. Signal Chain for PRB_R3 and PRB_R6

2.4.3.1.4 1st order IIR, AGC, Filter B

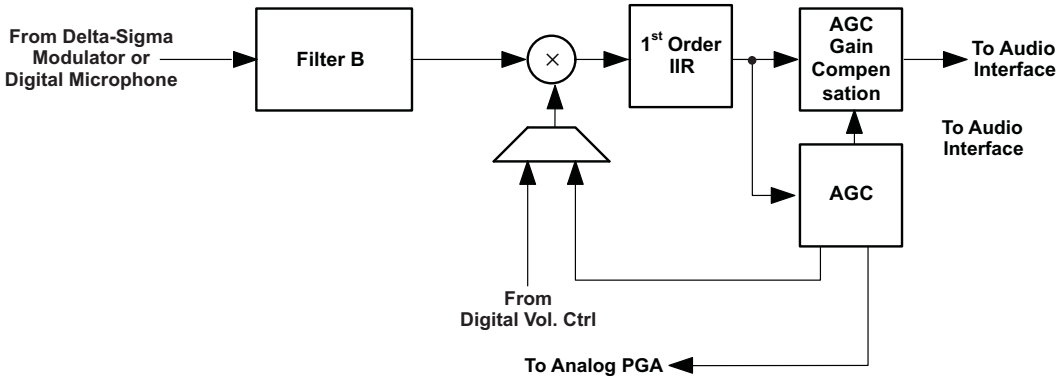


Figure 2-16. Signal Chain for PRB_R7 and PRB_R10

2.4.3.1.5 3 Biquads, 1st order IIR, AGC, Filter B

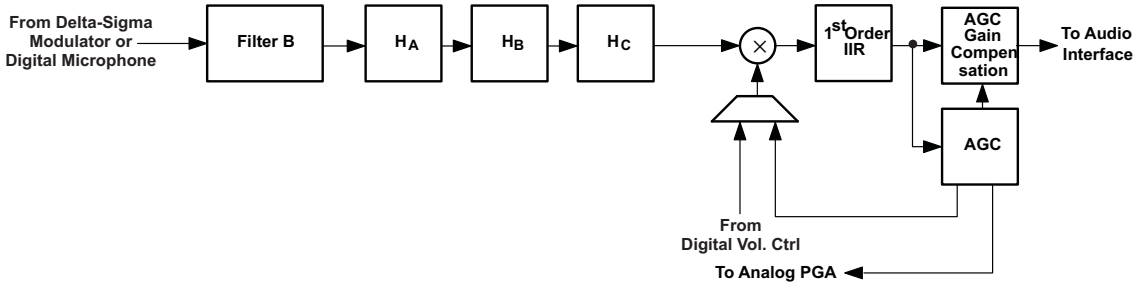


Figure 2-17. Signal Chain for PRB_R8 and PRB_R11

2.4.3.1.6 17 Tap FIR, 1st order IIR, AGC, Filter B

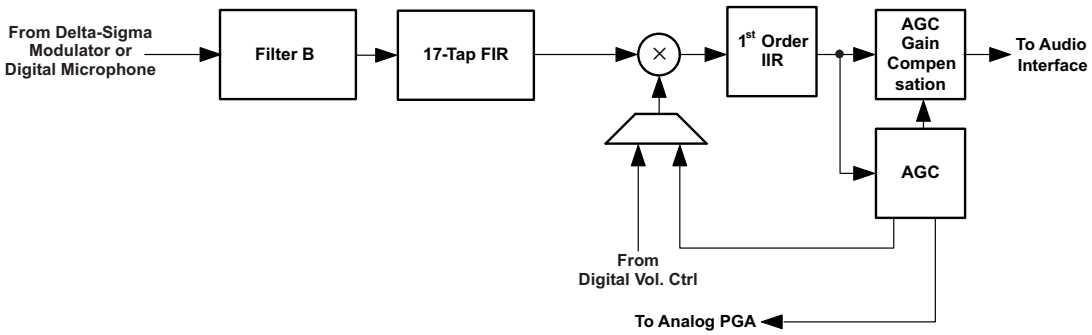


Figure 2-18. Signal Chain for PRB_R9 and PRB_R12

2.4.3.1.7 1st order IIR, AGC, Filter C

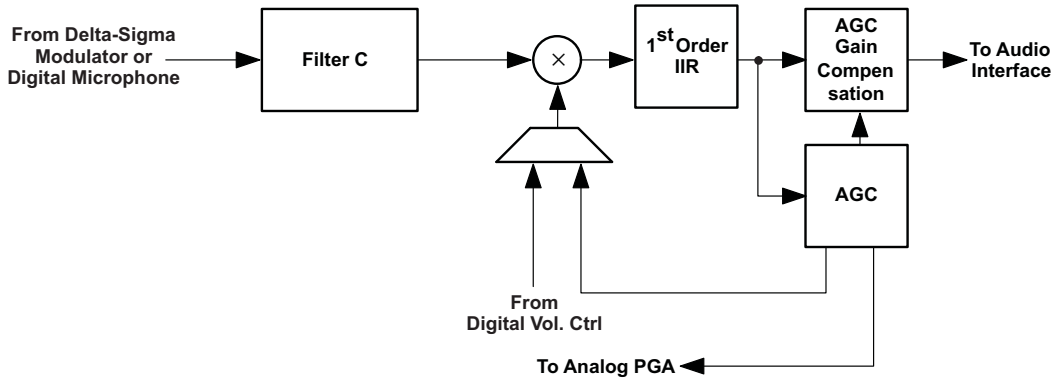


Figure 2-19. Signal Chain for PRB_R13 and PRB_R16

2.4.3.1.8 5 Biquads, 1st order IIR, AGC, Filter C

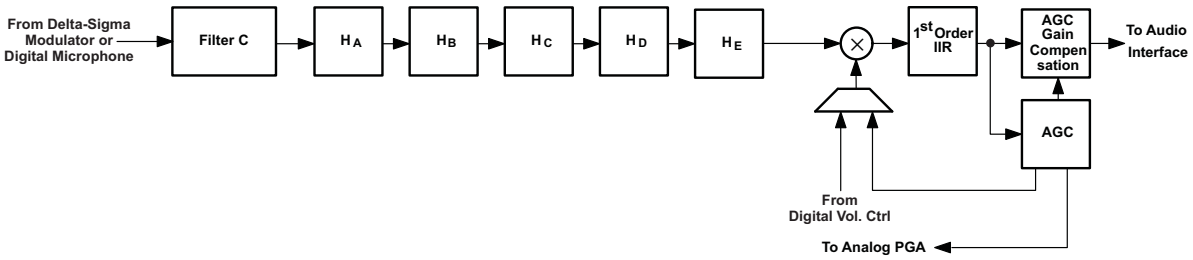


Figure 2-20. Signal Chain for PRB_R14 and PRB_R17

2.4.3.1.9 25 Tap FIR, 1st order IIR, AGC, Filter C

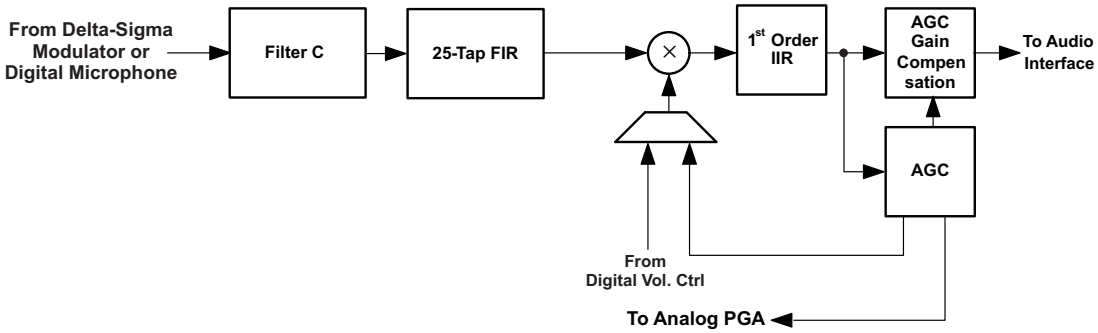


Figure 2-21. Signal for PRB_R15 and PRB_R18

2.4.3.2 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A 1st-order IIR filter is always available, and is useful to efficiently filter out possible DC components of the signal. Up to 5 biquad section or alternatively up to 25-tap FIR filters are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering see Section 2.4.3.5.7 below.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see Section 5.14.

2.4.3.2.1 1st Order IIR Section

The transfer function for the first order IIR Filter is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (3)$$

The frequency response for the 1st order IIR Section with default coefficients is flat at a gain of 0dB. Details on ADC coefficient default values are given in Section 5.14.

Table 2-17. ADC 1st order IIR Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
1st Order IIR	N0	C4 (B40_P1_R24-R26)	C36 (B40_P2_R32-R34)
	N1	C5 (B40_P1_R29-R30)	C37 (B40_P2_R36-R38)
	D1	C6 (B40_P1_R32-R34)	C39 (B40_P2_R40-R42)

2.4.3.2.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2 * N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2 * D_1 z^{-1} - D_2 z^{-2}} \quad (4)$$

The frequency response for each of the biquad section with default coefficients is flat at a gain of 0dB. Details on ADC coefficient default values are given in Section 5.14.

Table 2-18. ADC Biquad Filter Coefficients

Filter	FIlter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
BIQUAD A	N0	C7 (B40_P1_R36-R38)	C39 (B40_P2_R44-R46)
	N1	C8 (B40_P1_R40-R42)	C40 (B40_P2_R48-R50)
	N2	C9 (B40_P1_R44-R46)	C41 (B40_P2_R52-R54)
	D1	C10 (B40_P1_R48-R50)	C42 (B40_P2_R56-R58)
	D2	C11 (B40_P1_R52-R54)	C43 (B40_P2_R60-R62)
BIQUAD B	N0	C12 (B40_P1_R56-R58)	C44 (B40_P2_R64-R66)
	N1	C13 (B40_P1_R60-R62)	C45 (B40_P2_R68-R70)
	N2	C14 (B40_P1_R64-R66)	C46 (B40_P2_R72-R74)
	D1	C15 (B40_P1_R68-R70)	C47 (B40_P2_R76-R78)
	D2	C16 (B40_P1_R72-R74)	C48 (B40_P2_R80-R82)
BIQUAD C	N0	C17 (B40_P1_R76-R78)	C49 (B40_P2_R84-R86)
	N1	C18 (B40_P1_R80-R82)	C50 (B40_P2_R88-R90)
	N2	C19 (B40_P1_R84-R86)	C51 (B40_P2_R92-R94)
	D1	C20 (B40_P1_R88-R90)	C52 (B40_P2_R96-R98)
	D2	C21 (B40_P1_R92-R94)	C53 (B40_P2_R100-R102)
BIQUAD D	N0	C22 (B40_P1_R96-R98)	C54 (B40_P2_R104-R106)
	N1	C23 (B40_P1_R100-R102)	C55 (B40_P2_R108-R110)
	N2	C24 (B40_P1_R104-R106)	C56 (B40_P2_R112-R114)
	D1	C25 (B40_P1_R108-R110)	C57 (B40_P2_R116-R118)
	D2	C26 (B40_P1_R112-R114)	C58 (B40_P2_R120-R122)
BIQUAD E	N0	C27 (B40_P1_R116-R118)	C59 (B40_P2_R124-R126)
	N1	C28 (B40_P1_R120-R122)	C60 (B40_P3_R8-R10)
	N2	C29 (B40_P1_R124-R126)	C61 (B40_P3_R12-R14)
	D1	C30 (B40_P2_R8-R10)	C62 (B40_P3_R16-R18)
	D2	C31 (B40_P2_R12-R14)	C63 (B40_P3_R20-R22)

2.4.3.2.3 FIR Section

Six of the available ADC processing blocks offer FIR filters for signal processing. PRB_R9 and PRB_R12 feature a 20-tap FIR filter while the processing blocks PRB_R3, PRB_R6, PRB_R15 and PRB_R18 feature a 25-tap FIR filter

$$H(z) = \sum_{n=0}^{M} Fir_n z^{-n}$$

$$M = 24, \text{for PRB\_R3, PRB\_R6, PRB\_R15 and PRB\_R18}$$

$$M = 19, \text{for PRB\_R9 and PRB\_R12} \quad (5)$$

The coefficients of the FIR filters are 24-bit 2's complement format and correspond to the ADC coefficient space as listed below. There is no default transfer function for the FIR filter. When the FIR filter gets used all applicable coefficients must be programmed.

Table 2-19. ADC FIR Filter Coefficients

Filter	FIlter Coefficient Left ADC Channel	Filter Coefficient Right ADC Channel
Fir0	C7 (B40_P1_R36-R38)	C39 (B40_P2_R44-R46)
Fir1	C8 (B40_P1_R40-R42)	C40 (B40_P2_R48-R50)
Fir2	C9 (B40_P1_R44-R46)	C41 (B40_P2_R52-R54)
Fir3	C10 (B40_P1_R48-R50)	C42 (B40_P2_R56-R58)
Fir4	C11 (B40_P1_R52-R54)	C43 (B40_P2_R60-R62)
Fir5	C12 (B40_P1_R56-R58)	C44 (B40_P2_R64-R66)
Fir6	C13 (B40_P1_R60-R62)	C45 (B40_P2_R68-R70)
Fir7	C14 (B40_P1_R64-R66)	C46 (B40_P2_R72-R74)
Fir8	C15 (B40_P1_R68-R70)	C47 (B40_P2_R76-R78)
Fir9	C16 (B40_P1_R72-R74)	C48 (B40_P2_R80-R82)
Fir10	C17 (B40_P1_R76-R78)	C49 (B40_P2_R84-R86)
Fir11	C18 (B40_P1_R80-R82)	C50 (B40_P2_R88-R90)
Fir12	C19 (B40_P1_R84-R86)	C51 (B40_P2_R92-R94)
Fir13	C20 (B40_P1_R88-R90)	C52 (B40_P2_R96-R98)
Fir14	C21 (B40_P1_R92-R94)	C53 (B40_P2_R100-R102)
Fir15	C22 (B40_P1_R96-R98)	C54 (B40_P2_R104-R106)
Fir16	C23 (B40_P1_R100-R102)	C55 (B40_P2_R108-R110)
Fir17	C24 (B40_P1_R104-R106)	C56 (B40_P2_R112-R114)
Fir18	C25 (B40_P1_R108-R110)	C57 (B40_P2_R116-R118)
Fir19	C26 (B40_P1_R112-R114)	C58 (B40_P2_R120-R122)
Fir20	C27 (B40_P1_R116-R118)	C59 (B40_P2_R124-R126)
Fir21	C28 (B40_P1_R120-R122)	C60 (B40_P3_R8-R10)
Fir22	C29 (B40_P1_R124-R126)	C61 (B40_P3_R12-R14)
Fir23	C30 (B40_P2_R8-R10)	C62 (B40_P3_R16-R18)
Fir24	C31 (B40_P2_R12-R14)	C63 (B40_P3_R20-R22)

2.4.3.3 Decimation Filter

The TLV320AIC3212 offers 3 different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR*Fs to the final output sampling rate of Fs. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B and C.

2.4.3.3.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance the oversampling ratio must be set to 128. Please also see the PowerTune chapter for details on performance and power in dependency of AOSR.

Filter A can also be used for 96kHz at an AOSR of 64.

Table 2-20. ADC Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…64Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…32Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.1	dB

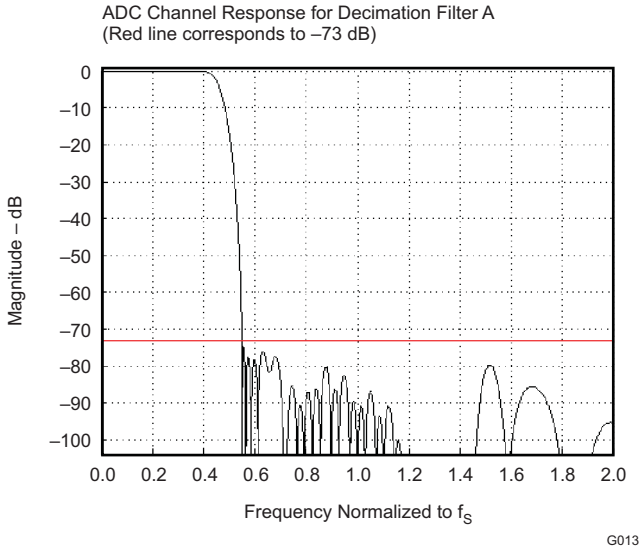


Figure 2-22. ADC Decimation Filter A, Frequency Response

2.4.3.3.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96kHz at a oversampling ratio of 64.

Table 2-21. ADC Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39Fs	±0.077	dB
Filter Gain Stop Band	0.60Fs…32Fs	–46	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39Fs	0.076	dB
Pass Band Ripple, 44.1 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.11	dB

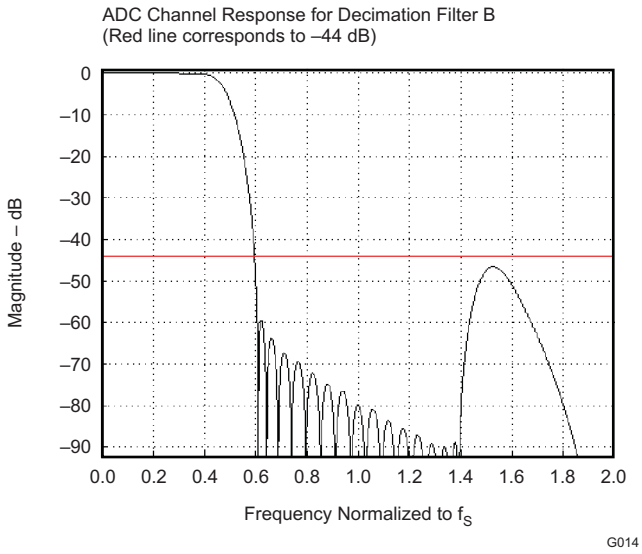


Figure 2-23. ADC Decimation Filter B, Frequency Response

2.4.3.3.3 Decimation Filter C

Filter type C along with AOSR of 32 is specially designed for 192ksps operation for the ADC. The pass band which extends up to 0.11*Fs (corresponds to 21kHz), is suited for audio applications.

Table 2-22. ADC Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11Fs	0…0.11Fs	±0.033	dB
Filter Gain from 0.28Fs to 16Fs	0.28Fs…16Fs	–60	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 44.1 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 192 ksps	0…20kHz	0.086	dB

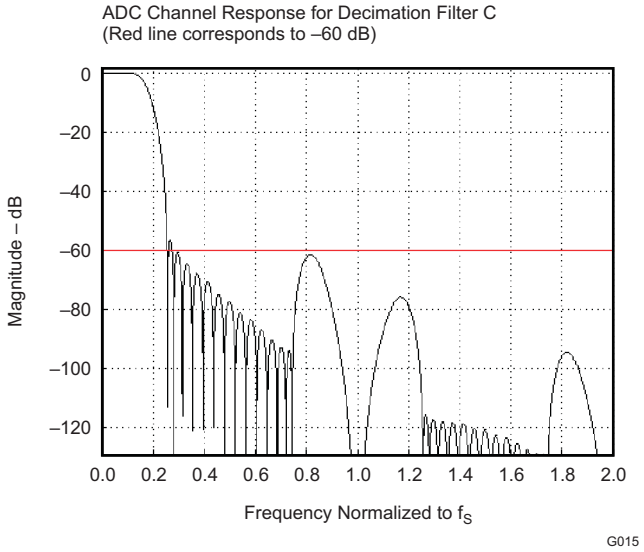


Figure 2-24. ADC Decimation Filter C, Frequency Response

2.4.3.4 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface once every cycle of Fs,ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

2.4.3.5 ADC Special Functions

2.4.3.5.1 Microphone Bias

The TLV320AIC3212 has two built-in low noise Microphone Bias pins for electret-condenser microphones: MICBIAS and MICBIAS_EXT. Typically, MICBIAS is utilized for onboard microphones, while MICBIAS_EXT provides a microphone bias for inserted headsets. Each bias amplifier can support up to 3mA of load current to support multiple microphones. Each bias amplifier has been designed to provide a combination of high PSRR, low noise and programmable bias voltages to allow the user to fine tune the biasing to specific microphone combinations. To support a wide range of bias voltages, the bias amplifier can work off either a low analog supply or the higher AVDD3_33 analog supply.

Table 2-23. MICBIAS Voltage Control

B0_P1_R51_D[1:0]	B0_P1_R8_D2	MICBIAS Voltage (without load)
00	0	1.62V
00	1	1.35V
01	0	2.4V
01	1	2.0V
10	0	2.5V
10	1	3.0V
11	X	AVDD3_33

Table 2-24. MICBIAS_EXT Voltage Control

B0_P1_R51_D[5:4]	B0_P1_R8_D2	MICBIAS Voltage (without load)
00	0	1.62V
00	1	1.35V
01	0	2.4V
01	1	2.0V
10	0	2.5V
10	1	3.0V
11	X	AVDD3_33

2.4.3.5.2 Digital Microphone Function

In addition to supporting analog microphones, the TLV320AIC3212 also interfaces to digital microphones.

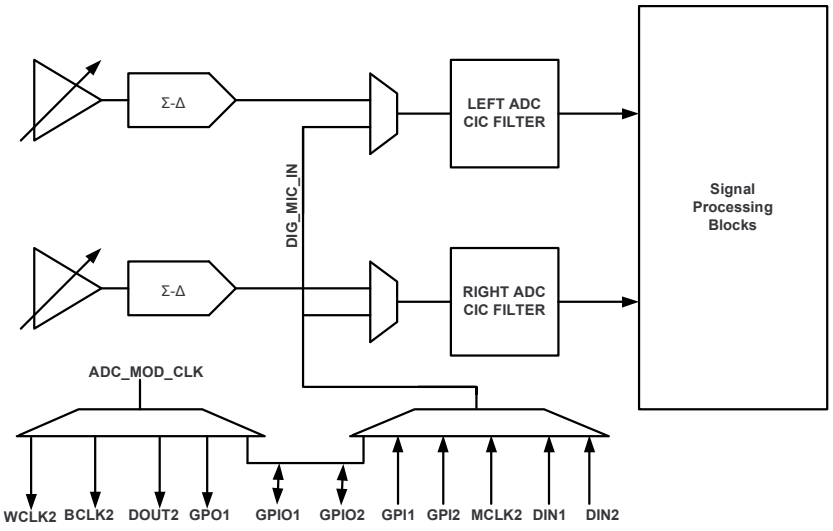


Figure 2-25. Digital Microphone in TLV320AIC3212

The TLV320AIC3212 outputs internal clock ADC_MOD_CLK on the GPIO1 pin (B0_P4_R86_D[6:2]='01010'), the GPIO2 pin (B0_P4_R87_D[6:2]='01010'), the GPO1 pin (B0_P4_R96_D[4:1]='0111'), the WCLK2 pin (B0_P4_R69_D[5:2]='1010'), the BCLK2 pin (B0_P4_R70_D[5:2]='1010'), or DOUT2 pin (B0_P4_R71_D[4:1]='1010'). This clock can be connected to the external digital microphone device. The single-bit output of the external digital microphone device can be connected to GPIO1 (B0_P4_R86_D[6:2]='00001'), GPIO2 (B0_P4_R87_D[6:2]='00001'), GPI1 (B0_P4_R91_D[2:1]='01'), GPI2 (B0_P4_R92_D[5:4]='01'), MCLK2 (B0_P4_R82_D[5:4]='01'), DIN1 (B0_P4_R68_D[6:5]='01'), or DIN2 (B0_P4_R72_D[6:5]='01') pins. To set up the left and right ADC channels to accept digital microphone data, B0_P0_R81_D[5:4] and B0_P0_R81_D[3:2] should be configured for digital microphones. Internally the TLV320AIC3212 latches the steady value of data on the rising edge of ADC_MOD_CLK for the Left ADC channel, and the steady value of data on falling edge for the Right ADC channel, and the pins from which these channels are read are defined by the Digital Microphone Input Pin Control register (B0_P4_R101).

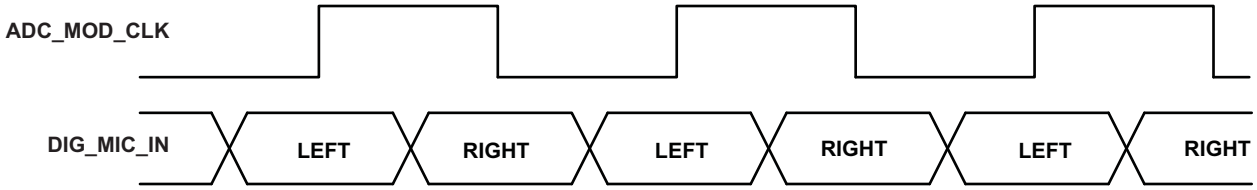


Figure 2-26. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

A typical external circuit connection for the digital microphone is shown in Figure 2-27. Typical circuit diagram is one possibility for connecting digital microphones. All pin assignment options for digital microphones are described in Rows E and J of the pin muxing tables in Table 2-2 and Table 2-3 (located in Section 2.2.3). Depending on the performance of the digital microphone (e.g. PSRR) and the noise level on the IOVDD power supply, some additional filtering may be needed for Vmic near the digital microphone for best performance.

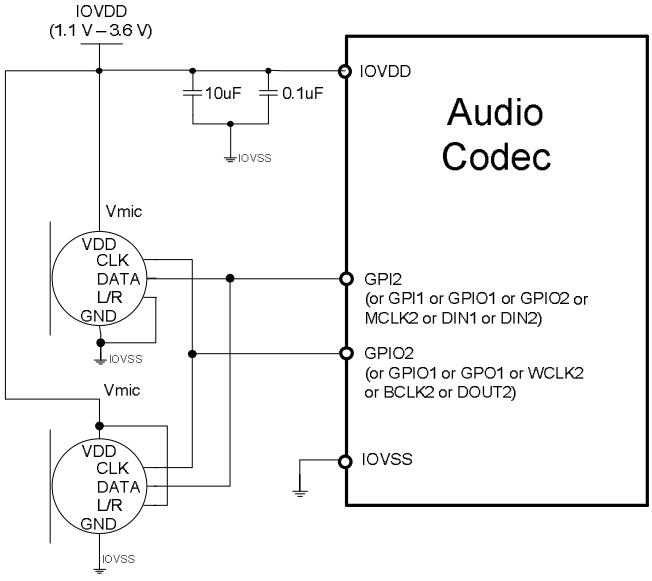


Figure 2-27. Typical Digital Microphone External Circuitry

2.4.3.5.3 Channel-to-Channel Phase Adjustment

The TLV320AIC3212 has a built-in feature to fine-adjust the phase between the stereo ADC record signals. The phase compensation is particularly helpful to adjust delays when using dual microphones for noise cancellation etc. This delay can be controlled in fine amounts in the following fashion.

Delay(7:0) = B0_P0_R85_D[7:0]

Where

$$RIGHT\_ADC\_PHASE\_COMP(t) = RIGHT\_ADC\_OUT(t - t_{pr}) \quad (6)$$

where

$$t_{pr} = \frac{(Delay(4:0) + Delay(6:5) * AOSR * k_f)}{AOSR * ADC\_FS} \quad (7)$$

Where k_f is a function of the decimation filter:

Decimation Filter Type	k_f
A	0.25
B	0.5
C	1

and

$$LEFT\_ADC\_PHASE\_COMP(t) = LEFT\_ADC\_OUT(t - t_{pl}) \quad (8)$$

Where

$$t_{pl} = \frac{Delay(7)}{AOSR * ADC\_FS} \quad (9)$$

2.4.3.5.4 DC Measurement

The TLV320AIC3212 supports a highly flexible DC measurement feature using the high resolution oversampling and noise-shaping ADC. This mode can be used when the particular ADC channel is not used for the voice/audio record function. This mode can be enabled by programming B0_P0_R102_D[7:6]. The converted data is 24-bits, using 2.22 numbering format. The value of the converted data for the left-channel ADC can be read back from B0_P0_R104-R106 and for the right-channel ADC from B0_P0_R107-R109. Before reading back the converted data, B0_P0_R103_D6 must be programmed to latch the converted data into the read-back register. After the converted data is read back, B0_P0_R103_D6 must be reset to 0 immediately. In DC measurement mode, two measurement methods are supported.

Mode A

In DC-measurement mode A, a variable-length averaging filter is used. The length of the averaging filter D, can be programmed from 1 to 20 by programming B0_P0_R102_D[4:0]. To choose mode A, B0_P0_R102_D5 must be programmed to 0.

Mode B

To choose mode B, B0_P0_R102_D5 must be programmed to 1. In DC-measurement mode B, a first-order IIR filter is used. The coefficients of this filter are determined by D, B0_P0_R102_D[4:0]. The nature of the filter is given in the table below

Table 2-25. DC Measurement Bandwidth Settings

D: B0_P0_R102_D[4:0]	–3 dB BW (kHz)	–0.5 dB BW (kHz)
1	688.44	236.5
2	275.97	96.334
3	127.4	44.579
4	61.505	21.532
5	30.248	10.59
6	15.004	5.253
7	7.472	2.616
8	3.729	1.305
9	1.862	652
10	931	326
11	465	163
12	232.6	81.5
13	116.3	40.7
14	58.1	20.3
15	29.1	10.2
16	14.54	5.09
17	7.25	2.54
18	3.63	1.27
19	1.8	0.635
20	0.908	0.3165

By programming B0_P0_R103_D5 to ‘1’, the averaging filter is periodically reset after 2^R number of ADC_MOD_CLK, where R is programmed in B0_P0_R103_D[4:0]. When B0_P0_R103_D5 is set to 1 then the value of D should be less than the value of R. When B0_P0_R103_D5 is programmed as 0 the averaging filter is never reset.

2.4.3.5.5 Fast Charging AC Capacitors

The value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage. To enable quick charging, the TLV320AIC3212 has modes to speed up the charging of the coupling capacitor. These are controlled by controlling B0_P1_R71_D[1:0].

2.4.3.5.6 Anti Thump

For normal voice or audio recording, the analog input pins of the TLV320AIC3212, must be AC-coupled to isolate the DC-common mode voltage of the driving circuit from the common-mode voltage of the TLV320AIC3212.

When the analog inputs are not selected for any routing, the input pins are 3-stated and the voltage on the pins is undefined. When the unselected inputs are selected for any routing, the input pins must charge from the undefined voltage to the input common-mode voltage. This charging signal can cause audible artifacts. In order to avoid such artifacts the TLV320AIC3212 also incorporates anti-thump circuitry to allow connection of unused inputs to the common-mode level. This feature is disabled by default, and can be enabled by writing the appropriate values into B0_P1_R58_D[7:0]. The use of this feature in combination with the PTM_R1 setting in B0_P0_R61 when the ADC channel is powered down causes the additional current consumption of 700µA from AVdd and 125µA from DVdd in the sleep mode.

2.4.3.5.7 Adaptive Filtering

After the ADC is running, the filter coefficients are locked and cannot be accessed for read or write. However the TLV320AIC3212 offers an adaptive filter mode as well. Setting B40_P0_R1_D2=1 turns on double buffering of the coefficients. In this mode filter coefficients can be updated through the host and activated without stopping and restarting the ADC, enabling advanced adaptive filtering applications.

To support double buffering, all coefficients are stored in two buffers (Buffer A and B). When the ADC is running and adaptive filtering mode is turned on, setting the control bit B40_P0_R1_D0=1 switches the coefficient buffers at the next start of a sampling period. The bit reverts to 0 after the switch occurs. At the same time, the flag B40_P0_R1_D1 toggles.

The flag in B40_P0_R1_D1 indicates which of the two buffers is actually in use.

For B40_P0_R1_D1=0: Buffer A is in use by the ADC engine. For B40_P0_R1_D1=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the ADC, regardless to which buffer the coefficients have been written.

ADC running	Flag, B40_P0_R1_D1	Coefficient Buffer in use	Writing to	Will update
No	0	None	C4, Buffer A	C4, Buffer A
No	0	None	C4, Buffer B	C4, Buffer B
Yes	0	Buffer A	C4, Buffer A	C4, Buffer B
Yes	0	Buffer A	C4, Buffer B	C4, Buffer B
Yes	1	Buffer B	C4, Buffer A	C4, Buffer A
Yes	1	Buffer B	C4, Buffer B	C4, Buffer A

2.4.3.6 Setup

The following discussion is intended to guide a system designer through the steps necessary to configure the TLV320AIC3212 ADC.

Step 1

The system clock source (master clock) and the targeted ADC sampling frequency must be identified.

The oversampling ratio (OSR) of the TLV320AIC3212 must be configured to match the properties of the digital microphone.

Based on the identified filter type and the required signal processing capabilities the appropriate processing block can be determined from the list of available processing blocks (PRB_R1 to PRB_R18) (See Table 2-16).

Based on the available master clock, the chosen OSR and the targeted sampling rate, the clock divider values NADC and MADC can be determined. If necessary the internal PLL will add a large degree of flexibility.

In summary, ADC_CLKIN which is either derived directly from the system clock source or from the internal PLL, divided by MADC, NADC and AOSR, must be equal to the ADC sampling rate ADC_FS. The source of the ADC_CLKIN clock signal can be shared with the DAC clock generation block, or can be derived from a separate clock source compared to the DAC_CLKIN signal.

ADC_CLKIN = NADC*MADC*AOSR*ADC_FS

To a large degree NADC and MADC can be chosen independently in the range of 1 to 128. In general NADC should be as large as possible as long as the following condition can still be met:

MADC*AOSR/32 ≥ RC

RC is a function of the chosen processing block, and is listed in Table 2-16.

The common mode setting of the device is determined by the available analog power supply and the desired PowerTune mode, this common mode setting is shared across DAC (input common mode) and analog bypass path.

At this point the following device specific parameters are known:

PRB_Rx, AOSR, NADC, MADC, common mode setting

Additionally if the PLL is used the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed between powering the device up and reading data from the device:

Define starting point:	Set register page to Book 0, Page 0 Initiate SW Reset
Program Clock Settings	Program PLL clock pre-divider (PLL_CLKIN_DIV) and PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program the processing block to be used

At this point, at the latest, analog power supply must be applied to the device

Program Analog Blocks	Set register Page to Book 0, Page 1 Disable coarse AVdd generation Enable Master Analog Power Control

A detailed example can be found in Chapter 4.

2.5 DAC

The TLV320AIC3212 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3212 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3212 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3212 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Usable in single-ended stereo or differential mono mode
  - Analog volume setting with a range of -6 to +14 dB
- 2 line-out amplifiers
  - Usable in single-ended stereo or differential mono mode
- 2 Class-D speaker amplifiers
  - Usable in stereo differential mode
  - Analog volume control with a settings of +6, +12, +18, +24, and +30 dB
- 1 Receiver amplifier
  - Usable in mono differential mode
  - Analog volume setting with a range of -6 to +29 dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3212 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

The TLV320AIC3212 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. The Table 2-26 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 2-26. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	RC Class
PRB_P1(1)	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	5
PRB_P7	B	Stereo	Yes	0	No	No	No	5
PRB_P8	B	Stereo	No	4	Yes	No	No	9
PRB_P9	B	Stereo	No	4	No	No	No	7
PRB_P10	B	Stereo	Yes	6	Yes	No	No	9
PRB_P11	B	Stereo	Yes	6	No	No	No	7
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	5
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	13
PRB_P26	D	Stereo	No	0	No	No	No	1

(1) Default

2.5.1 DAC Processing Blocks – Details

2.5.1.1 3 Biquads, Interpolation Filter A

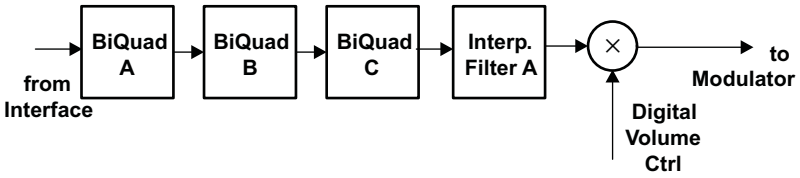


Figure 2-28. Signal Chain for PRB_P1 and PRB_P4

2.5.1.2 6 Biquads, 1st order IIR, DRC, Interpolation Filter A or B

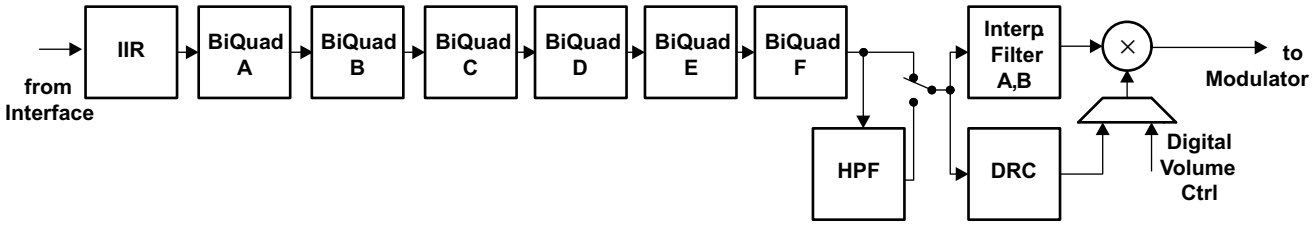


Figure 2-29. Signal Chain for PRB_P2, PRB_P5, PRB_P10 and PRB_P15

2.5.1.3 6 Biquads, 1st order IIR, Interpolation Filter A or B

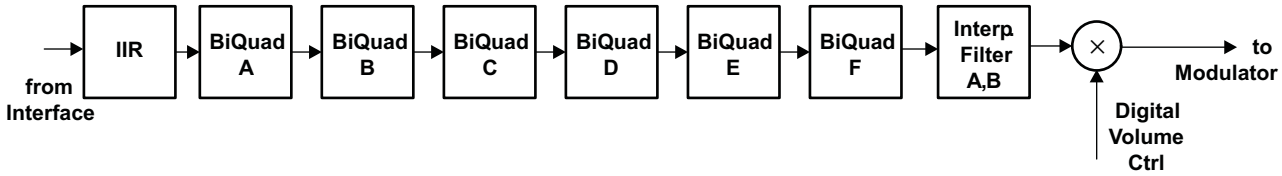


Figure 2-30. Signal Chain for PRB_P3, PRB_P6, PRB_P11 and PRB_P16

2.5.1.4 IIR, Interpolation Filter B or C

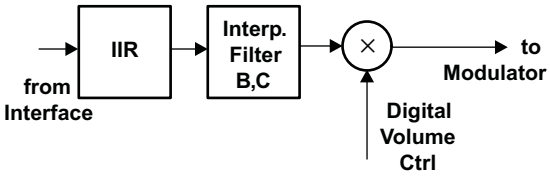


Figure 2-31. Signal Chain for PRB_P7, PRB_P12, PRB_P17 and PRB_P20

2.5.1.5 4 Biquads, DRC, Interpolation Filter B

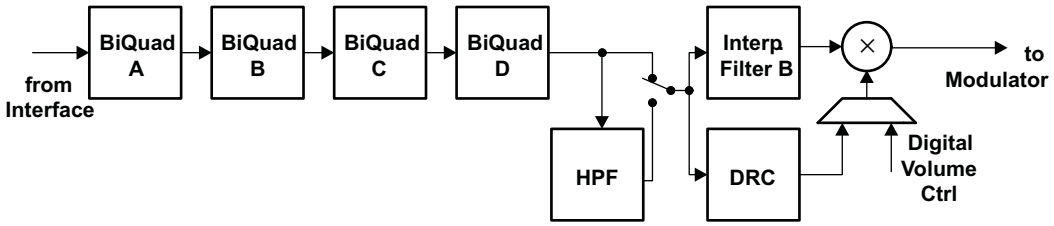


Figure 2-32. Signal Chain for PRB_P8 and PRB_P13

2.5.1.6 4 Biquads, Interpolation Filter B

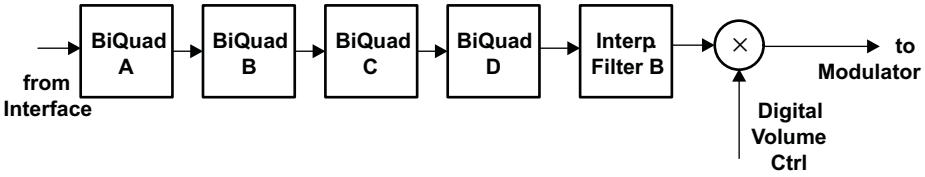


Figure 2-33. Signal Chain for PRB_P9 and PRB_P14

2.5.1.7 4 Biquads, 1st order IIR, DRC, Interpolation Filter B

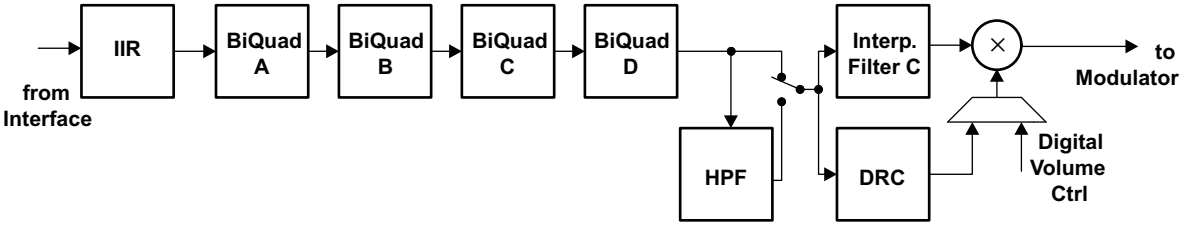


Figure 2-34. Signal Chain for PRB_P18 and PRB_P21

2.5.1.8 4 Biquads, 1st order IIR, Interpolation Filter C

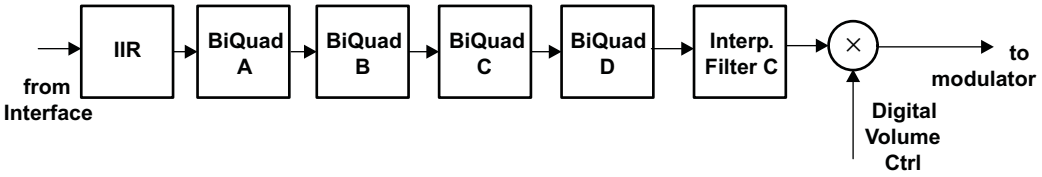


Figure 2-35. Signal Chain for PRB_P19 and PRB_P22

2.5.1.9 2 Biquads, 3D, Interpolation Filter A

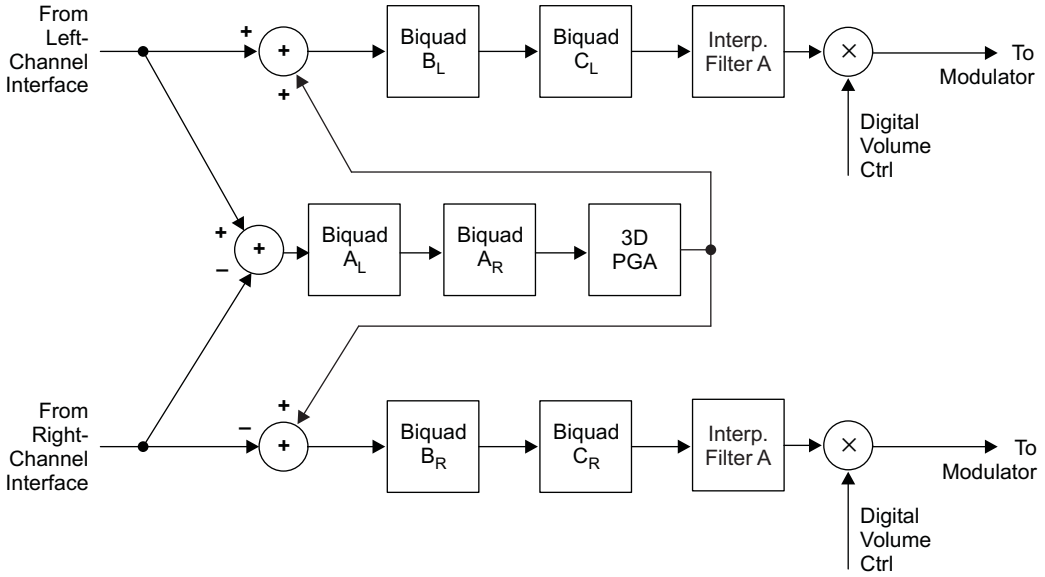


Figure 2-36. Signal Chain for PRB_P23

2.5.1.10 5 Biquads, DRC, 3D, Interpolation Filter A

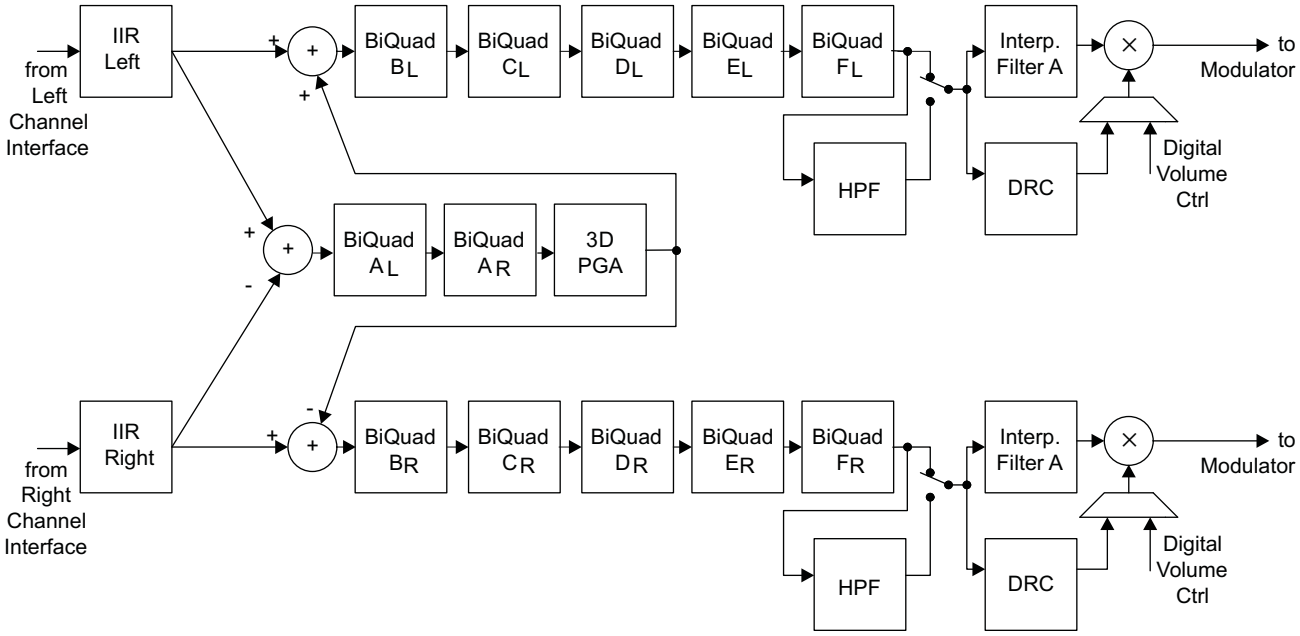


Figure 2-37. Signal Chain for PRB_P24

2.5.1.11 5 Biquads, DRC, 3D, Beep Generator, Interpolation Filter A

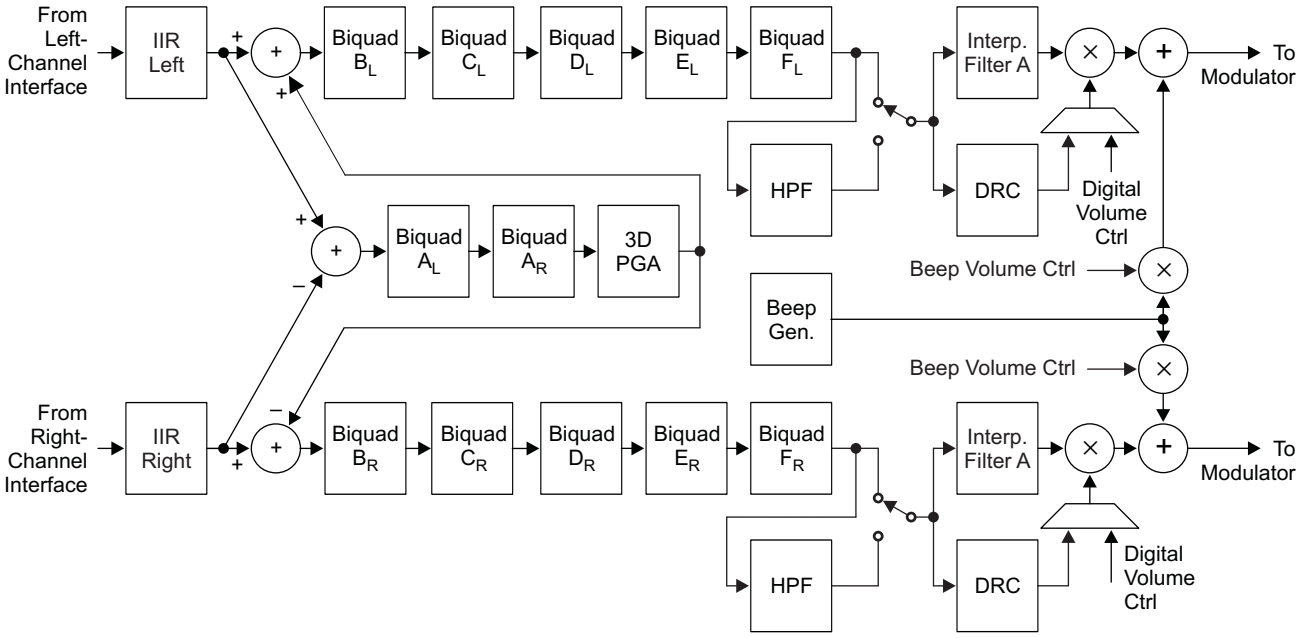


Figure 2-38. Signal Chain for PRB_P25

2.5.1.12 Interpolation Filter D

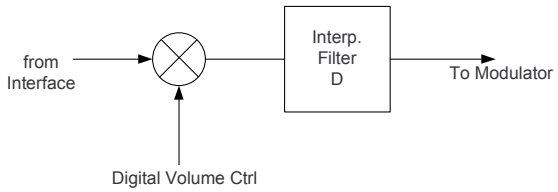


Figure 2-39. Signal Chain for PRB_P26

2.5.2 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. Up to 6 biquad sections are available for specific processing blocks.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering please see Section 2.5.5.3.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see the default values tables in the Register Map section.

2.5.2.1 1st-Order IIR Section

The IIR is of first-order and its transfer function is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \tag{10}$$

The frequency response for the 1st order IIR Section with default coefficients is flat. Details on DAC coefficient default values are given in Section 5.16.

Table 2-27. DAC IIR Filter Coefficients

Filter	Filter Coefficient	DAC Coefficient Left Channel	DAC Coefficient Right Channel
1st Order IIR	N0	C65 (B80_P3_R28-R30)	C68 (B80_P3_R40-R42)
	N1	C66 (B80_P3_R32-R34)	C69 (B80_P3_R44-R46)
	D1	C67 (B80_P3_R36-R38)	C70 (B80_P3_R48-R50)

2.5.2.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2*N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2*D_1 z^{-1} - D_2 z^{-2}} \tag{11}$$

The frequency response for each biquad section with default coefficients is flat at a gain of 0dB. Details on DAC coefficient default values are given in Section 5.16.

Table 2-28. DAC Biquad Filter Coefficients

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD A	N0	C1 (B80_P1_R12-R14)	C33 (B80_P2_R20-R22)
	N1	C2 (B80_P1_R16-R18)	C34 (B80_P2_R24-R26)
	N2	C3 (B80_P1_R20-R22)	C35 (B80_P2_R28-R30)
	D1	C4 (B80_P1_R24-R26)	C36 (B80_P2_R32-R34)
	D2	C5 (B80_P1_R28-R30)	C37 (B80_P2_R36-R38)

Table 2-28. DAC Biquad Filter Coefficients (continued)

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD B	N0	C6 (B80_P1_R32-R34)	C38 (B80_P2_R40-R42)
	N1	C7 (B80_P1_R36-R38)	C39 (B80_P2_R44-R46)
	N2	C8 (B80_P1_R40-R42)	C40 (B80_P2_R48-R50)
	D1	C9 (B80_P1_R44-R46)	C41 (B80_P2_R52-R54)
	D2	C10 (B80_P1_R48-R50)	C42 (B80_P2_R56-R58)
BIQUAD C	N0	C11 (B80_P1_R52-R54)	C43 (B80_P2_R60-R62)
	N1	C12 (B80_P1_R56-R58)	C44 (B80_P2_R64-R66)
	N2	C13 (B80_P1_R60-R62)	C45 (B80_P2_R68-R70)
	D1	C14 (B80_P1_R64-R66)	C46 (B80_P2_R72-R74)
	D2	C15 (B80_P1_R68-R70)	C47 (B80_P2_R76-R78)
BIQUAD D	N0	C16 (B80_P1_R72-R74)	C48 (B80_P2_R80-R82)
	N1	C17 (B80_P1_R76-R78)	C49 (B80_P2_R84-R86)
	N2	C18 (B80_P1_R80-R82)	C50 (B80_P2_R88-R90)
	D1	C19 (B80_P1_R84-R86)	C51 (B80_P2_R92-R94)
	D2	C20 (B80_P1_R88-R90)	C52 (B80_P2_R96-R98)
BIQUAD E	N0	C21 (B80_P1_R92-R94)	C53 (B80_P2_R100-R102)
	N1	C22 (B80_P1_R96-R98)	C54 (B80_P2_R104-R106)
	N2	C23 (B80_P1_R100-R102)	C55 (B80_P2_R108-R110)
	D1	C24 (B80_P1_R104-R106)	C56 (B80_P2_R112-R114)
	D2	C25 (B80_P1_R108-R110)	C57 (B80_P2_R116-R118)
BIQUAD F	N0	C26 (B80_P1_R112-R114)	C58 (B80_P2_R120-R122)
	N1	C27 (B80_P1_R116-R118)	C59 (B80_P2_R124-R126)
	N2	C28 (B80_P1_R120-R122)	C60 (B80_P3_R8-R10)
	D1	C29 (B80_P1_R124-R126)	C61 (B80_P3_R12-R14)
	D2	C30 (B80_P2_R8-R10)	C62 (B80_P3_R16-R18)

2.5.2.2.1 3D-PGA

The 3D-PGA attenuation block as used in the processing blocks PRB_P23, PRB_P24 and PRB_P25 can be programmed in the range of -1.0 to +1.0. A value of -1.0 corresponds to 0x7FFFFF in DAC coefficient C32 (B80_P2_R16-R18). A value of 1.0 corresponds to 0x800000 in coefficient C32.

2.5.3 Interpolation Filters

2.5.3.1 Interpolation Filter A

Filter A is designed for an Fs up to 48ksps with a flat passband of 0kHz–20kHz.

Table 2-29. DAC Interpolation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45Fs	±0.015	dB
Filter Gain Stop Band	0.55Fs… 7.455Fs	–65	dB
Filter Group Delay		21/Fs	s

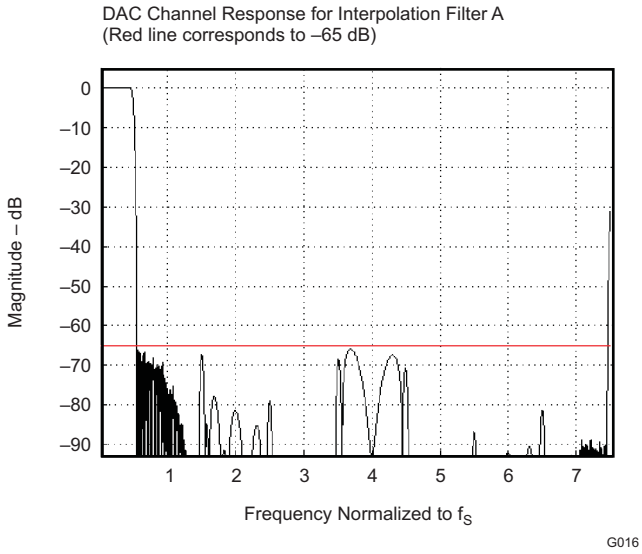


Figure 2-40. DAC Interpolation Filter A, Frequency Response

2.5.3.2 Interpolation Filter B

Filter B is specifically designed for an Fs of above 96ksps. Thus, the flat pass-band region easily covers the required audio band of 0-20kHz.

Table 2-30. DAC Interpolation Filter B, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45Fs	±0.015	dB
Filter Gain Stop Band	0.55Fs… 3.45Fs	–58	dB
Filter Group Delay		18/Fs	s

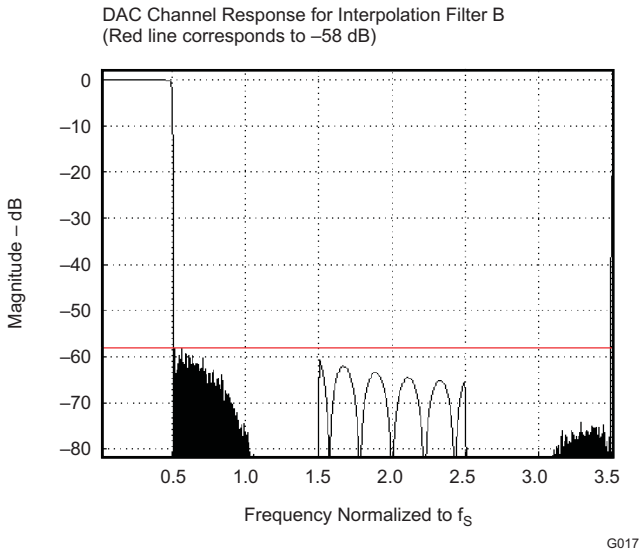


Figure 2-41. Channel Interpolation Filter B, Frequency Response

2.5.3.3 Interpolation Filter C

Filter C is specifically designed for the 192ksps mode. The pass band extends up to 0.40*Fs (corresponds to 80kHz), more than sufficient for audio applications.

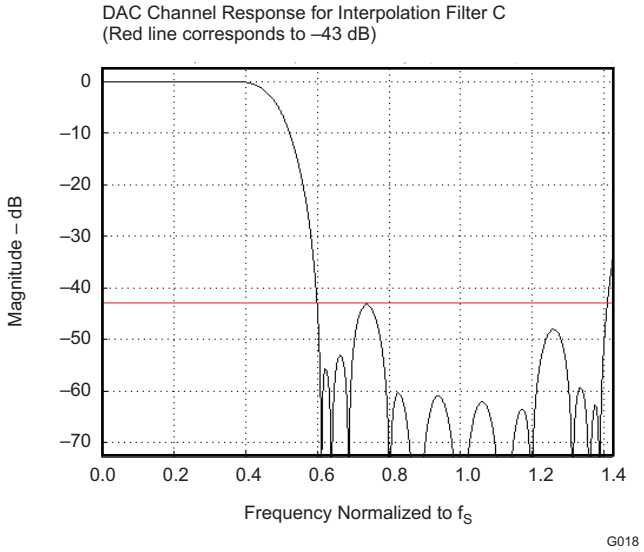


Figure 2-42. DAC Interpolation Filter C, Frequency Response

Table 2-31. DAC Interpolation Filter C, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.35Fs	±0.03	dB
Filter Gain Stop Band	0.60Fs… 1.4Fs	–43	dB
Filter Group Delay		13/Fs	s

2.5.3.4 Interpolation Filter D

Filter D is designed for low-power, low-latency operation.

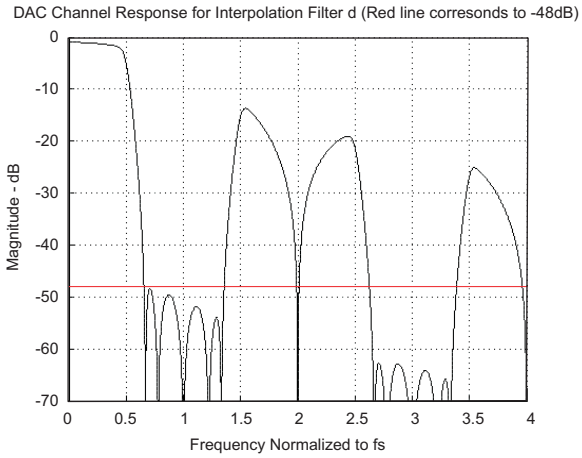


Figure 2-43. DAC Interpolation Filter D, Frequency Response

Table 2-32. DAC Interpolation Filter D, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.4Fs	-1.0	dB
Filter Gain Stop Band	0.65Fs… 1.35Fs	–48	dB
Filter Group Delay		3/Fs	s

2.5.4 DAC Gain Setting

2.5.4.1 PowerTune Modes

As part of the PowerTune strategy, the analog properties of the DAC are adjusted. As a consequence, the full-scale signal swing achieved at the headphone outputs must be adjusted.

Please see Table 2-33 for the proper gain compensation values across the different combinations.

Table 2-33. DAC Gain vs. PowerTune Modes

DAC PowerTune Mode Control	PowerTune Mode	Headphone Gain	
Page 1,Register 3/4, Bits D4-D2)		CM = 0.75V, Gain for 375mV$_{RMS}$ output swing at 0dB full scale input	CM = 0.9V, Gain for 500mV$_{RMS}$ output swing at 0dB full scale input
000	PTM_P3, PTM_P4	0	0
001	PTM_P2	4	4
010	PTM_P1	14	14

2.5.4.2 Digital Volume Control

The TLV320AIC3212 signal processing blocks incorporate a digital volume control block that can control the volume of the playback signal from +24dB to –63.5dB in steps of 0.5dB. These can be controlled by writing to B0_P0_R65 and B0_P0_R66. The volume control of left and right channels by default can be controlled independently, however by programming B0_P0_R64_D[1:0], they can be made interdependent. The volume changes are soft-stepped in steps of 0.5dB to avoid audible artifacts during gain change. The rate of soft-stepping can be controlled by programming B0_P0_R63_D[1:0] to either one step per frame (DAC_FS) or one step per 2 frames. The soft-stepping feature can also be entirely disabled. During soft-stepping the value of the actual applied gain would differ from the programmed gain

in register. The TLV320AIC3212 gives a feedback to the user in form of register readable flag to indicate that soft-stepping is currently in progress. The flags for left and right channels can be read back by reading B0_P0_R38_D4 and B0_P0_R38_D0 respectively. A value of 0 in these flags indicates a soft-stepping operation in progress, and a value of 1 indicates that soft-stepping has completed. A soft-stepping operation comes into effect during a) power-up, when the volume control soft-steps from –63.5dB to programmed gain value b) volume change by user when DAC is powered up and c) power-down, when the volume control block soft-steps to –63.5dB before powering down the channel.

2.5.4.3 Dynamic Range Compression

Typical music signals are characterized by crest factors, the ratio of peak signal power to average signal power, of 12dB or more. In order to avoid audible distortions due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping of peak signals. As a result, during nominal periods, the applied gain is low, causing the perception that the signal is not loud enough. To overcome this problem, the DRC in the TLV320AIC3212 continuously monitors the output of the DAC Digital Volume control to detect its power level w.r.t. 0dB FS. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. This results in sounds more pleasing to the ear as well as sounding louder during nominal periods.

The DRC functionality in the TLV320AIC3212 is implemented by a combination of Processing Blocks in the DAC channel as described in Section 2.5.1.

The DRC can be disabled by writing into B0_P0_R68_D[6:5].

The DRC typically works on the filtered version of the input signal. The input signals have no audio information at DC and extremely low frequencies; however they can significantly influence the energy estimation function in DRC. Also most of the information about signal energy is concentrated in the low frequency region of the input signal.

In order to estimate the energy of the input signal, the signal is first fed to the DRC high-pass filter and then to the DRC low-pass filter. These filters are implemented as first-order IIR filters given by

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (12)$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (13)$$

The coefficients for these filters are 24-bits wide in two's-complement and are user programmable through register write as given in Table 2-34, and coefficient default values are summarized in Section 5.16.

Table 2-34. DRC HPF and LPF Coefficients

Coefficient	Location
HPF N0	C71 (B80_P3_R52-R55)
HPF N1	C72 (B80_P3_R56-R59)
HPF D1	C73 (B80_P3_R60-R63)
LPF N0	C74 (B80_P3_R64-R67)
LPF N1	C75 (B80_P3_R68-R71)
LPF D1	C76 (B80_P3_R72-R75)

The default values of these coefficients implement a high-pass filter with a cut-off at 0.00166*DAC_FS, and a low-pass filter with a cutoff at 0.00033*DAC_FS.

The output of the DRC high-pass filter is fed to the Processing Block selected for the DAC Channel. The absolute value of the DRC-LPF filter is used for energy estimation within the DRC.

The gain in the DAC Digital Volume Control is controlled by B0_P0_R65-R66. When the DRC is enabled, the applied gain is a function of the Digital Volume Control register setting and the output of the DRC.

The DRC parameters are described in sections that follow.

2.5.4.3.1 DRC Threshold

The DRC Threshold represents the level of the DAC playback signal at which the gain compression becomes active. The output of the digital volume control in the DAC is compared with the set threshold. The threshold value is programmable by writing to register B0_P0_R68_D[4:2]. The Threshold value can be adjusted between –3dBFS to -24dBFS in steps of 3dB. Keeping the DRC Threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC Threshold value too low can limit the perceived loudness of the output signal.

The recommended DRC-Threshold value is –24 dB.

When the output signal exceeds the set DRC Threshold, the interrupt flag bits at B0_P0_R44_D[3:2] are updated. These flag bits are 'sticky' in nature, and are reset only after they are read back by the user. The non-sticky versions of the interrupt flags are also available at B0_P0_R46_D[3:2].

2.5.4.3.2 DRC Hysteresis

DRC Hysteresis is programmable by writing to B0_P0_R68_D[1:0]. It can be programmed to values between 0dB and 3dB in steps of 1dB. It is a programmable window around the programmed DRC Threshold that must be exceeded for a disabled DRC to become enabled, or an enabled DRC to become disabled. For example, if the DRC Threshold is set to -12dBFS and DRC Hysteresis is set to 3dB, then if the gain compressions in the DRC is inactive, the output of the DAC Digital Volume Control must exceed –9dBFS before gain compression due to the DRC is activated. Similarly, when the gain compression in the DRC is active, the output of the DAC Digital Volume Control needs to fall below -15dBFS for gain compression in the DRC to be deactivated. The DRC Hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of DAC Digital Volume Control rapidly fluctuates in a narrow region around the programmed DRC Threshold. By programming the DRC Hysteresis as 0dB, the hysteresis action is disabled.

Recommended Value of DRC Hysteresis is 3 dB.

2.5.4.3.3 DRC Hold

The DRC Hold is intended to slow the start of decay for a specified period of time in response to a decrease in energy level. To minimize audible artifacts, it is recommended to set the DRC Hold time to 0 through programming B0_P0_R69_D[6:3] = 0000.

2.5.4.3.4 DRC Attack Rate

When the output of the DAC Digital Volume Control exceeds the programmed DRC Threshold, the gain applied in the DAC Digital Volume Control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called Attack. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the Attack Rate programmable via B0_P0_R70_D[7:4]. Attack Rates can be programmed from 4dB gain change per 1/DAC_FS to 1.2207e-5dB gain change per 1/DAC_FS.

Attack Rates should be programmed such that before the output of the DAC Digital Volume control can clip, the input signal should be sufficiently attenuated. High Attack Rates can cause audible artifacts, and too-slow Attack Rates may not be able to prevent the input signal from clipping.

The recommended DRC Attack Rate value is 1.9531e-4 dB per 1/DAC_FS.

2.5.4.3.5 DRC Decay Rate

When the DRC detects a reduction in output signal swing beyond the programmed DRC Threshold, the DRC enters a Decay state, where the applied gain in Digital Volume Control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the Decay Rate programmed through B0_P0_R70_D[3:0]. The Decay Rates can be programmed from 1.5625e-3dB per 1/DAC_FS to 4.7683e-7dB per 1/DAC_FS. If the Decay Rates are programmed too high, then sudden gain changes can cause audible artifacts. However, if it is programmed too slow, then the output may be perceived as too low for a long time after the peak signal has passed.

The recommended Value of DRC Decay Rate is 2.4414e-5 dB per 1/DAC_FS.

2.5.4.3.6 Example Setup for DRC

- PGA Gain = 12 dB
- Threshold = -24 dB
- Hysteresis = 3 dB
- Hold time = 0 ms
- Attack Rate = 1.9531e-4 dB per 1/DAC_FS
- Decay Rate = 2.4414e-5 dB per 1/DAC_FS

Script

```
#Ensure on Page 0 of current Book
w 30 00 00
#Go to Book 0
w 30 FF 00
#Go to Page 0
w 30 00 00
#DAC => 12 db gain left
w 30 41 18
#DAC => 12 db gain right
w 30 42 18
#DAC => DRC Enabled for both channels, Threshold = -24 db, Hysteresis = 3 dB
w 30 44 7F
#DRC Hold = 0 ms, Rate of Changes of Gain = 0.5 dB/Fs'
w 30 45 00
#Attack Rate = 1.9531e-4 dB/Frame , DRC Decay Rate =2.4414e-5 dB/Frame
w 30 46 B6
#Go to Book 80
w 30 FF 50
#Go to Page 3
w 30 00 03
#DRC HPF
w 30 34 7F AB 00 00 80 55 00 00 7F 56 00 00
#DRC LPF
W 30 40 00 11 00 00 00 11 00 00 7F DE 00 00
```

2.5.5 DAC Special Functions

2.5.5.1 Beep Generation

A special function has also been included in the processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. This is intended for generating key-click sounds for user feedback. A default value for the sine-wave frequency, sine burst length, and signal magnitude is kept in the Tone Generator Registers B0_P0_R71-R79. The sine wave generator is very flexible, and is completely register programmable via 9 registers of 8 bits each to provide many different sounds.

Two registers are used for programming the 16-bit, two's-complement, sine-wave coefficient (B0_P0_R76-R77). Two other registers program the 16-bit, two's-complement, cosine-wave coefficient (B0_P0_R78-R79). This coefficient resolution allows virtually any frequency of sine wave in the audio band to be generated up to DAC_FS/2.

Three registers are used to control the length of the sine burst waveform which are located on B0_P0_R73-R75. The resolution (bit) in the registers of the sine burst length is one sample time, so this allows great control on the overall time of the sine burst waveform. This 24-bit length timer supports 16,777,215 sample times. (For example if DAC_FS is set at 48kHz, and the registers combined value equals 96000d (01770h), then the sine burst would last exactly two seconds.)

Two registers are used to independently control the Left sine-wave volume and the Right sine-wave volume. The 6-bit digital volume control allows level control of 0dB to –63dB in one dB steps. The left-channel volume is controlled by writing to B0_P0_R71_D[5:0]. The right-channel volume is controlled by B0_P0_R72_D[5:0]. A master volume control for the left and right channel of the beep generator can be set up using B0_P0_R72_D[7:6]. The default volume control setting is 0dB, the tone generator maximum-output level.

For playing back the sine wave, the DAC must be configured with regards to clock setup and routing. The sine wave gets started by setting the Beep Generator Enable Bit (B0_P0_R71_D7=1). After the sine wave has played for its predefined time period this bit will automatically set back to 0. While the sine wave is playing, the parameters of the beep generator cannot be changed. To stop the sine wave while it is playing set the Beep Generator Enable Bit to 0.

2.5.5.2 Digital Auto Mute

The TLV320AIC3212 also incorporates a special feature, in which the DAC channel is auto-muted when a continuous stream of DC-input is detected. By default, this feature is disabled. It can be enabled by writing a non-000 value into B0_P0_R64_D[6:4]. The non-zero value controls the duration of continuous stream of DC-input before which the auto-mute feature takes effect. This feature is especially helpful for eliminating high-frequency-noise power being delivered into the load even during silent periods of speech or music.

2.5.5.3 Adaptive Filtering

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However the TLV320AIC3212 offers an adaptive filter mode as well, and the DAC contains a single adaptive filter coefficient bank (Adaptive Bank in Book 80) . Setting B80_P0_R1_D2=1 for the Primary Adaptive Bank will turn on double buffering of the coefficients. In this mode, filter coefficients can be updated through the host, and activated without stopping and restarting the DAC. This enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (Buffers A and B). When the DAC is running and adaptive filtering mode is turned on, setting the control bit B80_P0_R1_D0=1 switches the coefficient buffers at the next start of a sampling period. This bit is set back to 0 after the switch occurs. At the same time, the flag B80_P0_R1_D1 toggles.

The flag in B80_P0_R1_D1 indicates which of the two buffers in the Bank is actually in use.

B80_P0_R1_D1=0: Buffer A is in use by the DAC engine, Bit D1=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless to which buffer the coefficients have been written.

DAC running	B80_P0_R1_D1	Coefficient Buffer in use	Writing to	Will update
No	0	None	C1, Buffer A	C1, Buffer A
No	0	None	C1, Buffer B	C1, Buffer B
Yes	0	Buffer A	C1, Buffer A	C1, Buffer B
Yes	0	Buffer A	C1, Buffer B	C1, Buffer B
Yes	1	Buffer B	C1, Buffer A	C1, Buffer A
Yes	1	Buffer B	C1, Buffer B	C1, Buffer A

The user programmable coefficients C1 to C70 are defined on B80_P1-P3 for Buffer A and B80_P9-P11 for Buffer B.

2.5.6 DAC Setup

The following paragraphs are intended to guide a user through the steps necessary to configure the TLV320AIC3212 DAC.

Step 1

The system clock source (master clock) and the targeted DAC sampling frequency must be identified.

Depending on the targeted performance the interpolation filter type (A, B, C, or D) and DOSR value can be determined.

Filter A should be used for 48kHz high-performance operation, DOSR must be a multiple of 8.

Filter B should be used for up to 96kHz operations, DOSR must be a multiple of 4.

Filter C should be used for up to 192kHz operations, DOSR must be a multiple of 2.

Filter D should be used for up to 192kHz operations, DOSR must be a multiple of 2.

In all cases the DOSR is limited in its range by the following condition:

2.8MHz < DOSR * DAC_FS < 6.2MHz

Based on the identified filter type and the required signal processing capabilities, the appropriate processing block can be determined from the list of available processing blocks (PRB_P1 to PRB_P26).

Based on the available master clock, the chosen DOSR and the targeted sampling rate, the clock divider values NDAC and MDAC can be determined. If necessary, the internal PLL can add a large degree of flexibility.

In summary, DAC_CLKIN (derived directly from the system clock source or from the internal PLL) divided by MDAC, NDAC and DOSR must be equal to the DAC sampling rate DAC_FS. The source of the DAC_CLKIN clock signal can be shared with the ADC clock generation block, or can be derived from a separate clock source compared to the ADC_CLKIN signal.

DAC_CLKIN = NDAC*MDAC*DOSR*DAC_FS

To a large degree, NDAC and MDAC can be chosen independently in the range of 1 to 128. In general, NDAC should be as large as possible as long as the following condition can still be met:

MDAC*DOSR/32 ≥ RC

RC is a function of the chosen processing block and is listed in Table 2-26.

The common-mode voltage setting of the device is determined by the available analog power supply and the desired PowerTune mode. This common-mode (input common-mode) value is common across the ADC, DAC and analog bypass path. The output common-mode setting is determined by the available analog power supplies (AVdd and LDOin) and the desired output-signal swing.

At this point the following device specific parameters are known:

PRB_Px, DOSR, NDAC, MDAC, input and output common-mode values

If the PLL is used, the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed in the time between powering the device up and reading data from the device:

Define starting point:	Set register page to Book 0, Page 0 Initiate SW Reset
Program Clock Settings	Program PLL clock pre-divider (PLL_CLKIN_DIV) and PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NDAC Program and power up MDAC Program OSR value Program I^2S word length if required (e.g. 20bit) Program the processing block to be used
At this point, at the latest, analog power supply must be applied to the device	
Program Analog Blocks	Set register Page to Book 0, Page 1 Disable coarse AVdd generation Enable Master Analog Power Control Program Common Mode voltage Program PowerTune (PTM) mode Program Reference fast charging Program Headphone specific depop settings (in case of headphone driver used) Program routing of DAC output to the output amplifier (headphone) Unmute and set gain of output driver Power up output driver
Apply waiting time determined by the de-pop settings and the soft-stepping settings of the driver gain or poll B0_P1_R63-R65	
Power Up DAC	Set register Page to Book 0, Page 0 Power up DAC Channels Unmute digital volume control

Detailed examples can be found in Chapter 4.

2.6 PowerTune

The TLV320AIC3212 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

2.6.1 PowerTune Modes

2.6.1.1 ADC – Programming PTM_R1 to PTM_R4

The device powers up with PTM_R4 (highest performance) set as default. This mode always works across all combinations of common-mode voltage, chosen processing block, or chosen oversampling ratio. If the application can make use of a lower-power configuration please see the ADC and DAC power consumption chapters below for valid combination of PowerTune modes and other device parameters.

The ADC configuration of the PowerTune mode affects right and left channels simultaneously.

	PTM_R1	PTM_R2	PTM_R3	PTM_R4
B0_P1_R61_D[7:6]	0x3	0x2	0x1	0x0

2.6.1.2 DAC - Programming PTM_P1 to PTM_P4

On the playback side, the performance is determined by a combination of register settings and the audio data word length applied. For the highest performance setting (PTM_P4), an audio-data word length of 20 bits is required, while for the modes PTM_P1 to PTM_P3 a word length of 16 bits is sufficient.

	PTM_P1	PTM_P2	PTM_P3	PTM_P4
B0_P1_R3_D[4:2]	0x2	0x1	0x0	0x0
B0_P1_R4_D[4:2]	0x2	0x1	0x0	0x0
Audio Data word length feeding DAC	16 bits	16 bits	16 bits	20 or more bits
B0_P4_R1_D[4:3] or B0_P4_R17_D[4:3] or B0_P4_R33_D[4:3]	0x0	0x0	0x0	0x1, 0x2, 0x3

2.6.1.3 Processing Blocks

The choice of processing blocks, PRB_P1 to PRB_P26 for playback and PRB_R1 to PRB_R18 for recording, also influences the power consumption. In fact, the numerous processing blocks have been implemented to offer a choice between power-optimization and configurations with more signal-processing resources.

2.6.2 ADC Power Consumption

The tables in this section give recommendations for various PowerTune modes. Typical performance and power-consumption values are listed. PowerTune modes that are not supported are marked with an ‘X’.

All measurements were taken with the PLL turned off and the ADC configured for single-ended input.

2.6.2.1 ADC, Stereo, 48kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 128, Processing Block = PRB_R1 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	375	375	375	X	500	500	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	–12	0	0	X	–12	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	78.2	91.2	91.0	X	79.5	93.1	93.0	dB
Power consumption	X	12.3	14.6	18.8	X	12.3	14.6	18.8	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R2	A	+1.2
PRB_R3	A	+0.8

2.6.2.2 ADC, Stereo, 48kHz, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	375	X	X	X	500	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	X	0	X	X	X	0	X	dB full scale
Effective SNR w.r.t. max. allowed input level	86.4	X	88.7	X	X	X	90.7	X	dB
Power consumption	8.3	X	11.3	X	X	X	11.4	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+0.7
PRB_R9	B	+0.5
PRB_R1	A	+2.5
PRB_R2	A	+3.7
PRB_R3	A	+3.3

2.6.2.3 ADC, Stereo, 48kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B), DVdd = 1.26V

	PTM_R1 CM = 0.75V AVdd=1.5V	PTM_R3 CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	0	dB full scale
Effective SNR w.r.t. max. allowed input level	85.9	90.8	dB
Power consumption	5.6	9.5	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+0.4
PRB_R9	B	+0.2
PRB_R1	A	+1.2
PRB_R2	A	+1.8
PRB_R3	A	+1.6

2.6.2.4 ADC, Mono, 48kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	375	375	375	X	500	500	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	–12	0	0	X	–12	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	77.8	91.0	90.8	X	79.0	93.3	93.2	dB
Power consumption	X	7.0	8.1	10.2	X	7.0	8.1	10.2	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R5	A	+0.6
PRB_R6	A	+0.4

2.6.2.5 ADC, Mono, 48kHz, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	375	X	X	X	500	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	X	0	X	X	X	0	X	dB full scale
Effective SNR w.r.t. max. allowed input level	86.7	X	88.7	X	X	X	90.9	X	dB
Power consumption	5.1	X	6.6	X	X	X	6.7	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	–0.4
PRB_R12	B	–0.1
PRB_R4	A	+1.0
PRB_R5	A	+1.6
PRB_R6	A	+1.4

2.6.2.6 ADC, Mono, 48 kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B), DVdd = 1.26V

	PTM_R1 CM = 0.75V AVdd=1.5V	PTM_R3 CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	–2	0	dB full scale
Effective SNR w.r.t. max. allowed input level	86.7	90.9	dB
Power consumption	3.3	5.3	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	–0.2
PRB_R12	B	–0.1
PRB_R4	A	+0.5
PRB_R5	A	+0.8
PRB_R6	A	+0.7

2.6.2.7 ADC, Stereo, 8kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 128, Processing Block = PRB_R1 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	90.6	X	X	X	92.9	X	X	X	dB
Power consumption	6.0	X	X	X	6.1	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R2	A	+0.2
PRB_R3	A	+0.1

2.6.2.8 ADC, Stereo, 8kHz, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	87.1	X	X	X	88.6	X	X	X	dB
Power consumption	5.5	X	X	X	5.5	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+0.1
PRB_R9	B	+0.1
PRB_R1	A	+0.4
PRB_R2	A	+0.6
PRB_R3	A	+0.6

2.6.2.9 ADC, Stereo, 8kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R7 (Decimation Filter B), PowerTune Mode = PTM_R1, DVdd = 1.26

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	87.2	88.8	dB
Power consumption	4.2	5.0	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R8	B	+0.1
PRB_R9	B	0
PRB_R1	A	+0.2
PRB_R2	A	+0.3
PRB_R3	A	+0.3

2.6.2.10 ADC, Mono, 8kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	91.0	X	X	X	93.1	X	X	X	dB
Power consumption	3.5	X	X	X	3.5	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R5	A	+0.1
PRB_R6	A	+0.1

2.6.2.11 ADC, Mono, 8kHz, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	375	X	X	X	500	X	X	X	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	X	X	X	0	X	X	X	dB full scale
Effective SNR w.r.t. max. allowed input level	87.8	X	X	X	88.7	X	X	X	dB
Power consumption	3.2	X	X	X	3.3	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	–0.1
PRB_R12	B	0
PRB_R4	A	+0.2
PRB_R5	A	+0.3
PRB_R6	A	+0.2

2.6.2.12 ADC, Mono, 8kHz, Lowest Power Consumption

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B), PowerTune Mode = PTM_R1, DVdd = 1.26V

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	87.7	89.3	dB
Power consumption	2.3	2.8	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R10	B	0
PRB_R12	B	0
PRB_R4	A	+0.1
PRB_R5	A	+0.1
PRB_R6	A	+0.1

2.6.2.13 ADC, Stereo, 192kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

AOSR = 32, Processing Block = PRB_R14 (Decimation Filter C)

	Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
	PTM_R1	PTM_R2	PTM_R3	PTM_R4	PTM_R1	PTM_R2	PTM_R3	PTM_R4	UNIT
0dB full scale	X	X	X	375	X	X	X	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	X	X	X	0	X	X	X	0	dB full scale
Effective SNR w.r.t. max. allowed input level	X	X	X	91.2	X	X	X	93.6	dB
Power consumption	X	X	X	27.0	X	X	X	27.0	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R13	C	–4.5
PRB_R15	C	–1.6

2.6.2.14 ADC, Stereo, 192kHz, Lowest Power Consumption

AOSR = 32, Processing Block = PRB_R14 (Decimation Filter C), PowerTune Mode = PTM_R4, DVdd = 1.26V

	CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale	375	500	mV_{RMS}
Max. allowed input level w.r.t. 0dB full scale	0	0	dB full scale
Effective SNR w.r.t. max. allowed input level	91.1	93.6	dB
Power consumption	17.3	19.4	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_R13	C	–2.2
PRB_R15	C	–0.9

2.6.3 DAC Power Consumption

The tables in this section give recommendations for various DAC PowerTune modes. Typical performance and power-consumption numbers for line-out signals are listed. For more details on performance and power-consumption numbers for headphone, see Section Section 2.3.3.5. PowerTune modes which are not supported are marked with an 'X'.

All measurements were taken with the PLL turned off, no signal is present, and the DAC modulator is fully running.

2.6.3.1 DAC, Stereo, 48kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

DOSR = 128, Processing Block = PRB_P8 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	225	375	375	100	300	500	500	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.5	96.3	99.3	99.2	91.7	98.4	101.2	101.2	dB
	Power consumption	11.3	11.9	12.4	12.4	11.5	12.2	12.9	12.9	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	–0.1
PRB_P2	A	+2.6
PRB_P3	A	+1.1
PRB_P7	B	–2.8
PRB_P9	B	–1.7
PRB_P10	B	+0.6
PRB_P11	B	–1.2
PRB_P23	A	–0.1
PRB_P24	A	+2.8
PRB_P25	A	+3.6

2.6.3.2 DAC, Stereo, 48kHz, Lowest Power Consumption

DOSR = 64, Interpolation Filter D, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V PRB_P26 PTM_P1	CM = 0.9V AVdd=1.8V PRB_P26 PTM_P1	CM = 0.75V AVdd=1.5V PRB_P7 PTM_P4	UNIT
0dB full scale[1]		75	100	375	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	88.6	90.7	99.2	dB
	Power consumption	2.7	3.3	5.2	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW) [1]
PRB_P1	A	+3.1
PRB_P2	A	+4.4
PRB_P3	A	+3.6
PRB_P7	B	+1.7
PRB_P9	B	+2.3
PRB_P10	B	+3.4
PRB_P11	B	+2.5
PRB_P23	A	+3.1
PRB_P24	A	+4.5
PRB_P25	A	+4.8

(1) Estimated power change is w.r.t. PRB_P26.

2.6.3.3 DAC, Mono, 48kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

DOSR = 128, Processing Block = PRB_P13 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	225	375	375	100	300	500	500	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.6	96.5	99.4	99.3	91.2	98.5	101.4	101.4	dB
	Power consumption	6.1	6.3	6.6	6.6	6.2	6.5	6.9	6.9	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change(mW)
PRB_P4	A	+0.1
PRB_P5	A	+1.8
PRB_P6	A	+1.0
PRB_P12	B	–1.3
PRB_P14	B	–0.7
PRB_P15	B	+0.6
PRB_P16	B	–0.3

2.6.3.4 DAC, Mono, 48kHz, Lowest Power Consumption

DOSR = 64, Processing Block = PRB_P13 (Interpolation Filter B), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.8	91.9	dB
	Power consumption	3.1	3.5	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P4	A	0
PRB_P5	A	+0.8
PRB_P6	A	+0.4
PRB_P12	B	–0.6
PRB_P14	B	–0.3
PRB_P15	B	+0.3
PRB_P16	B	–0.1

2.6.3.5 DAC, Stereo, 8kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

DOSR = 768, Processing Block = PRB_P7 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale		75	X	X	X	100	X	X	X	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.6	X	X	X	91.7	X	X	X	dB
	Power consumption	4.7	X	X	X	4.8	X	X	X	mW

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.5
PRB_P2	A	+1.0
PRB_P3	A	+0.7
PRB_P8	B	+0.5
PRB_P9	B	+0.3
PRB_P10	B	+0.6
PRB_P11	B	+0.4
PRB_P23	A	+0.5
PRB_P24	A	+1.0
PRB_P25	A	+1.0

2.6.3.6 DAC, Stereo, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P26 (Interpolation Filter D), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	88.6	90.6	dB
	Power consumption	2.2	2.8	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.5
PRB_P2	A	+0.7
PRB_P3	A	+0.6
PRB_P7	B	+0.3
PRB_P8	B	+0.5
PRB_P9	B	+0.3
PRB_P10	B	+0.5
PRB_P11	B	+0.4
PRB_P23	A	+0.5
PRB_P24	A	+0.7
PRB_P25	A	+0.8

2.6.3.7 DAC, Mono, 8kHz, Highest Performance, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

DOSR = 768, Processing Block = PRB_P4 (Interpolation Filter A)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	X	X	X	100	X	X	X	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.6	X	X	X	91.8	X	X	X	dB
	Power consumption	3.3	X	X	X	3.4	X	X	X	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.2
PRB_P6	A	0
PRB_P12	B	–0.2
PRB_P13	B	–0.1
PRB_P14	B	–0.2
PRB_P15	B	0
PRB_P16	B	–0.1

2.6.3.8 DAC, Mono, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P4 (Interpolation Filter A), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	89.3	91.9	dB
	Power consumption	1.7	2.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.1
PRB_P6	A	+0.1
PRB_P12	B	–0.1
PRB_P13	B	0
PRB_P14	B	–0.1
PRB_P15	B	0
PRB_P16	B	0

2.6.3.9 DAC, Stereo, 192kHz, DVDD = IOVDD = 1.8V, AVDDx_18 = 1.8V

DOSR = 32, Processing Block = PRB_P17 (Interpolation Filter C)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		X	X	X	375	X	X	X	500	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	X	X	X	99.2	X	X	X	101.2	dB
	Power consumption	X	X	X	12.0	X	X	X	12.2	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+11.0
PRB_P19	C	+4.8

2.6.3.10 DAC, Stereo, 192kHz, Lowest Power Consumption

DOSR = 16, Processing Block = PRB_R17 (Interpolation Filter C), PowerTune Mode = PTM_P4, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		375	500	mV_{RMS}
Line out	Effective SNR w.r.t. 0dB full scale	99.2	101.1	dB
	Power consumption	6.1	6.8	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see Section 2.5.4.1.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+5.4
PRB_P19	C	+2.3

2.7 Clock Generation and PLL

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3212.

The TLV320AIC3212 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require source reference clocks, and these clocks can be from a single source or from two separate sources. They can be provided on a variety of device pins such as MCLKx, BCLK1, BCLK2, GPI1, GPI2, or GPIOx pins. The clocks, ADC_CLKIN and DAC_CLKIN, can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the selectable processing block sections. In the event that the desired audio or selectable processing block clocks cannot be generated from the reference clocks on MCLKx, BCLK1, BCLK2, or GPIOx, the codec also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. The ADC_CLKIN and DAC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the selectable processing block sections.

The TLV320AIC3212 supports a wide range of options for generating clocks for the ADC and DAC sections as well as the interface and other control blocks as shown in Figure 2-44. The clocks for the ADC and the DAC require a source reference clock. In the TLV320AIC3212 the ADC and DAC clock-trees can have different root clocks. These clocks can be provided on a variety of device pins such as MCLK1, MCLK2, BCLK1, GPIO1, BCLK2, GPI1, GPIO2, and GPI2, and the onchip high-frequency reference clock (HF_REF_CLK) and high-frequency oscillator clock (HF_OSC_CLK) can also be provided as sources. The source reference clock for the ADC can be chosen by programming the ADC_CLKIN value on B0_P0_R4_D[3:0]. The source reference clock for the DAC can be chosed by programming the DAC_CLKIN value on B0_P0_R4_D[7:4]. The ADC_CLKIN and DAC_CLKIN can then be routed through highly flexible clock dividers shown in Figure 2-44 to generate the various clocks required for the ADC, DAC, and selectable processing block sections. In the event that the desired audio selectable processing block clocks cannot be generated from the reference clocks coming from the device pins listed above, the TLV320AIC3212 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from ADC_CLKIN and DAC_CLKIN, the TLV320AIC3212 provides several programmable clock dividers to help achieve a variety of sampling rates for the ADC and DAC, as well as clocks for the selectable processing block sections.

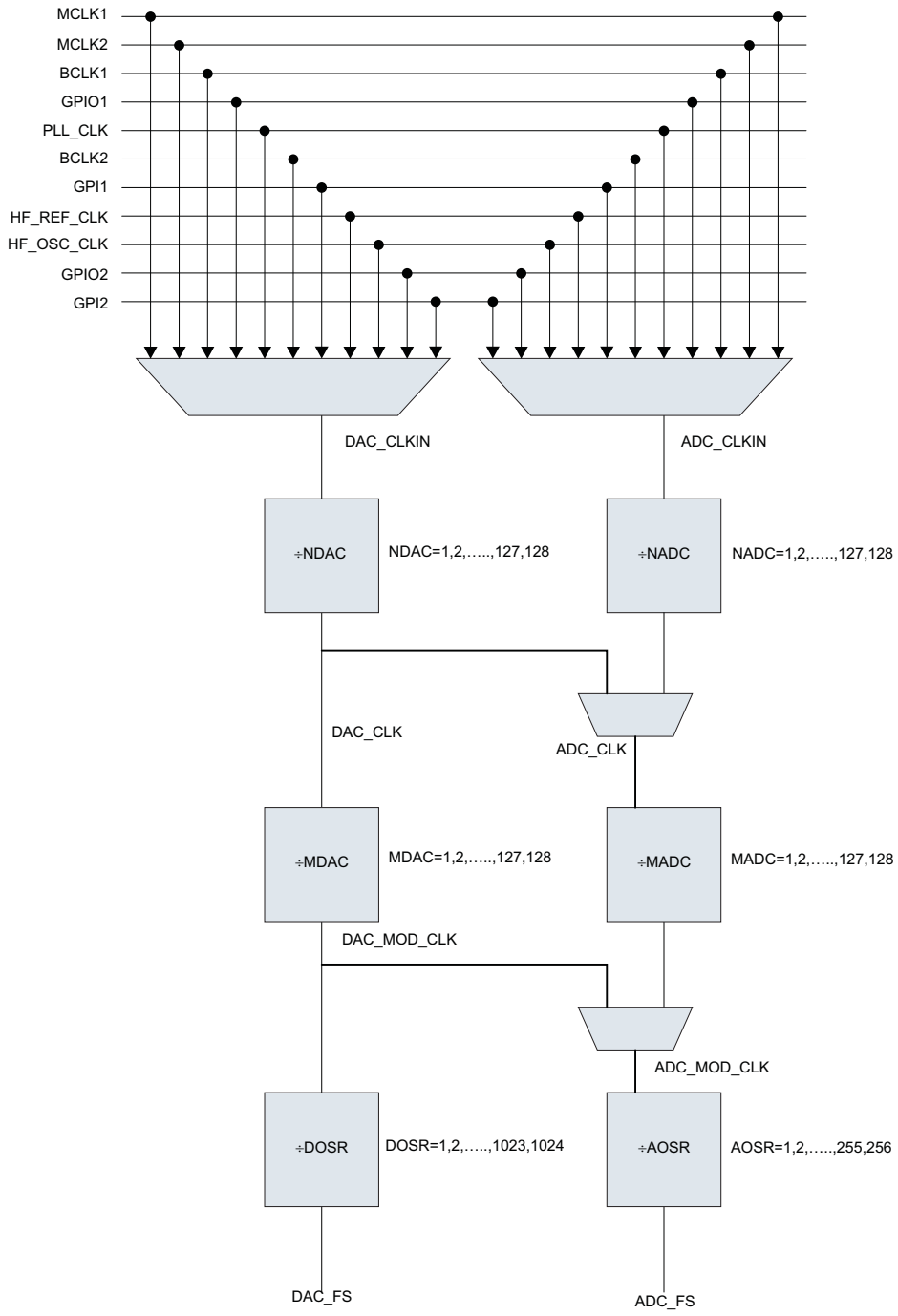


Figure 2-44. Clock Distribution Tree

The DAC and ADC clocks are obtained as follows:

$$DAC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MDAC \times DOSR} \quad (14)$$

$$DAC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MDAC} \quad (15)$$

$$ADC\_f_S = \frac{ADC\_CLKIN}{NADC \times MADC \times AOSR} \quad (16)$$

$$ADC\_MOD\_CLK = \frac{ADC\_CLKIN}{NADC \times MADC} \quad (17)$$

The MUX settings in the ADC clock tree allow alternative clock settings:

$$ADC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MADC \times AOSR}$$

or

$$ADC\_f_s = \frac{DAC\_CLKIN}{NDAC \times MDAC \times AOSR} \quad (18)$$

$$ADC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MADC}$$

or

$$ADC\_MOD\_CLK = \frac{DAC\_CLKIN}{NDAC \times MDAC} \quad (19)$$

By default ADC_CLK = DAC_CLK and ADC_MOD_CLK = DAC_MOD_CLK.

Table 2-35. DAC CLKIN and ADC CLKIN Clock Dividers

Divider	Bits	Range
NDAC	B0_P0_R11_D[6:0]	1, 2, … 127, 128
MDAC	B0_P0_R12_D[6:0]	1, 2, … 127, 128
DOSR	B0_P0_R13_D[1:0] and B0_P0_R14_D[7:0]	1, 2, … 1023, 1024
NADC	B0_P0_R18_D[6:0]	1, 2, … 127, 128
MADC	B0_P0_R19_D[6:0]	1, 2, … 127, 128
AOSR	B0_P0_R20_D[7:0]	1, 2, … 255, 256

The registers used for DAC and ADC clock selection are listed in Table 2-36.

Table 2-36. DAC and ADC Clock Selectors

Selector	Bits	Inputs
DAC_CLKIN	B0_P0_R4_D[7:4]	MCLK1, MCLK2, BCLK1, GPIO1, PLL_CLK, BCLK2, GPI1, HR_REF_CLK, HF_OSC_CLK, GPIO2, GPI2
ADC_CLKIN	B0_P0_R4_D[3:0]	MCLK1, MCLK2, BCLK1, GPIO1, PLL_CLK, BCLK2, GPI1, HR_REF_CLK, HF_OSC_CLK, GPIO2, GPI2
ADC_CLK	B0_P0_R18_D7	NDAC output (DAC_CLK), NADC output
ADC_MOD_CLK	B0_P0_R19_D7	MDAC output (DAC_MOD_CLK), MADC output

The DAC Modulator is clocked by DAC_MOD_CLK. For proper power-up of the DAC Channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (B0_P0_R11_D7=1 and B0_P0_R12_D7=1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in B0_P0_R37_D7 for the Left DAC and B0_P0_R37_D3 for the Right DAC. When both flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider.

The ADC modulator is clocked by ADC_MOD_CLK. For proper power-up of the ADC Channel, these clocks are enabled by the NADC and MADC clock dividers (B0_P0_R18_D7=1 and B0_P0_R19_D7=1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NADC and MADC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in B0_P0_R36_D6 for the Left ADC and B0_P0_R36_D2 for the Right ADC. When both flags indicate power-down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK is derived from the NDAC divider output, the NDAC must be kept powered up till the power-down status flags for ADC do not indicate that the ADC is still in the process of powering down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_FS is needed (i.e. when WCLK is generated by TLV320AIC3212 or AGC is enabled) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, all the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.

The TLV320AIC3212 also has options for routing some of the internal clocks to the output pins of the device to be used as general purpose clocks in the system.

For example, the TLV320AIC3212 can be configured to drive the bit clock signals ASI1_BCLK_OUT, ASI2_BCLK_OUT, and ASI3_BCLK_OUT on the three serial interfaces as shown in Figure 2-45.

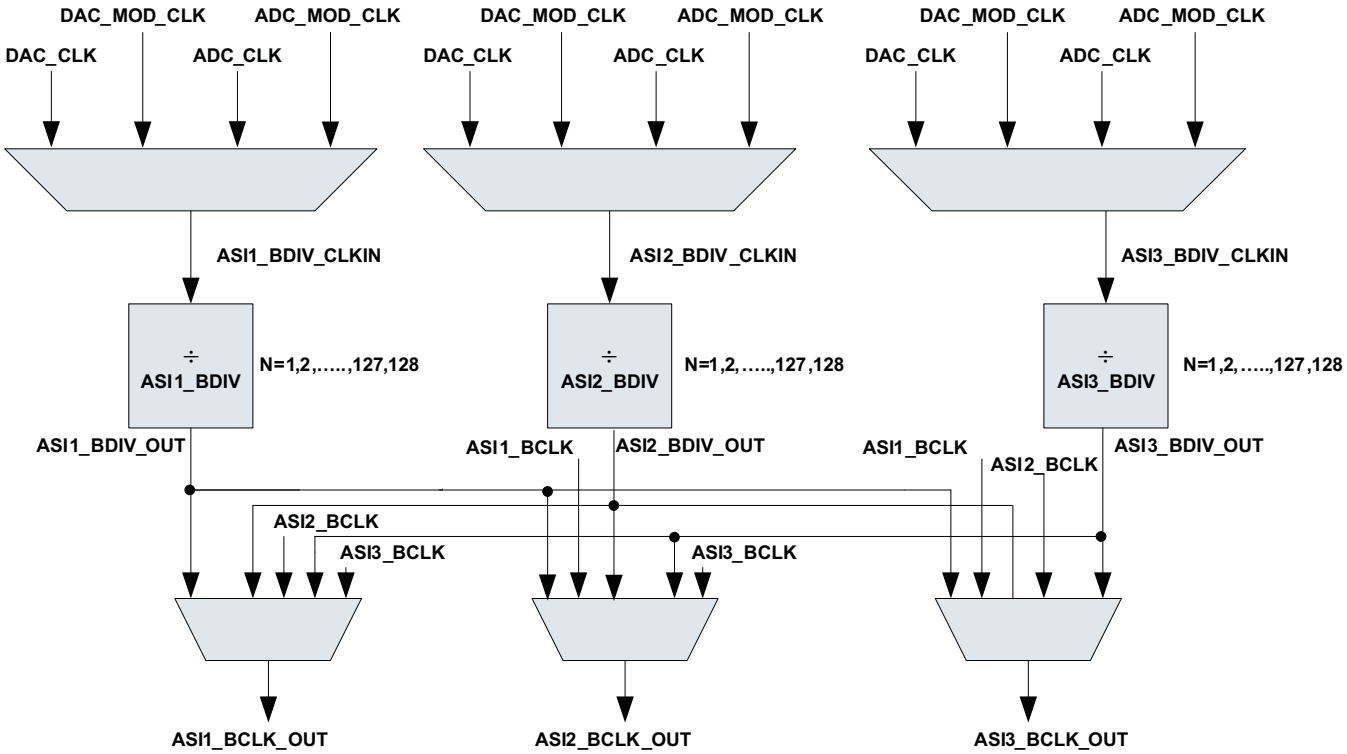


Figure 2-45. Bit Clock Output Options for ASI1, ASI2, and ASI3

When TLV320AIC3212 is configured to drive ASI1_BCLK_OUT, the clock signal can be selected via B0_P4_R14_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI2_BCLK Input, or ASI3_BCLK Input.

When TLV320AIC3212 is configured to drive ASI2_BCLK_OUT, the clock signal can be selected via B0_P4_R30_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK Input, or ASI3_BCLK Input.

When TLV320AIC3212 is configured to drive ASI3_BCLK_OUT, the clock signal can be selected via B0_P4_R46_D[6:4] to come from ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, or ASI2_BCLK.

ASI1_BDIV_OUT is a divided value of ASI1_BDIV_CLKIN, where the division value can be programmed in B0_P4_R12_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R12_D7. The ASI1_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI1_BDIV_CLKIN mux in B0_P4_R11_D[1:0].

ASI2_BDIV_OUT is a divided value of ASI2_BDIV_CLKIN, where the division value can be programmed in B0_P4_R28_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R28_D7. The ASI2_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI2_BDIV_CLKIN mux in B0_P4_R27_D[1:0].

ASI3_BDIV_OUT is a divided value of ASI3_BDIV_CLKIN, where the division value can be programmed in B0_P4_R44_D[6:0] from 1 to 128, and this bit clock divider can be powered on by setting B0_P4_R44_D7. The ASI3_BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or ADC_MOD_CLK by configuring the ASI3_BDIV_CLKIN mux in B0_P4_R43_D[1:0].

The TLV320AIC3212 can also be configured to provide the world clocks for ASI1, ASI2, and ASI3 as shown in Figure 2-46.

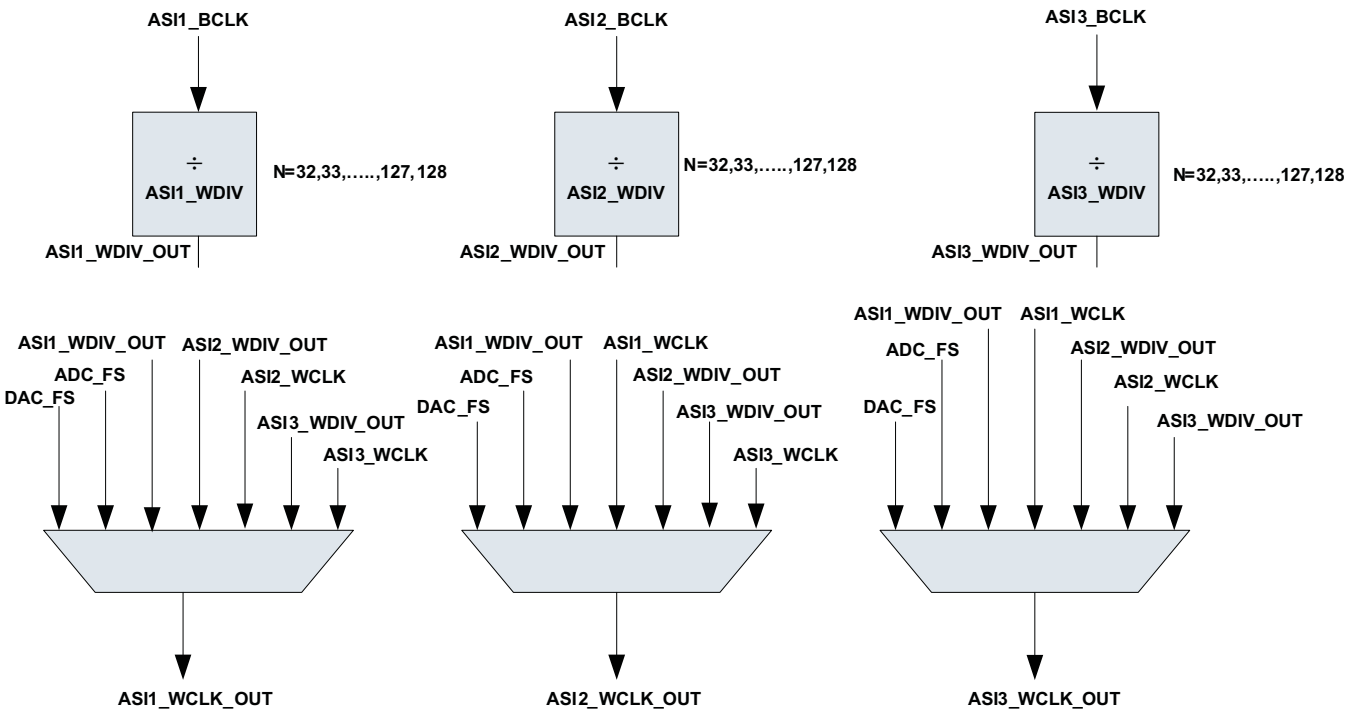


Figure 2-46. Word Clock Options for ASI1, ASI2, and ASI3

ASI1_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI2_WCLK Input, and ASI3_WCLK Input using B0_P4_R14_D[2:0]. ASI1_WDIV_OUT is driven as a divided value of ASI1_BCLK, where the division can be programmed in B0_P4_R13_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R13_D7.

ASI2_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI1_WCLK Input, and ASI3_WCLK Input using B0_P4_R30_D[2:0]. ASI2_WDIV_OUT is driven as a divided value of ASI2_BCLK, where the division can be programmed in B0_P4_R29_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R29_D7.

ASI3_WCLK_OUT can be selected to come from DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, as well as ASI1_WCLK Input, and ASI2_WCLK Input using B0_P4_R46_D[2:0]. ASI3_WDIV_OUT is driven as a divided value of ASI3_BCLK, where the division can be programmed in B0_P4_R45_D[6:0] from 32 to 128, and this word clock divider can be powered on by setting B0_P4_R45_D7.

The bit clock and work clock dividers are summarized in Table 2-37. The bit clock and word clock selectors are summarized in Table 2-38.

Table 2-37. ASI1, ASI2, and ASI3 Bit and Word Clock Dividers

Divider	Bits	Range
ASI1_BDIV	B0_P4_R12_D[6:0]	1, 2, … 127, 128
ASI2_BDIV	B0_P4_R28_D[6:0]	1, 2, … 127, 128
ASI3_BDIV	B0_P4_R44_D[6:0]	1, 2, … 127, 128
ASI1_WDIV	B0_P4_R13_D[6:0]	32, 33, … 127, 128
ASI2_WDIV	B0_P4_R29_D[6:0]	32, 33, … 127, 128
ASI3_WDIV	B0_P4_R45_D[6:0]	32, 33, … 127, 128

Table 2-38. ASI1, ASI2, and ASI3 Bit and Word Clock Selection

Selector	Bits	Inputs
ASI1_BCLK_OUT	B0_P4_R14_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI2_BCLK, ASI3_BCLK
ASI2_BCLK_OUT	B0_P4_R30_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, ASI3_BCLK
ASI3_BCLK_OUT	B0_P4_R46_D[6:4]	ASI1_BDIV_OUT, ASI2_BDIV_OUT, ASI3_BDIV_OUT, ASI1_BCLK, ASI2_BCLK
ASI1_BDIV_CLKIN	B0_P4_R11_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI2_BDIV_CLKIN	B0_P4_R27_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI3_BDIV_CLKIN	B0_P4_R43_D[1:0]	DAC_CLK, DAC_MOD_CLK, ADC_CLK, ADC_MOD_CLK
ASI1_WCLK_OUT	B0_P4_R14_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI2_WCLK, ASI3_WCLK
ASI2_WCLK_OUT	B0_P4_R30_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI1_WCLK, ASI3_WCLK
ASI3_WCLK_OUT	B0_P4_R46_D[2:0]	DAC_FS, ADC_FS, ASI1_WDIV_OUT, ASI2_WDIV_OUT, ASI3_WDIV_OUT, ASI1_WCLK, ASI2_WCLK

Additionally a general purpose clock CLKOUT can be driven out on DOUT1, WCLK2, BCLK2, GPIO1, GPIO2, or GPO1 according to the settings in Table 2-39.

Table 2-39. CLKOUT Selection

Clock Output	Bits
DOUT1	B0_P4_R67_D[4:1] = ’0011’
WCLK2	B0_P4_R69_D[5:2] = ’0100’
BCLK2	B0_P4_R70_D[5:2] = ’0100’
GPIO1	B0_P4_R86_D[6:2] = ’00100’
GPIO2	B0_P4_R87_D[6:2] = ’00100’
GPO1	B0_P4_R96_D[4:1] = ”0011’

This clock can be a divided down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to B0_P0_R22_D[6:0], and this CDIV clock divider can be powered on by setting B0_P4_R22_D7. The CDIV_CLKIN can itself be programmed as one of the clocks among the list shown in Figure 2-47. This can be controlled by programming the mux in B0_P0_R21_D[3:0].

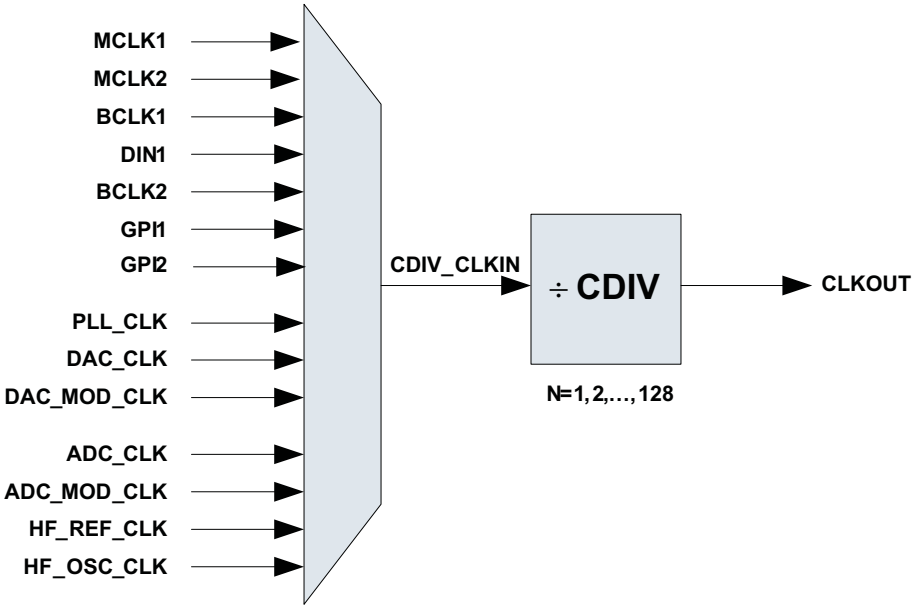


Figure 2-47. General Purpose Clock Output Options

Table 2-40. Maximum TLV320AIC3212 Clock Frequencies

	DVdd ≥ 1.26V	DVdd ≥ 1.65V	DVdd ≥ 1.71V
ADC_CLKIN	40MHz	137MHz	137MHz
DAC_CLKIN	40MHz	137MHz	137MHz
ADC_CLK	37.5MHz	70MHz	70MHz
ADC_MOD_CLK	6.758MHz	6.758MHz	6.758MHz
ADC_FS	0.192MHz	0.192MHz	0.192MHz
DAC_CLK	33.0MHz	70MHz	70MHz
DAC_MOD_CLK	6.758MHz	6.758MHz	6.758MHz
DAC_FS	0.192MHz	0.192MHz	0.192MHz
ASI1_BDIV_CLKIN , ASI2_BDIV_CLKIN , ASI3_BDIV_CLKIN	40MHz	70MHz	70MHz
CDIV_CLKIN	40MHz	120MHz	129MHz

2.7.1 PLL

The TLV320AIC3212 has an on-chip PLL to generate the clock frequency for the audio ADC, DAC, and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL Clocking and muxing is shown in Figure 2-48.

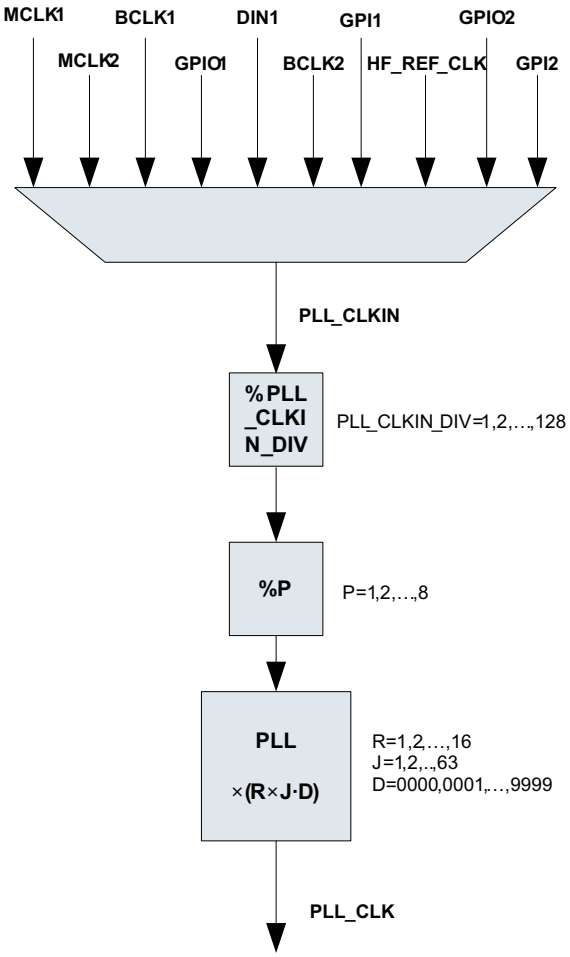


Figure 2-48. PLL Clocking and Mux

The PLL input supports clocks varying from 512kHz to 20MHz and is register programmable to enable generation of required sampling rates with fine resolution. The PLL can be turned on by writing to B0_P0_R6_D7. When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation PLL_CLK = (PLL_CLKIN x R x J.D)/(PxPLL_CLKIN_DIV)

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{PxPLL\_CLKIN\_DIV} \quad (20)$$

R = 1, 2, … 16.

J = 1, 2, 3, 4,… 63, and D = 0, 1, 2, 3, 4, … 9999

P = 1, 2, 3, 4, … 8

PLL_CLKIN_DIV = 1, 2, … 128.

R, J, D, P, and PLL_CLKIN_DIV are register programmable.

The PLL can be programmed via B0_P0_R6-R10. The PLL can be turned on via B0_P0_R6_D7. The variable P can be programmed via B0_P0_R6_D[6:4]. The default register value for P is 1. The variable R can be programmed via B0_P0_R6_D[3:0]. The default register value for R is 1. The variable J can be programmed via B0_P0_R7_D[5:0]. The default register value for J is 4. The variable D is 12-bits, programmed into two registers. The MSB portion can be programmed via B0_P0_R8_D[5:0], and the LSB portion is programmed via B0_P0_R9_D[7:0]. The default register value for D is 0. The PLL_CLKIN_DIV value can be programmed via B0_P0_R10_D[6:0]. The default register value for PLL_CLKIN_DIV is 1.

When the PLL is enabled the following conditions must be satisfied

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512\,\text{kHz} \le \frac{\text{PLL\_CLKIN}}{\text{P} \times \text{PLL\_CLKIN\_DIV}} \le 20\,\text{MHz} \quad (21)$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10\,\text{MHz} \le \frac{\text{PLL\_CLKIN}}{\text{P} \times \text{PLL\_CLKIN\_DIV}} \le 20\,\text{MHz} \quad (22)$$

In the TLV320AIC3212 the PLL_CLK supports a wide range of output clock values, based on register settings and power-supply conditions.

Table 2-41. PLL_CLK Frequency Range

AVdd	PLL Mode B0_P0_R5_D6	Min PLL_CLK frequency (MHz)	Max PLL_CLK frequency (MHz)
≥1.5V	0	80	103
	1	95	110
≥1.65V	0	80	118
	1	92	123
≥1.80V	0	80	132
	1	92	137

The PLL can be powered up independently from the ADC and DAC blocks, and can also be used as a general purpose PLL by selecting its output as an input to the General Purpose Output Clock mux (enabling routing to a variety of digital output pins). After powering up the PLL, PLL_CLK is available typically after 10ms. The PLL output frequency is controlled by J.D and R dividers

PLL Divider	Bits
J	B0_P0_R7_D[5:0]
D	B0_P0_R8_D[5:0] && B0_P0_R9_D[7:0]
R	B0_P0_R6_D[3:0]

The D-divider value is 14-bits wide and is controlled by 2 registers. For proper update of the D-divider value, B0_P0_R8 must be programmed first followed immediately by B0_P0_R9. Unless the write to B0_P0_R9 is completed, the new value of D will not take effect.

The clocks for codec and various signal processing blocks, ADC_CLKIN and DAC_CLKIN can be generated from MCLK1, MCLK2, BCLK1, GPIO1, BCLK2, GPI1, HF_REF_CLK, HF_OSC_CLK, GPIO2, GPI2, or PLL_CLK (B0_P0_R4_D[7:0]).

If the ADC_CLKIN and/or the DAC_CLKIN are derived from the PLL, then the PLL must be powered up first and powered down last.

Table 2-42 lists several example cases of typical MCLK rates and how to program the PLL to achieve a sample rate Fs of either 44.1kHz or 48kHz.

Table 2-42. PLL Example Configurations

Fs = 44.1kHz											
MCLK (MHz)	PLL_CLKIN_DIV	PLLP	PLLR	PLLJ	PLLD	MADC	NADC	AOSR	MDAC	NDAC	DOSR
2.8224	1	1	3	10	0	3	5	128	3	5	128
5.6448	1	1	3	5	0	3	5	128	3	5	128
12	1	1	1	7	560	3	5	128	3	5	128
13	1	1	2	4	2336	13	3	64	4	6	104
16	1	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	1	4	4100	3	5	128	3	5	128
48	1	4	1	7	560	3	5	128	3	5	128

Table 2-42. PLL Example Configurations (continued)

Fs = 44.1kHz											
MCLK (MHz)	PLL_CLKIN_DIV	PLLP	PLLR	PLLJ	PLLD	MADC	NADC	AOSR	MDAC	NDAC	DOSR
Fs = 48kHz											
2.048	1	1	3	14	0	2	7	128	7	2	128
3.072	1	1	4	7	0	2	7	128	7	2	128
4.096	1	1	3	7	0	2	7	128	7	2	128
6.144	1	1	2	7	0	2	7	128	7	2	128
8.192	1	1	4	3	0	2	8	128	4	4	128
12	1	1	1	7	1680	2	7	128	7	2	128
16	1	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	1	4	4800	2	7	128	7	2	128
48	1	4	1	7	1680	2	7	128	7	2	128

2.7.2 Low Frequency Reference Clock

To extend the frequency locking range of the on-chip PLL to an external clock at low frequencies, a clock frequency multiplier is used to generate its output clock with the frequency K times of its input reference clock frequency for the PLL to lock, where K is a 28-bit value of the control register bits {B0_P0_R25_D[3:0], B0_P1_R26, B0_P0R27, B0_P0_R28}. The reference clock source can be selected with the control register bits, B0_P0_R24_D[7:4]. The clock routing for the low frequency clock is shown in Figure 2-49.

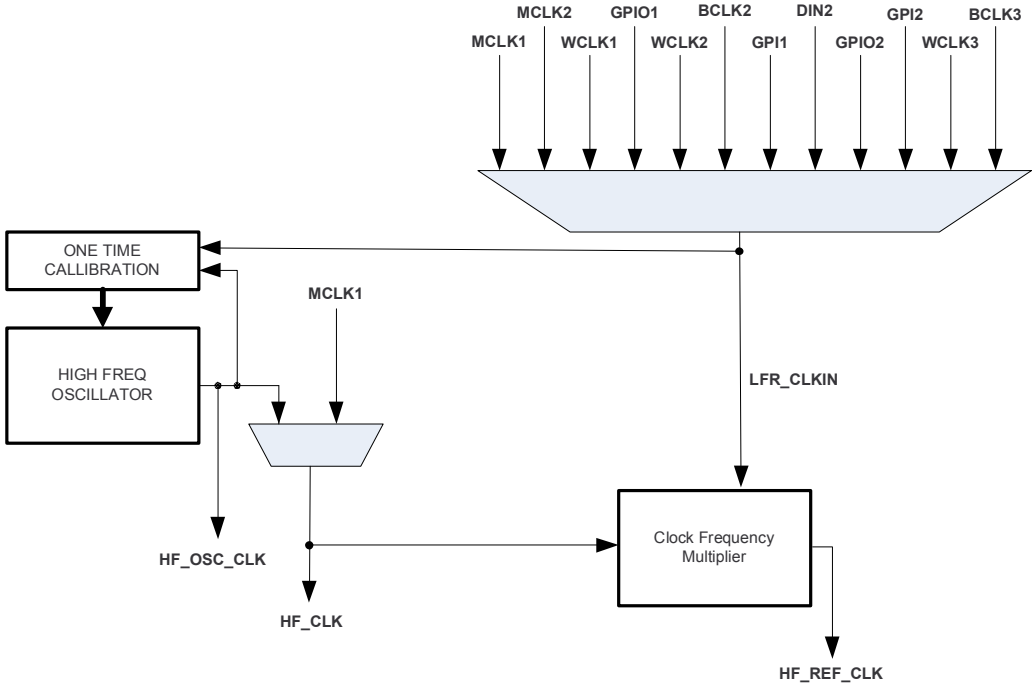


Figure 2-49. Low-Frequency Clocking

The output clock, HF_REF_CLOCK, is generated by delta-sigma modulation with a high frequency clock, HF_CLK. The source of HF_CLK can be setup by programming the control bits, B0_P0_R24_R[3:0]. If the on-chip high frequency oscillator clock, HF_OSC_CLK, is selected as the source, it is recommended to calibrate the oscillator clock by following the proper calibration procedure before turning on the clock multiplier.

The HF_OSC_CLK can have large device-to-device variation of its default frequency. For proper functioning, the HF_OSC_CLK can be calibrated with respect to the LFR_CLKIN. This calibration happens at power-up of the block when this feature is enabled (HF_OSC_CLK is used by any other function). By default this calibration is enabled and if so desired can be disabled by writing B0_P0_R29_D5 = '0'. For calibrating the HF_OSC_CLK the 26-bit ratio of frequencies (Desired HF_OSC_CLK freq / Frequency of LFR_CLKIN) can be programmed in B0_P0_R29_D[1:0], B0_P0_R30_D[7:0], B0_P0_R31_D[7:0], and B0_P0_R32_D[7:0]. This ratio must be programmed before enabling this block. Also, the LFR_CLKIN must be present when the HF_OSC_CLK is enabled, and the LFR_CLKIN frequency should be less than 50 kHz. This calibration is an approximate calibration, and the frequency of HF_OSC_CLK will approximately equal Programmed Ratio * LFR_CLKIN frequency. The error can be approx +/- 7 MHz. The desired frequency should ideally be kept between 50 MHz and 57.5 MHz for good audio performance. Once the calibration is over, the calibrated clock will be available for use by other blocks. The HF_OSC_CLK has an additional programmability by which this block can be used even when AVDD1_18 supply is not powered up. This can be useful when a free running clock is required when AVDD1_18 is not powered as no other analog blocks may be powered up. This feature can be controlled by B0_P0_R29_D6.

For a better quality of the PLL clock, the clock multiplier output should be set at higher frequency by choosing a higher multiplication value of K, if there are multiple options. But the multiplied frequency should not be higher than ¼ times of HF_REF_CLK frequency and the frequency has to be within the PLL locking range, 10-20MHz for D≠0 and 512kHz – 20MHz for D=0. To select HF_REF_CLK as the PLL reference, B0_P0_R5_D[5:2] should be set as '0110'.

2.8 Control Interfaces

The TLV320AIC3212 control interface supports SPI or I^2C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^2C, SPI_SELECT should be tied low. It is not recommended to change the state of SPI_SELECT during device operation.

2.8.1 I^2C Control Mode

The TLV320AIC3212 supports the I^2C control protocol, and will respond by default (GPI3 and GPI4 grounded) to the 7-bit I^2C address of 0011000. With the two I^2C address pins, GPI3 and GPI4, the device can be configured to respond to one of four 7-bit I^2C addresses, 0011000, 0011001, 0011010, or 0011011. The full 8-bit I^2C address can be calculated as:

8-Bit I^2C Address = "00110" + GPI4 + GPI3 + R/W

E.g. to write to the TLV320AIC3212 with GPI4 = 1 and GPI3 = 0 the 8-Bit I^2C Address is "00110" + GPI4 + GPI3 + R/W = "00110100" = 0x34

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the TLV320AIC3212 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver's shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3212 can also respond to and acknowledge a General Call, which consists of the master issuing a command with a slave address byte of 00H. This feature is disabled by default, but can be enabled via B0_P0_R115_D5.

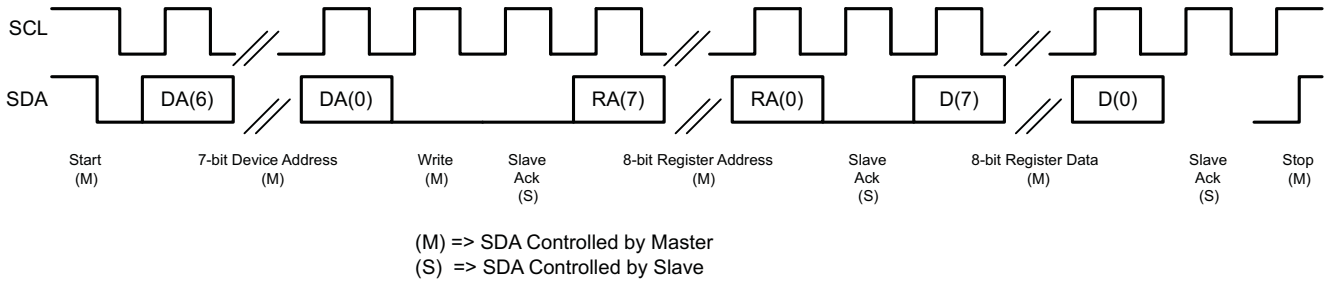


Figure 2-50. I^2C Write

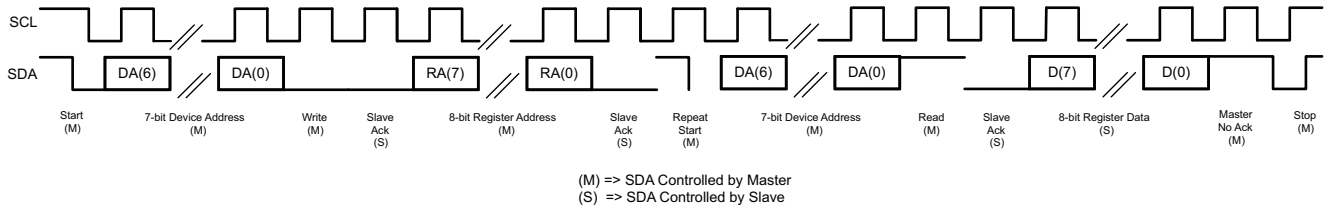


Figure 2-51. I^2C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I^2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

2.8.2 SPI Digital Interface

In the SPI control mode, the TLV320AIC3212 uses the pins SCL as $\overline{SS}$, GPI1 as SCLK, GPO1 as MISO, SDA as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0) and clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3212) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The TLV320AIC3212 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The SSZ pin can remain low between transmissions; however, the TLV320AIC3212 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TLV320AIC3212 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI pin of the part prior to the data for that register. The command is structured as shown in Table 2-43. The first 7 bits specify the address of the register which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI pin and contains the data to be written to the register. Reading of registers is accomplished in a similar fashion. The 8-bit command word sends the 7-bit register address, followed by the R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO pin during the second 8 SCLK clocks in the frame.

Table 2-43.

COMMAND WORD

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

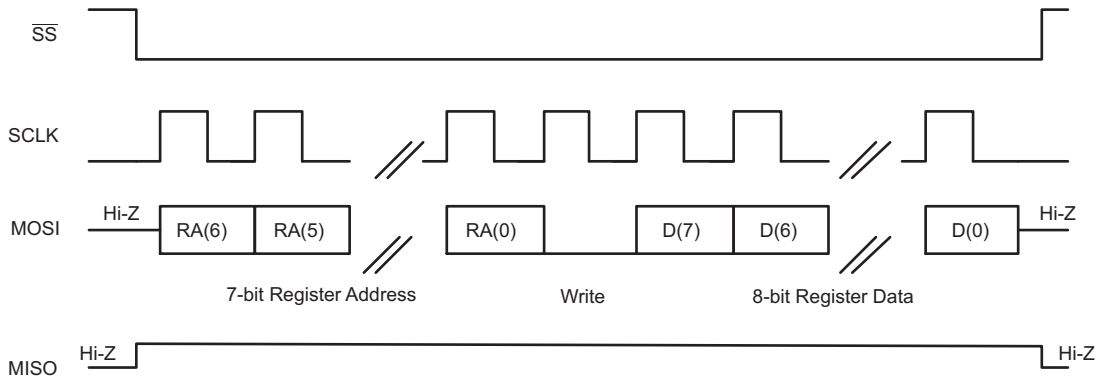


Figure 2-52. SPI Timing Diagram for Register Write

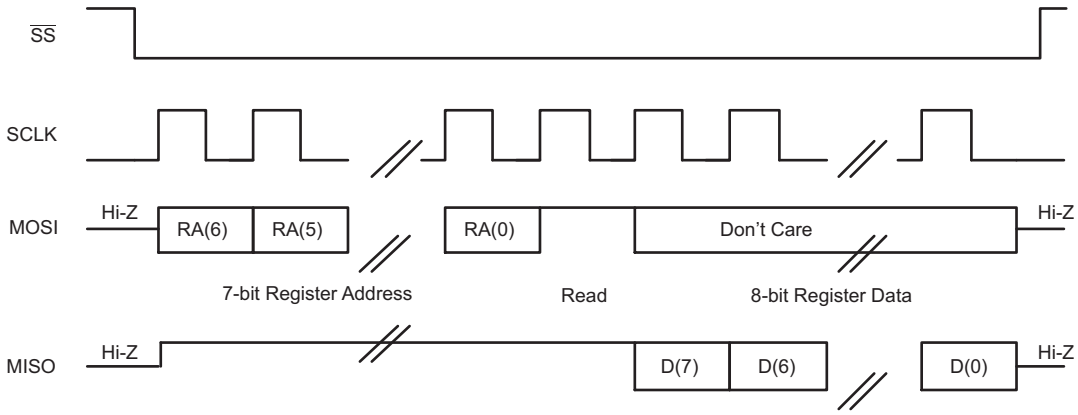


Figure 2-53. SPI Timing Diagram for Register Read

2.9 Audio Digital I/O Interfaces

The TLV320AIC3212 features three digital audio data serial interfaces, or audio buses. Any of these digital audio interfaces can be selected for playback and recording through the stereo DACs and stereo ADCs respectively. This enables this audio codec to handle digital audio from different devices on a mobile platform. A common example of this would be individual connections to an application processor, a communication baseband processor, or a Bluetooth chipset. By utilizing the TLV320AIC3212 as the center of the audio processing in a portable audio system, hardware design of the audio system is greatly simplified. In addition to these three individual digital audio interfaces, a fourth set of digital audio pins can be muxed into Audio Serial Interface #1. In other words, four separate 4-wire digital audio buses can be connected to the TLV320AIC3212. However, it should be noted that only one of the three audio serial interfaces can be routed to/from the DACs/ADCs at a time.

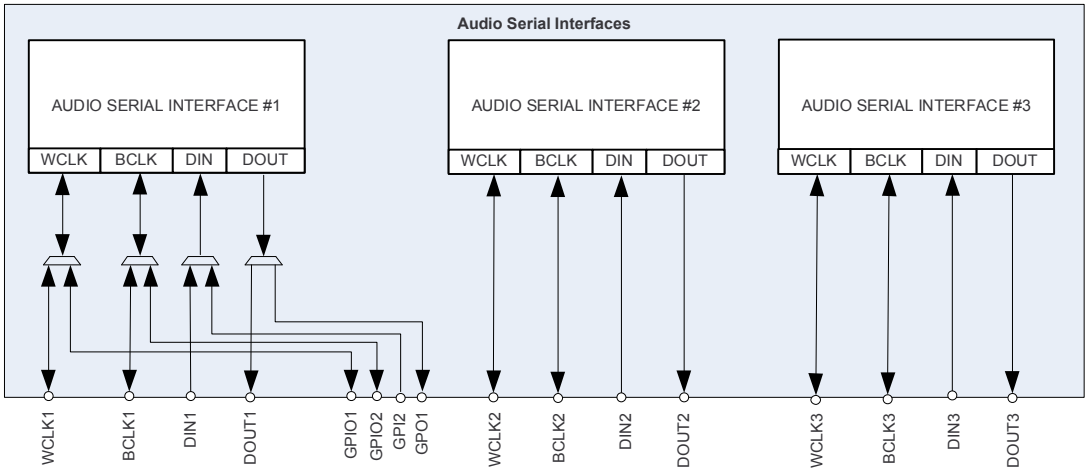


Figure 2-54. Typical Multiple Connections to Three Audio Serial Interfaces

Each audio bus on the TLV320AIC3212 is very flexible, including left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

Each of the three audio buses of the TLV320AIC3212 can be configured for left or right-justified, I²S, DSP, or TDM modes of operation, where communication with PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits. In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate word clocks.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple TLV320AIC3212s may share the same audio bus. When configuring an audio interface for six-wire mode, the ADC and DAC paths can operate based on separate bit clocks.

The TLV320AIC3212 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks.

The TLV320AIC3212 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen.

The TLV320AIC3212 further includes programmability to 3-state the DOUT line during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a 3-state output condition.

By default, when the word-clocks and bit-clocks are generated by the TLV320AIC3212, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

The TLV320AIC3212 contains advanced Digital Audio interfaces features to enable:

- Connections of Multiple Digital Audio interfaces
- 6-wire Digital Audio interfaces for separate uplink/downlink clocks or ADC/DAC clocks
- Time-Division Multiplexing (TDM)

2.9.1 Connecting Multiple Audio Digital Interfaces

The TLV320AIC3212 enables connections to multiple audio data buses. Figure 2-54 shows a typical example of utilizing the digital pins on the device to connect to four separate 4-wire digital audio buses, with up to three of these 4-wire buses receiving and sending digital audio data simultaneously. This configuration can be utilized when using I²C for control of the device. If only 3 total audio interface connections are needed (e.g. a fourth audio bus does not need to be muxed into Audio Serial Interface 1), either I²C or SPI control can be used. (Further details on SPI control and pins utilized can be found in Section 2.8.2 and Table 2-3.)

To configure each of the three audio serial interfaces, both the audio interface and the pins should be set up for appropriate routing of the signals. Audio Serial Interface #1 configuration registers are located in B0_P4_R1-R16. Audio Serial Interface #2 configuration registers are located in B0_P4_R17-R32. Audio Serial Interface #3 configuration registers are located in B0_P4_R33-R48. The pin muxing registers are located in B0_P4_R65-R96. Table 2-44 displays the appropriate register settings needed to implement the Audio Serial Interface configuration found in Figure 2-54.

Table 2-44. Register Settings for Typical Multiple Audio Digital Interface Connections

Pin	Interface Control (Codec Interface is Slave)	Interface Control (Codec Interface is Master)	Pin Control (Codec Interface as Slave)	Pin Control (Codec Interface as Master)
Audio Serial Interface #1 Word Clock to WCLK1 pin	B0_P4_R10_D[7:5] = 000	B0_P4_R10_D[7:5] = 001	B0_P4_R65_D[5:2] = 0001	
Audio Serial Interface #1 Bit Clock to BCLK1 pin	B0_P4_R10_D[4:2] = 000	B0_P4_R10_D[4:2] = 001	N/A	
Audio Serial Interface #1 Data Input to DIN1 pin	B0_P4_R5_D[4:0] = 00000 (default), B0_P4_R8_D[7:4] = 0101 (default) (ASI1-to-DAC datapath)		B0_P4_R68_D[6:5] = 01 (default)	
Audio Serial Interface #1 Data Output to DOUT1 pin	B0_P4_R6_D[3:0] = 0000 (default); B0_P4_R15_D[1:0] = 00 (default); B0_P4_R7_D[2:0] = 001 (default)		B0_P4_R67_D[4:1] = 0001 (default)	
Audio Serial Interface #2 Word Clock to WCLK2 pin	B0_P4_R26_D5 = 0 (default)	B0_P4_R26_D5 = 1	B0_P4_R69_D[5:2] = 0001 (default)	
Audio Serial Interface #2 Bit Clock to BCLK2 pin	B0_P4_R26_D2 = 0 (default)	B0_P4_R26_D2 = 1	B0_P4_R70_D[5:2] = 0001 (default)	
Audio Serial Interface #2 Data Input to DIN2 pin	B0_P4_R24_D[7:4] = 0101 (ASI2-to-DAC datapath)		B0_P4_R72_D[6:5] = 01	
Audio Serial Interface #2 Data Output to DOUT2 pin	B0_P4_R23_D[2:0] = 101 (ADC-to-ASI2 routing - Port 2), B0_P4_R31_D[1:0] = 00 (default)		B0_P4_R71_D[4:1] = 0001 (default)	
Audio Serial Interface #3 Word Clock to WCLK3 pin	B0_P4_R42_D5 = 0 (default)	B0_P4_R42_D5 = 1	B0_P4_R73_D[5:2] = 0001 (default)	
Audio Serial Interface #3 Bit Clock to BCLK3 pin	B0_P4_R42_D2 = 0 (default)	B0_P4_R42_D2 = 1	B0_P4_R74_D[5:2] = 0001 (default)	
Audio Serial Interface #3 Data Input to DIN3 pin	B0_P4_R40_D[7:4] = 0101 (ASI3-to-DAC datapath)		B0_P4_R76_D[6:5] = 01	
Audio Serial Interface #3 Data Output to DOUT3 pin	B0_P4_R39_D[2:0] = 110 (ADC-to-ASI3 routing - Port 3), B0_P4_R47_D[1:0] = 00 (default)		B0_P4_R75_D[4:1] = 0001 (default)	
Switch Audio Serial Interface #1 Word Clock to GPIO1 pin	B0_P4_R10_D[7:5] = 010	B0_P4_R10_D[7:5] = 011	B0_P4_R86_D[6:2] = 00001	B0_P4_R86_D[6:2] = 00100
Switch Audio Serial Interface #1 Bit Clock to GPIO2 pin	B0_P4_R10_D[4:2] = 010	B0_P4_R10_D[4:2] = 011	B0_P4_R87_D[6:2] = 00001	B0_P4_R87_D[6:2] = 00100
Switch Audio Serial Interface #1 Data Input to GPI2 pin	B0_P4_R5_D[4:0] = 01011		B0_P4_R92_D[5:4] = 01	B0_P4_R92_D[5:4] = 01

Table 2-44. Register Settings for Typical Multiple Audio Digital Interface Connections (continued)

Pin	Interface Control (Codec Interface is Slave)	Interface Control (Codec Interface is Master)	Pin Control (Codec Interface as Slave)	Pin Control (Codec Interface as Master)
Switch Audio Serial Interface #1 Data Output to GPO1 pin	B0_P4_R6_D[3:0] = 1100; B0_P4_R15_D[1:0] = 00 (default)		B0_P4_R96_D[4:1] = 1111	B0_P4_R96_D[4:1] = 1111

Since each interface can be configured separately as master or slave, the appropriate settings are displayed for both possible configurations for each of the three audio serial interfaces. When in master mode, the bit clock and work clock source can be derived from a variety of sources, and more details on the possible sources of these clocks can be found in the Clocking Section, Section 2.7.

2.9.2 Six-wire Digital Audio Interfaces

In some systems, it is desirable to have separate bit clock and word clock connections for the ADC audio path. For example, in a telephony audio interface, the uplink (ADC) and downlink (DAC) path may connect to different physical interfaces. Each of the audio interfaces on the TLV320AIC3212 can be configured in 6-wire mode to enable the additional ADC word clock and bit clock routing to/from several digital pins. Thus, in 6-wire mode, the bus contains DAC word clock (DAC_WCLK), DAC bit clock (DAC_BCLK), Data Input (DIN), ADC word clock (ADC_WCLK), ADC bit clock (ADC_BCLK), and Data Output (DOUT).

The digital pins that can be used for the separate ADC clocks are GPIO1, GPIO2, GPI1, GPI2, GPI3, and GPI4. Note that GPI3 and GPI4 can only be utilized for these functions when SPI control is used, since these two pins become I^2C address pins when the codec is controlled by the I^2C protocol. Similarly, GPI1 can only be utilized in I^2C mode, since this pin is utilized by the SPI bus as the SCLK signal.

2.9.2.1 Six-Wire Mode as Bus Master

When the audio interface acts as a master on the audio bus, the word clock and bit clock for the audio serial interface can be routed to two sets of pins simultaneously. In other words, the word clock can be routed to WCLK1, and also to either GPIO1 or GPIO2. The bit clock can be routed to BCLK1 pin, and also to either GPIO1 or GPIO2. Figure 2-55 shows an example where the GPIO pins are utilized for the ADC word clock and bit clock, while the TLV320AIC3212 is still able to utilize Audio Serial Interfaces #2 and #3 for other digital audio (4-wire) connections. While this figure shows Audio Serial Interface #1 configured for six-wire mode, any of the audio serial interfaces could be set up for six-wire mode.

To configure the GPIO1 pin as an output for Audio Serial Interface #1 clocks, set B0_P4_R86_D[6:2] to "10000" for ASI1 word clock or "10001" for ASI1 bit clock. To configure the GPIO1 pin as an output for Audio Serial Interface #2 clocks, set B0_P4_R86_D[6:2] to "10010" for ASI2 word clock or "10011" for ASI2 bit clock. To configure the GPIO1 pin as an output for Audio Serial Interface #3 clocks, set B0_P4_R86_D[6:2] to "10100" for ASI3 word clock or "10101" for ASI3 bit clock.

To configure the GPIO2 pin as an output for Audio Serial Interface #1 clocks, set B0_P4_R87_D[6:2] to "10000" for ASI1 word clock or "10001" for ASI1 bit clock. To configure the GPIO2 pin as an output for Audio Serial Interface #2 clocks, set B0_P4_R87_D[6:2] to "10010" for ASI2 word clock or "10011" for ASI2 bit clock. To configure the GPIO2 pin as an output for Audio Serial Interface #3 clocks, set B0_P4_R86_D[6:2] to "10100" for ASI3 word clock or "10101" for ASI3 bit clock.

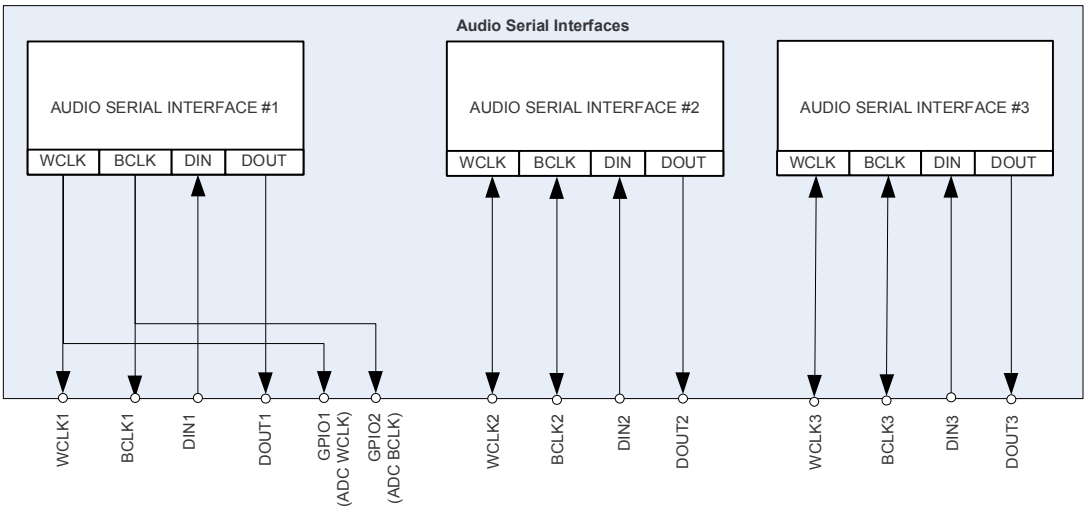


Figure 2-55. Six-Wire Audio Serial Interface with ADC WCLK and BCLK as Outputs

2.9.2.2 Six-Wire Mode as Bus Slave

When the audio interface acts as a slave on the audio bus, separate bit clocks and word clocks can be sent to the DAC datapath and the ADC datapath. This can be useful in a few common system scenarios:

- Separate uplink and downlink WCLK and BCLK (similar sampling rates)
- Separate uplink and downlink WCLK and BCLK (Uplink data rate at 8 kHz or 16 kHz with downlink data rate at 48 kHz)
- ADC Engine running at separate sample rate from DAC Engine

Figure 2-56 shows an example for sending in the separate ADC word clock and bit clock into GPI1 and GPI2, respectively. This configuration could be utilized for I^2C control mode. The TLV320AIC3212 is still able to have Audio Serial Interfaces #2 and #3 connections for other digital audio (4-wire) buses. While this figure shows Audio Serial Interface #1 configured for six-wire mode, any of the audio serial interfaces could be set up for six-wire mode with ADC WCLK and BCLK inputs.

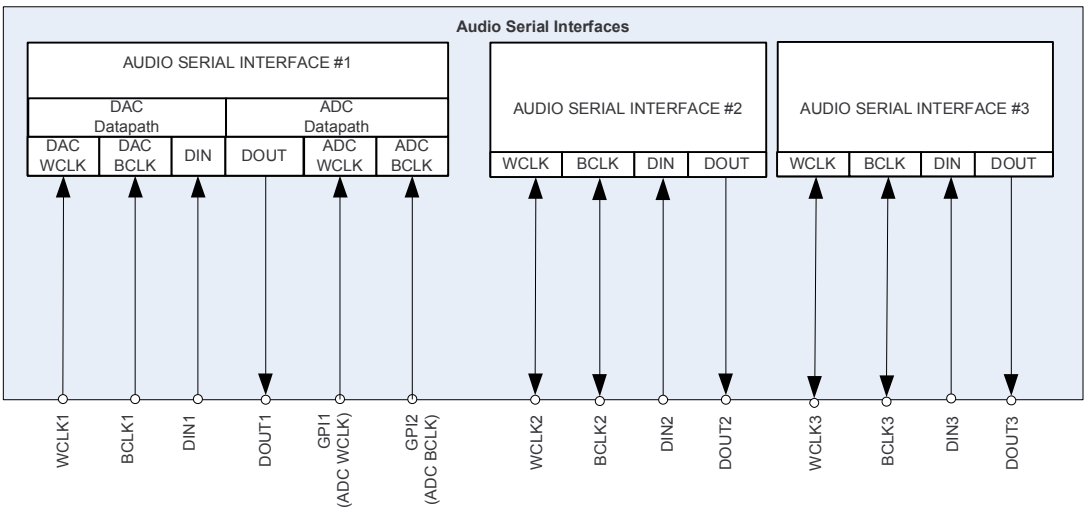


Figure 2-56. Six-Wire Audio Serial Interface with ADC WCLK and BCLK as Inputs (I^2C mode)

Figure 2-57 shows an example for sending in the separate ADC word clock and bit clock into GPI3 and GPI4, respectively. This configuration could be utilized for SPI control mode. The TLV320AIC3212 is still able to have Audio Serial Interfaces #2 and #3 connections for other digital audio (4-wire) buses.

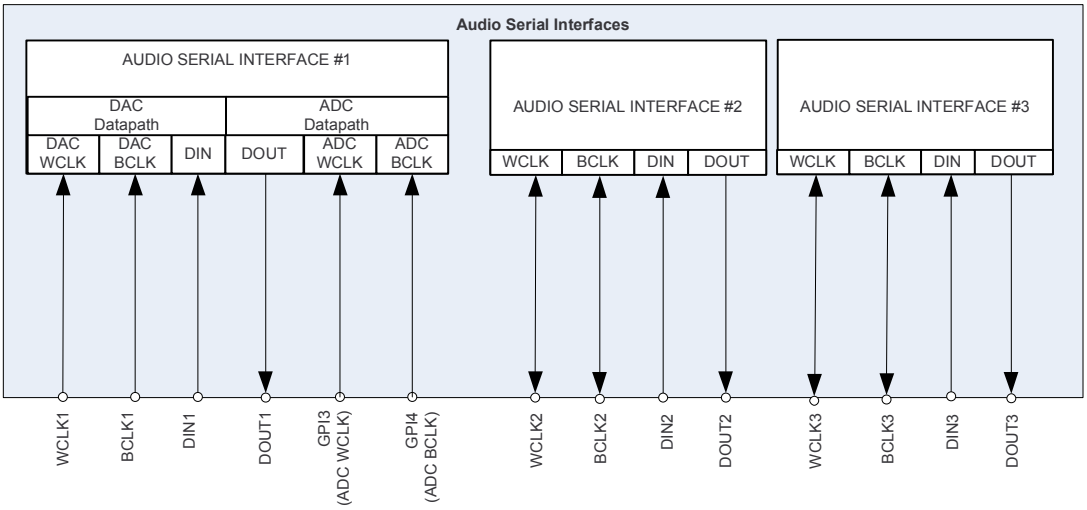


Figure 2-57. Six-Wire Audio Serial Interface with ADC WCLK and BCLK as Inputs (SPI mode)

While Figure 2-56 and Figure 2-57 show Audio Serial Interface #1 configured for six-wire mode with ADC word clock and bit clock as input, any of the audio serial interfaces could be similarly set up for six-wire mode. To configure one of the GPIOx or GPIx pins as an ADC input for Audio Serial Interface #1, the pin should be configured to Input Mode, and B0_P4_R16_D[6:4] should be set to non-zero (if utilizing as ADC word clock) or B0_P4_R16_D[2:0] should be set to non-zero (if utilizing as ADC bit clock). Similarly, to configure one of these pins as an ADC input for Audio Serial Interface #2, the pin should be configured to Input Mode, and B0_P4_R32_D[6:4] should be set to non-zero (if utilizing as ADC word clock) or B0_P4_R32_D[2:0] should be set to non-zero (if utilizing as ADC bit clock). To configure one of these pins as an ADC input for Audio Serial Interface #3, the pin should be configured to Input Mode, and B0_P4_R48_D[6:4] should be set to non-zero (if utilizing as ADC word clock) or B0_P4_R48_D[2:0] should be set to non-zero (if utilizing as ADC bit clock).

2.9.3 Audio Formats

Each Audio Serial Interface supports left or right-justified, I^2S, DSP, or mono PCM modes. In addition, time-division multiplexing (TDM) can be implemented in each of these formats to enable multi-channel operation.

2.9.3.1 Right Justified Mode

Audio Serial Interface 1 can be put into Right Justified Mode by programming B0_P4_R1_D[7:5] = 010. Audio Serial Interface 2 can be put into Right Justified Mode by programming B0_P4_R17_D[7:5] = 010. Audio Serial Interface 3 can be put into Right Justified Mode by programming B0_P4_R33_D[7:5] = 010. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

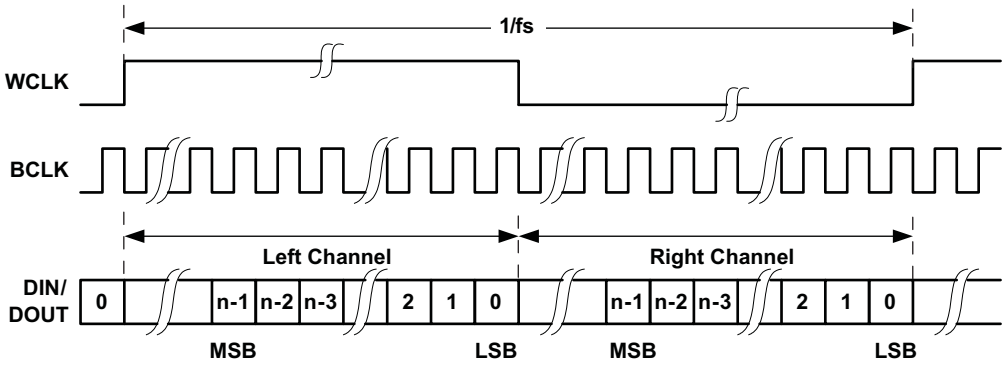


Figure 2-58. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

2.9.3.2 Left Justified Mode

Audio Serial Interface 1 can be put into Left Justified Mode by programming B0_P4_R1_D[7:5] = 011. Audio Serial Interface 2 can be put into Left Justified Mode by programming B0_P4_R17_D[7:5] = 011. Audio Serial Interface 3 can be put into Left Justified Mode by programming B0_P4_R33_D[7:5] = 011. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

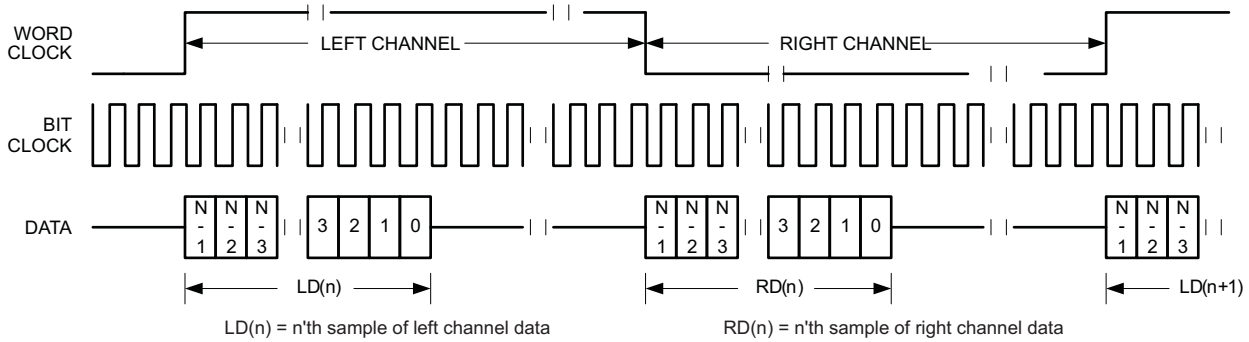


Figure 2-59. Timing Diagram for Left-Justified Mode

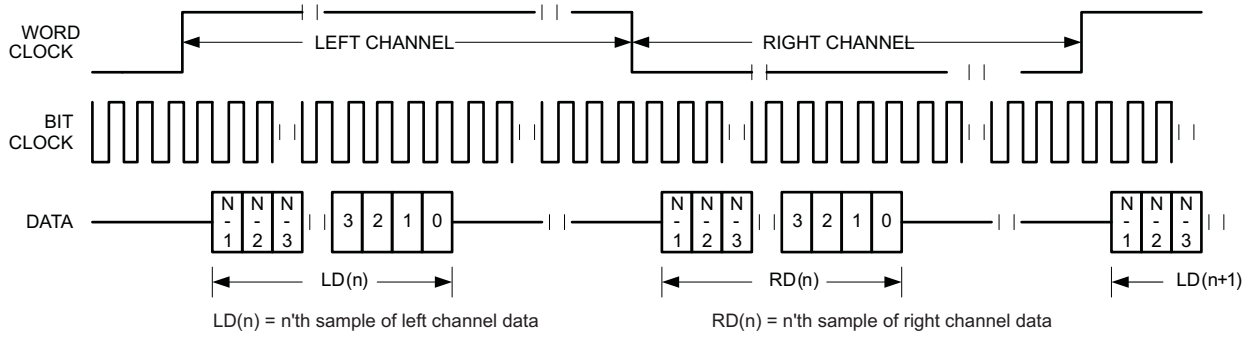


Figure 2-60. Timing Diagram for Left-Justified Mode with Offset=1

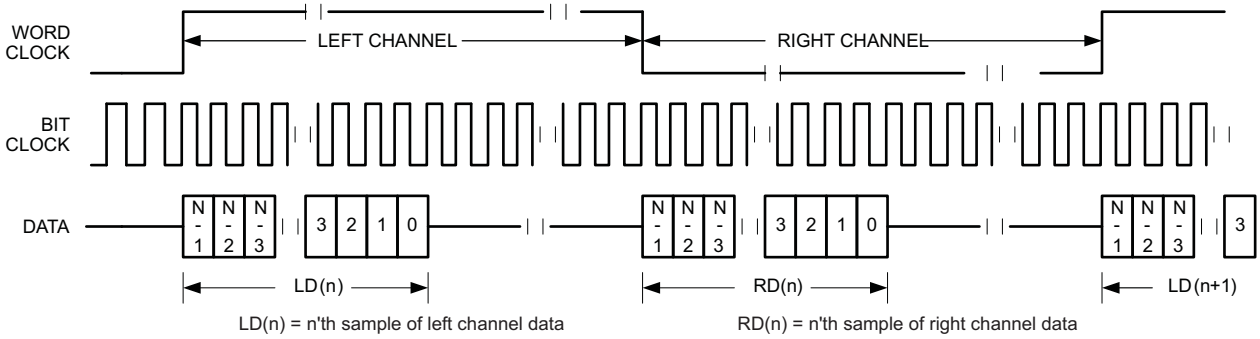


Figure 2-61. Timing Diagram for Left-Justified Mode with Offset=0 and inverted bit clock

For Left-Justified mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.9.3.3 I²S Mode

Audio Serial Interface 1 can be put into I²S Mode by programming B0_P4_R1_D[7:5] = 000. Audio Serial Interface 2 can be put into I²S Mode by programming B0_P4_R17_D[7:5] = 000. Audio Serial Interface 3 can be put into I²S Mode by programming B0_P4_R33_D[7:5] = 000. In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

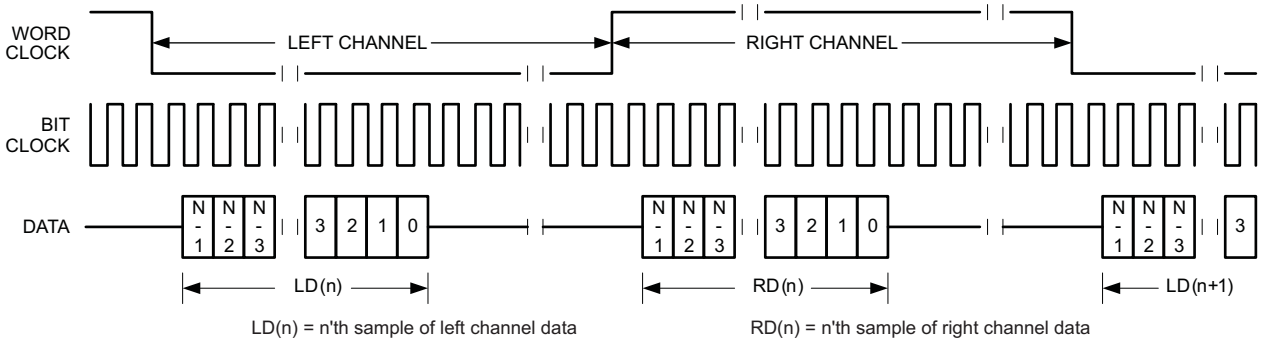


Figure 2-62. Timing Diagram for I²S Mode

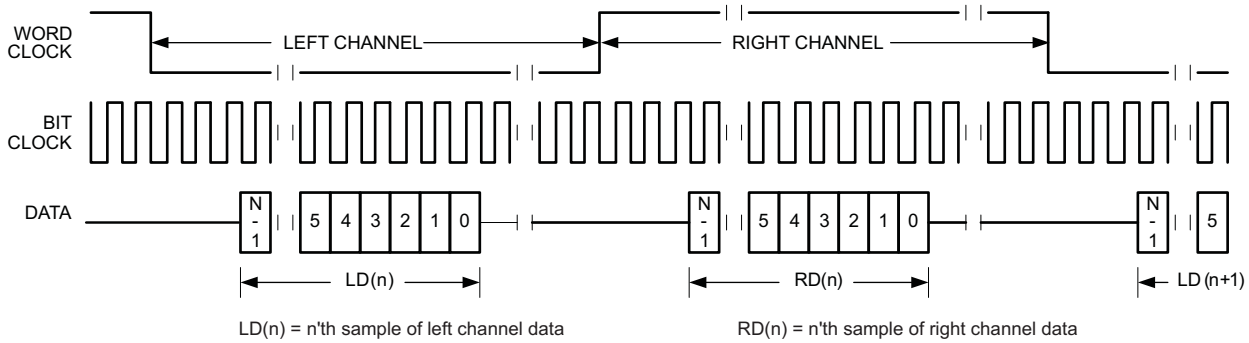


Figure 2-63. Timing Diagram for I²S Mode with offset=2

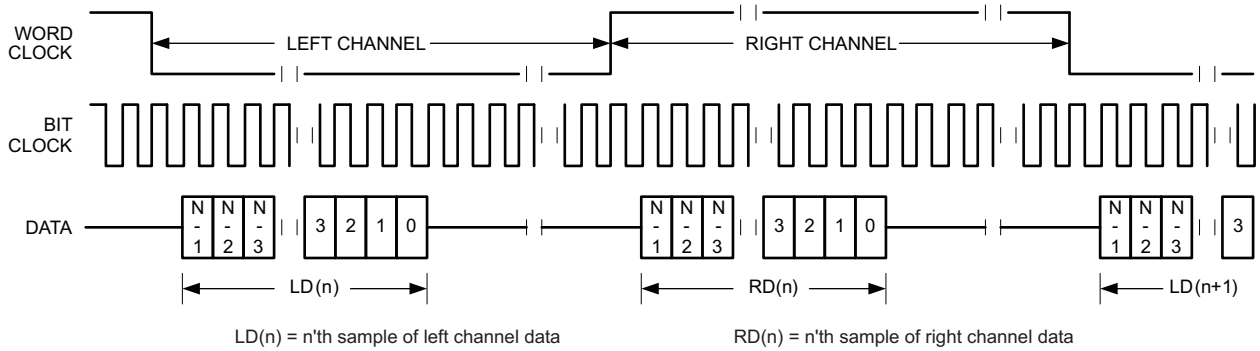


Figure 2-64. Timing Diagram for I²S Mode with offset=0 and bit clock invert

For I²S mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.9.3.4 DSP Mode

Audio Serial Interface 1 can be put into DSP Mode by programming B0_P4_R1_D[7:5] = 001. Audio Serial Interface 2 can be put into DSP Mode by programming B0_P4_R17_D[7:5] = 001. Audio Serial Interface 3 can be put into DSP Mode by programming B0_P4_R33_D[7:5] = 001. In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

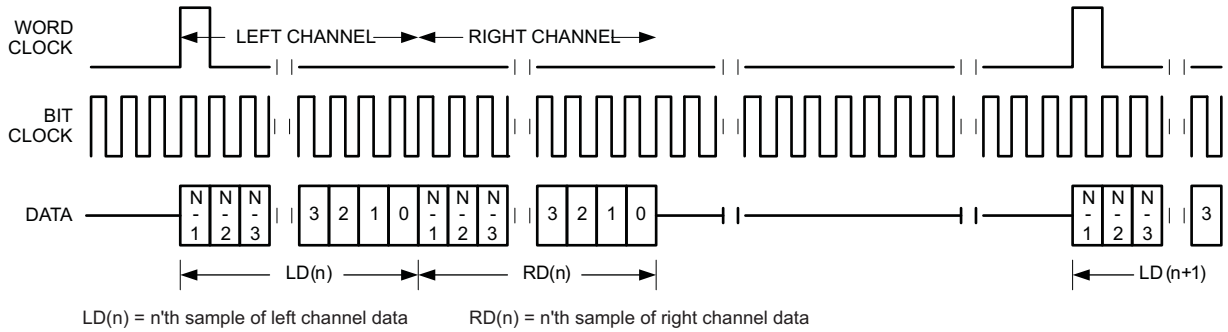


Figure 2-65. Timing Diagram for DSP Mode

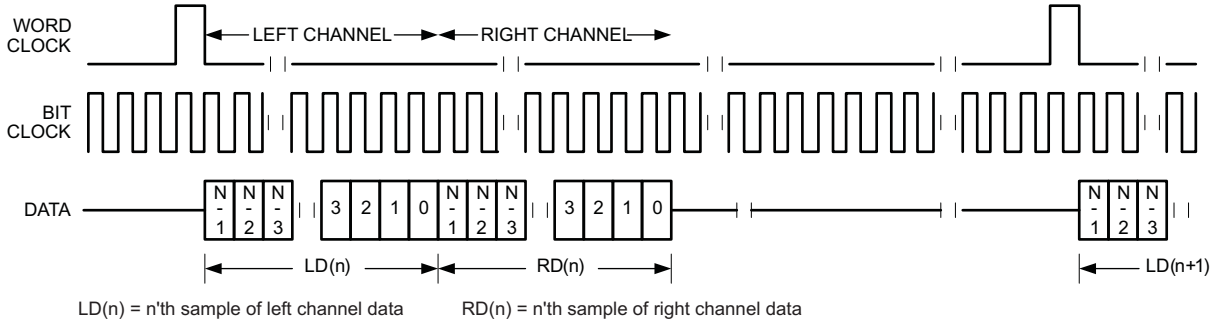


Figure 2-66. Timing Diagram for DSP Mode with offset = 1

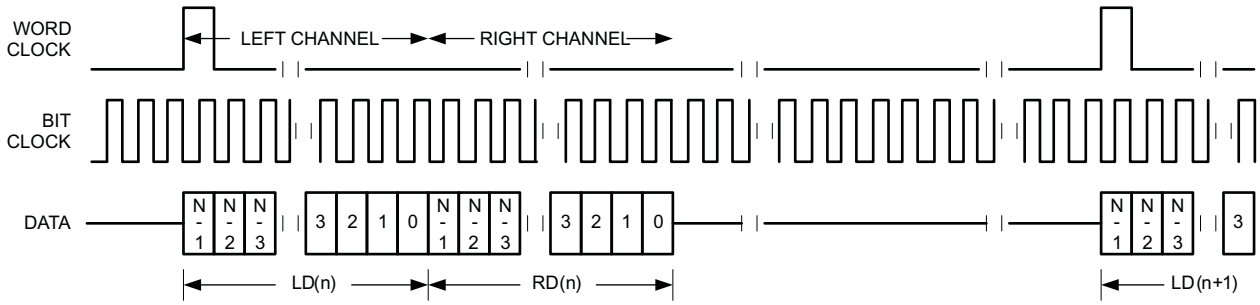


Figure 2-67. Timing Diagram for DSP Mode with offset = 0 and bit clock inverted

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.9.3.5 Mono PCM Mode

Audio Serial Interface 1 can be put into Mono PCM Mode by programming B0_P4_R1_D[7:5] = 100. Audio Serial Interface 2 can be put into DSP Mode by programming B0_P4_R17_D[7:5] = 100. Audio Serial Interface 3 can be put into DSP Mode by programming B0_P4_R33_D[7:5] = 100. In mono PCM mode, the rising edge of the word clock starts the data transfer of the single channel of data. Each data bit is valid on the falling edge of the bit clock.

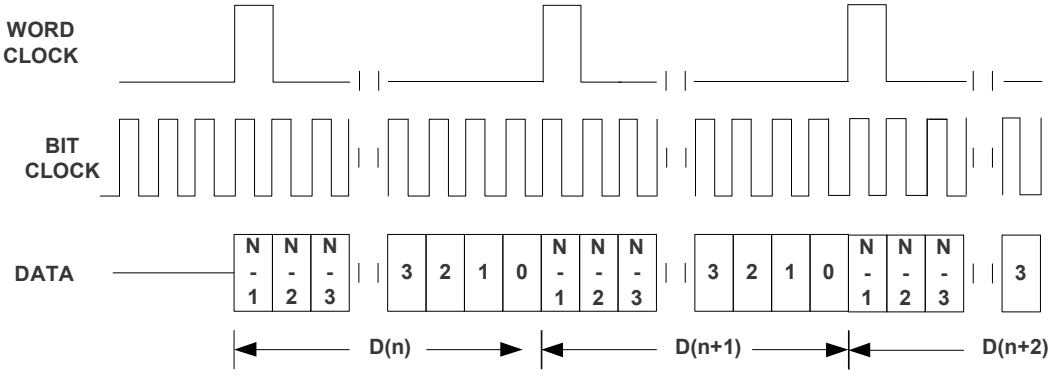


Figure 2-68. Timing Diagram for Mono PCM Mode

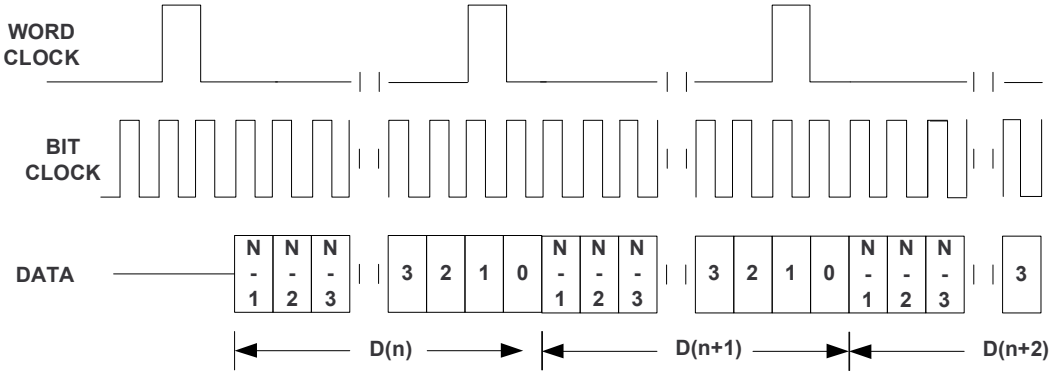


Figure 2-69. Timing Diagram for Mono PCM Mode with offset=2

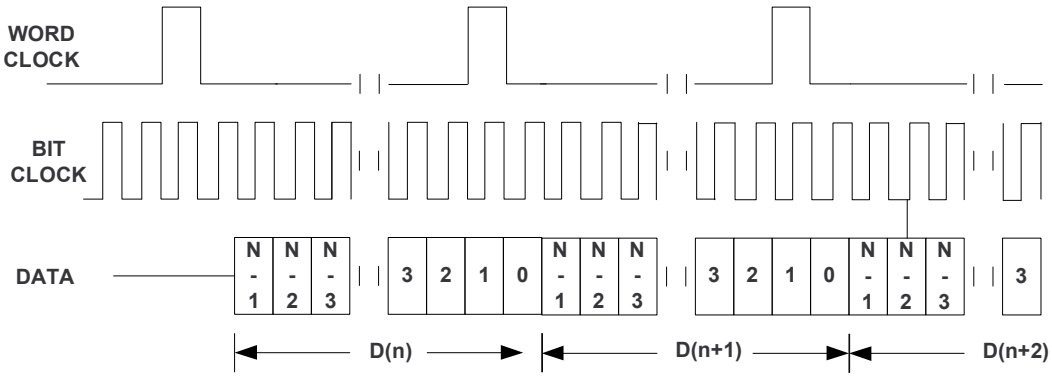


Figure 2-70. Timing Diagram for Mono PCM Mode with offset=2 and bit clock inverted

For mono PCM mode, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.9.4 Time-Division Multiplexing (TDM) Configuration

The TLV320AIC3212 can utilize TDM techniques to enable multiple codecs to transmit/receive on a single digital audio interface bus.

2.9.4.1 Single Host, Multiple Audio Codecs

Using the offset programmability and the DOUT line 3-state feature, the TLV320AIC3212 enables the flexibility where multiple TLV320AIC3212 devices can be interfaced together and can communicate to a host/multimedia processor using a single digital audio serial interface. Figure 2-71 displays a typical configuration where M devices are connected to a single host processor.

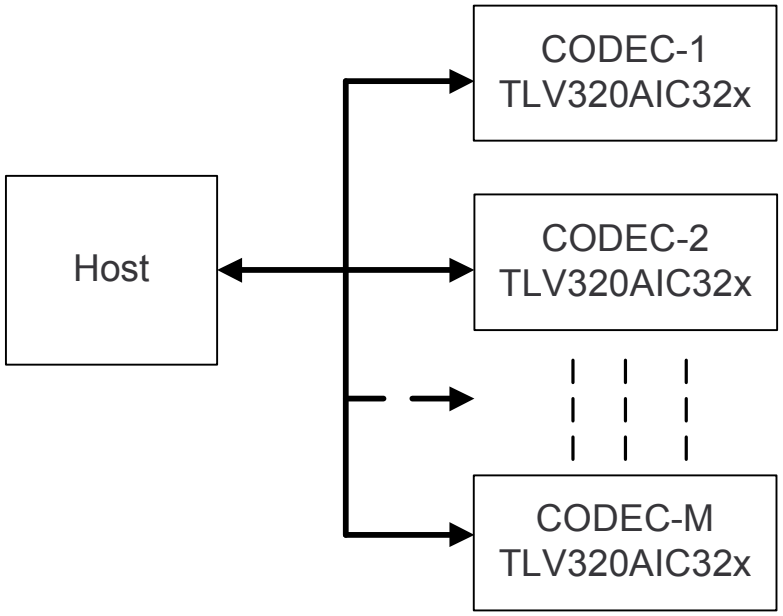


Figure 2-71. Interfacing Multiple TLV320AIC3212 Devices Using Single I^2S Interface

By changing the programmable offset for each device, the bit clock in each frame where the data begins can be changed, and the serial data output driver (DOUT) also can be programmed to a 3-state mode during all bit clocks except when valid data is being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected based on the programmed offset.

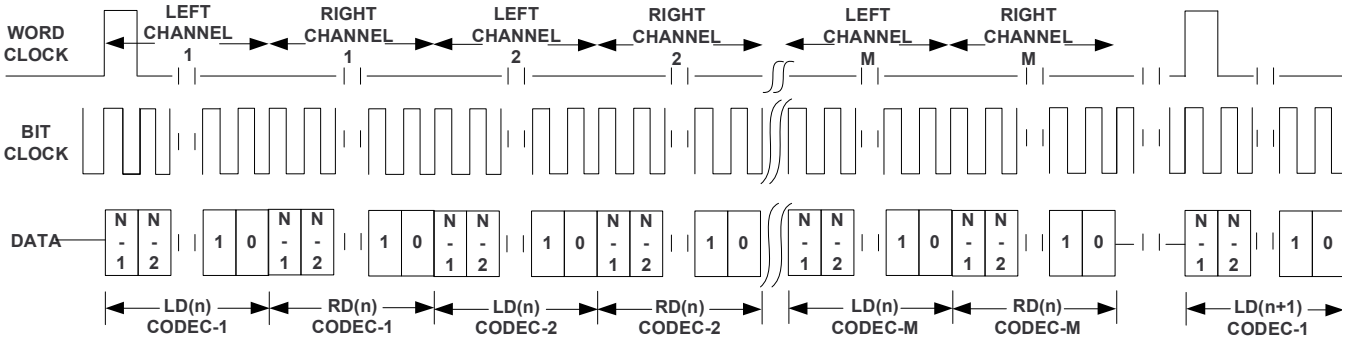


Figure 2-72. DSP Timing for Multiple Devices Interfaced Together, Sequential Left/Right Pairs

The digital audio serial interface timing diagram for the interface in Figure 2-71 is shown in Figure 2-72. In this particular configuration, the TLV320AIC3212 (or any other TLV320AIC32x codec) is programmed for DSP mode with N-bit word length per channel. The offset programmed for the Codec-1 is 0, for Codec-2 it is 2N, and likewise, the offset programmed for the Codec-M is (M-1) x 2N. In this TDM mode, the number of bit-clocks per frame should be greater than M*2N. The TLV320AIC3212 allows a maximum offset of 255 bit clocks, and this enables connections of up to 4 codecs for 32-bit stereo data and 8 codecs for 16-bit stereo data.

For each of the three individual Digital Audio interfaces, this offset controls when data is received and sent by these interfaces. For Audio Serial Interface 1, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R2. For Audio Serial Interface 2, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R18. For Audio Serial Interface 3, this offset can be set to a value in the range of 0 to 255 bit clocks by programming B0_P4_R34. When utilized in DSP mode, each of these offsets will determine the start of the left channel, with the right channel data immediately following the LSB of the left channel.

2.9.4.1.1 Time Slot Mode

In addition, Audio Serial Interface 1 can also control the offset of the right channel with respect to the end of the left channel of data. This is achieved by enabling Time Slot Mode (setting B0_P4_R8_D0) and configuring the Right Channel Offset 2 (in the range of 0 to 255 bit clocks) in B0_P4_R3. Thus, the Right Channel Offset 2 control allows us to place the right channel anywhere in the frame after the left channel, and this functionality can be utilized in each of the audio formats (DSP, left or right-justified, or I^2S).

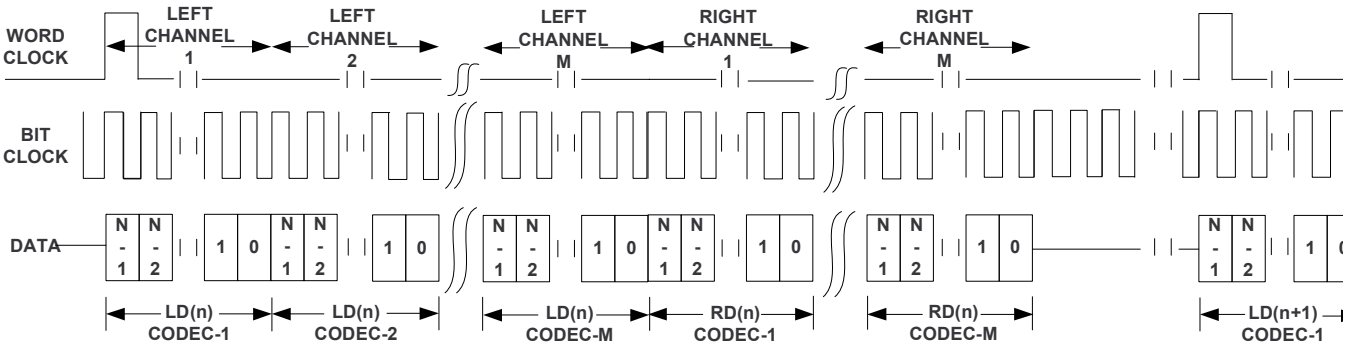


Figure 2-73. DSP Timing for Multiple Devices Interfaced Together, Grouped Left Channels and Right Channels

By utilizing Time Slot Mode, the individual left and right channels can be grouped together , as shown in Figure 2-73. Assuming each channel contains N bits in this example, Codec-1 would have an offset1=0 and offset2=M*N, Codec-2 would have an offset1=N and offset2=M*N, and likewise, Codec-M would have an offset1=(M-1)*N and offset2=M*N.

2.9.5 Routing for Audio Serial Interfaces

Figure 2-74 displays a summary of Audio Serial Interface routings for typical stereo/mono configurations. Default routings are indicated in blue, and the associated registers are listed in the diagram for convenience. For further details on register setup, consult the register map and also the tables in Section 2.2.3.1.

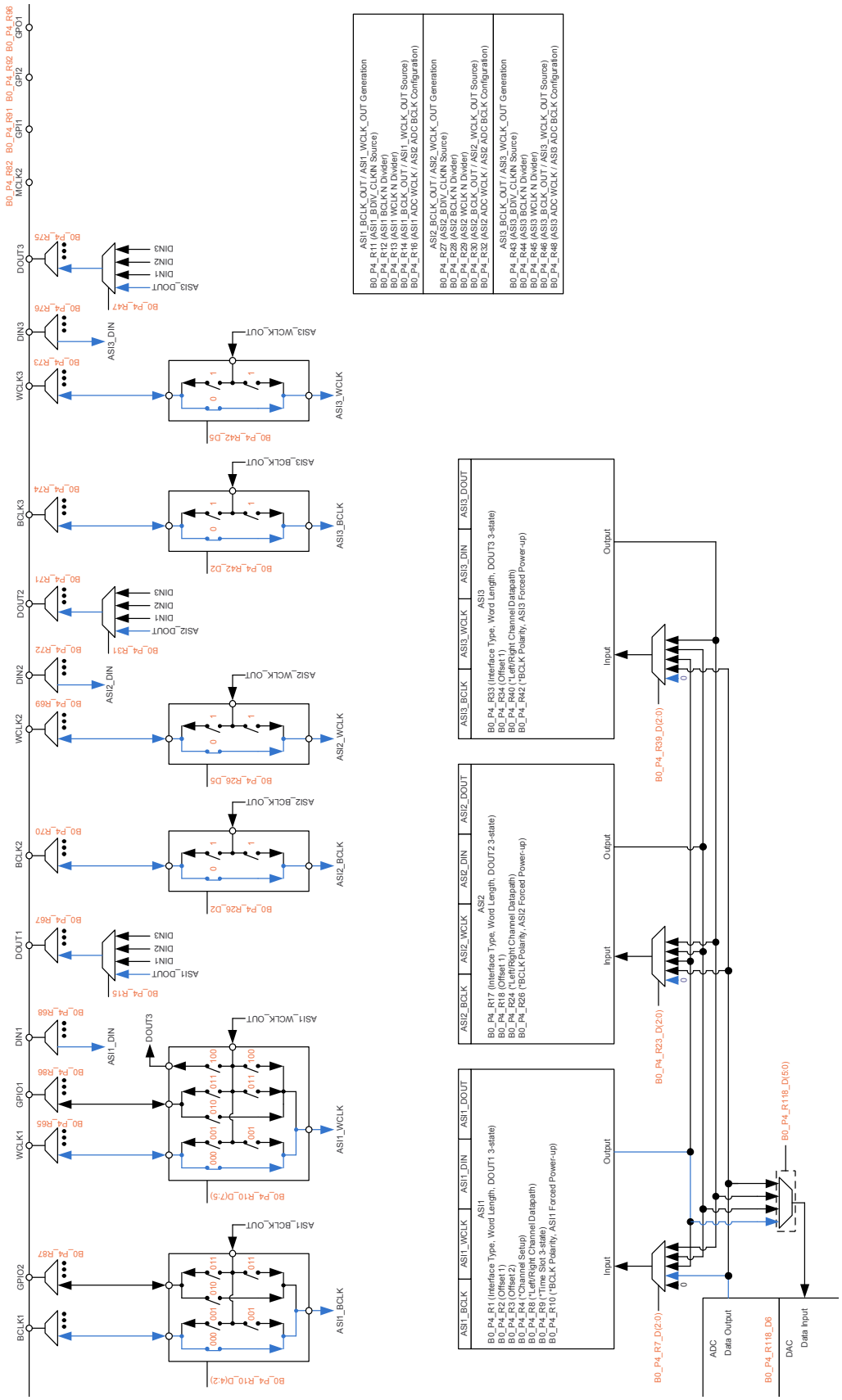


Figure 2-74. Summary of Routing for Audio Serial Interfaces

In order to setup routing from the digital pins to the audio serial interfaces, the pins need to be configured to connect to the desired interface. This table is valid for a typical configuration and assumes that B0_P4_R5_D[4:0]≠"01011" (i.e. GPI2 not used for ASI#1 DIN pin) and B0_P4_R6_D[3:0]≠"1100" (i.e. GPO1 not used as ASI#1 DOUT pin). The most important configuration registers for each audio serial interface is listed in the diagram with each ASI block. Once data has been routed to/from the digital pins, data can be routed to other audio serial interfaces, or sent to/from the DAC/ADC. In normal audio interface mode (stereo/mono), the TLV320AIC3212 can select one of the three audio serial interfaces to/from the ADC/DAC. Note that, by default, the data routing from the ADC to Audio Serial Interface #2 (B0_P4_R23_D[2:0]) and Audio Serial Interface #3 (B0_P4_R39_D[2:0]) is disabled, and when these muxes are switched to disabled, the ASI2_DOUT and ASI3_DOUT signals become high-impedance outputs.

2.10 Power Supply

The TLV320AIC3212 integrates a large amount of digital and analog functionality, and each of these blocks can be powered separately to enable the system to select appropriate power supplies for desired performance and power consumption. The device has separate power domains for digital IO, digital core, analog core, analog input, receiver driver, charge-pump input, headphone driver, and speaker drivers. If desired, all of the supplies (except for the supplies for speaker drivers, which can directly connect to the battery) can be connected together and be supplied from one source in the range of 1.65 to 1.95V. Individually, the IOVDD voltage can be supplied in the range of 1.1V to 3.6V. For improved power efficiency, the digital core power supply can range from 1.26V to 1.95V. The analog core voltages (AVDD1_18, AVDD2_18, AVDD4_18, and AVDD_18) can range from 1.5V to 1.95V. The microphone bias (AVDD3_33) and receiver driver supply (RECVDD_33) voltages can range from 1.65V to 3.6V. The charge-pump input voltage (CPVDD_18) can range from 1.26V to 1.95V, and the headphone driver supply (HVDD_18) voltage can range from 1.5V to 1.95V. The speaker driver voltages (SLVDD, SRVDD, and SPK_V) can range from 2.7V to 5.5V.

The TLV320AIC3212 has numerous power-supply connections which allow various optimizations for low system power.

- **IOVdd** - The IOVdd pin supplies the digital IO cells of the device. The voltage of IOVdd can range from 1.1 to 3.6V and is determined by the digital IO voltage of the rest of the system.
- **DVdd** - This pin supplies the digital core of the device. Lower DVdd voltages cause lower power dissipation. If efficient switched-mode power supplies are used in the system, system power can be optimized using low DVdd voltages. the full clock range is only supported with DVdd in the range of 1.65 to 1.95V. Also, operation with DVdd down to 1.26V is possible. (See Table 2-40)
- **AVdd1_18, AVdd2_18, AVdd4_18, AVdd_18** - These pins supply the analog core of the device. The analog core voltage (AVdd) should be in the range of 1.5 to 1.95V for specified performance. For AVdd voltages above 1.8V, the internal common mode voltage can be set to 0.9V (B0_P1_R8_D2=0, default) resulting in 500mVrms full-scale voltage internally. For analog voltages below 1.8V, the internal common mode voltage should be set to 0.75V (B0_P1_R8_D2=1), resulting in 375mVrms internal full scale voltage.

NOTE: At powerup, AVDDx_18 is weakly connected to DVdd. This coarse AVDDx_18 generation must be turned off by writing B0_P1_R1_D3 = 0 at the time AVDDx_18 is applied.

- **AVdd3_33** - This pin supplies both microphone biases on the device. This analog voltage should be in the range of 1.65 to 3.6V for specified performance. For AVdd voltages above 1.8V, the internal common mode voltage can be set to 0.9V (B0_P1_R8_D2=0, default) resulting in 500mVrms full-scale voltage internally. For AVdd voltages below 1.8V, the internal common mode voltage should be set to 0.75V (B0_P1_R8_D2=1), resulting in 375mVrms internal full scale voltage. *The AVdd3_33 voltage must be greater than or equal to the AVDDx_18 supplies.*
- **HVdd_18** - This pin supplies the headphone amplifier of the device. The headphone supply voltage should be in the range of 1.5 to 1.95V for specified performance. This power supply can also be connected to the analog core power supplies.
- **CPVdd_18** - This pin supplies the integrated charge pump of the device. The charge pump voltage should be in the range of 1.26 to 1.95V for specified performance. This power supply can also be connected to the analog core power supplies.

- **RECVdd_33** - This pin supplies the receiver amplifier of the device. The receiver supply voltage should be in the range of 1.65 to 3.6V for specified performance.
- **SLVdd, SRVdd, SPK_V** - These pins supply the speaker amplifiers of the device. The speaker supply voltages should be in the range of 2.7 to 5.5V for specified performance. Note that, even if the integrated speaker drivers are not utilized on the device, these supplies should still be connected (typically to battery voltage) and at a greater or equal voltage to all the other power supplies. The SPK_V should be connected to the same voltage as SLVdd and SRVdd, and this pin draws less current than the SLVdd and SRVdd pins. It is recommended to include a low-pass filter for this SPK_V node to enable best speaker driver performance. The speaker supply voltages can also be connected to VBAT for monitoring by the SAR ADC. Note that the VBAT pin is not a supply pin, but rather only used for monitoring the battery voltage.

2.11 Reference Voltage

All audio data converters require a DC reference voltage. The TLV320AIC3212 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with a good PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF_AUDIO pin to analog ground (AVSS).

To achieve low power consumption, this audio reference block is powered down when all analog blocks inside the device are powered down. In this condition, the VREF_AUDIO pin is 3-stated. On powerup of any analog block, the audio reference block is also powered up and the VREF_AUDIO pin settles to its steady-state voltage after the settling time (a function of the de-coupling capacitor on the VREF_AUDIO pin). This time is approximately equal to 1 second when using a 1µF decoupling capacitor. In the event that a faster power-up is required, either the audio reference block can be kept powered up (even when no other analog block is powered up) by programming B0_P1_R122_D2 = 1. However, in this case, an additional 100µA of current from AVdd is consumed. Additionally, to achieve a faster powerup, a fast-charge option is also provided where the charging time can be controlled between 40ms and 120ms by programming B0_P1_R122_D[1:0]. By default, the fast charge option is enabled.

In addition, the TLV320AIC3212 can also generate a separate 1.25V DC reference which is utilized by the SAR ADC for measurement. This SAR reference voltage must also be filtered externally using a minimum 1µF capacitor connected from the VREF_SAR pin to analog ground (AVSS).

To achieve low power consumption, this SAR reference block is powered down by default when SAR conversations are not occurring. The system could utilize this reference voltage outside of SAR ADC conversions by powering it continuously by programming B0_P3_R6_D5 =0.

2.12 Device Special Functions

2.12.1 SAR ADC

This section describes how to use the SAR ADC for the functions:

- Temperature measurement
- Battery measurement
- Auxiliary voltage measurement

The analog inputs of the TLV320AIC3212 are shown in Figure 2-75.

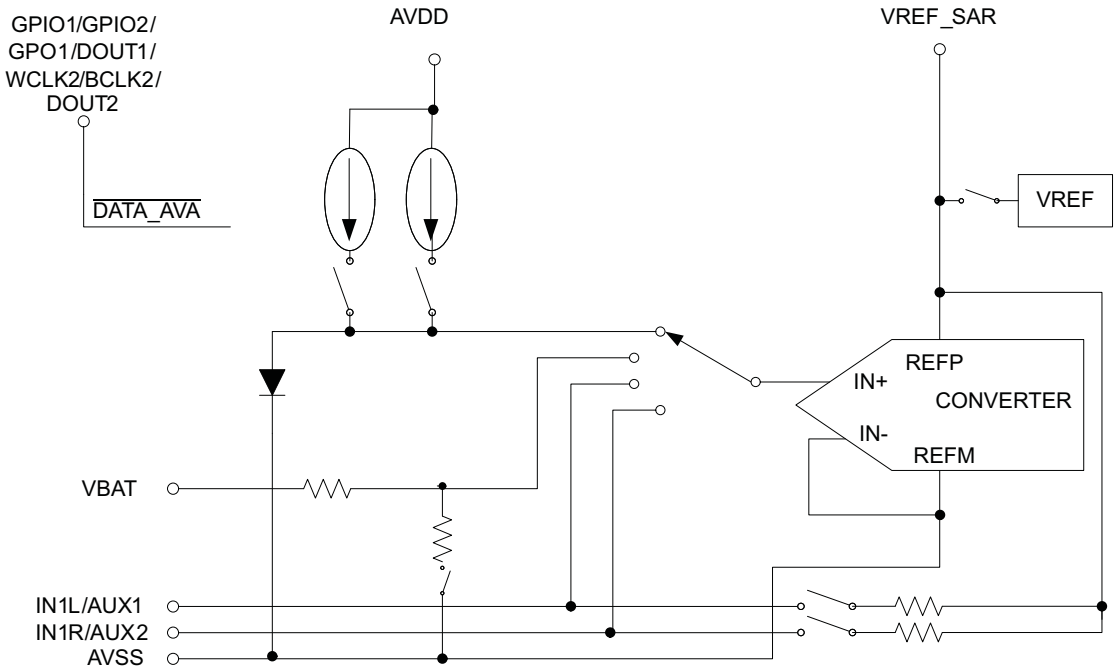


Figure 2-75. Simplified Diagram of the SAR ADC Analog Input Section

The ADC is controlled by an ADC control register (B0_P3_R3_D[7:0]). Several modes of operation are possible, depending on the bits set in the control register. Channel selection, scan operation, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the following sections for each type of analog input. The results of conversions made are stored in the appropriate result register.

The SAR ADC can be powered down forcefully by writing to B0_P3_R2_D7. Overall SAR configuration and mode is controlled by writing to B0_P3_R3_D[7:0].

Data Format

The TLV320AIC3212 output data is unsigned binary format and can be read from two 8-bit registers over the Control interface (SPI or I^2C).

Voltage Reference

The TLV320AIC3212 can use an internal voltage reference of 1.25 V or an external reference through the reference control register (B0_P3_R6).

The internal reference voltage should only be used in the single-ended mode for battery monitoring, for temperature measurement, and for using the auxiliary inputs.

The TLV320AIC3212 may use an external voltage reference (B0_P3_R6). In many systems, a 2.5-V reference is supplied; however, this device supports a reference voltage up to the AVDDx_18 level. The external reference should be a low-noise signal and accordingly, depending on the application, it might need some R-C filtering at the VREF_SAR pin.

This voltage reference should only be used in the single-ended mode for measuring the auxiliary inputs (IN1L/AUX1, IN1R/AUX2, and VBAT).

Variable Resolution

The TLV320AIC3212 provides three different resolutions for the ADC: 8, 10, or 12 bits. Lower resolutions are often practical for measurements such as system voltages. Performing the conversions at lower resolution reduces the amount of time it takes for the ADC to complete its conversion process, which lowers power consumption. The ADC resolution can be programmed by writing to B0_P3_R2_D[6:5].

2.12.1.1 Conversion Clock and Conversion Time

The TLV320AIC3212 contains an internal oscillator, which is used to drive the state machines inside the device that perform the many functions of the part. MCLK1 is also available as a high frequency clock source. The clock source (internal or MCLK1) is selected by writing to B0_P0_R23_D7. This clock is divided down to provide a clock to run the SAR ADC. The division ratio for this clock is set by writing to B0_P3_R2_D[4:3]. The ability to change the conversion clock rate allows the user to choose the optimal value for the resolution, speed, and power. If the internal oscillator is used for the conversion clock, the ADC is limited to 8-bit resolution. Using a 4-MHz conversion clock is suitable for 10-bit resolution; 12-bit resolution requires that the conversion clock run at 1 or 2 MHz.

To avoid asynchronous issues, the system should use the same value for both B0_P0_R23_B7 and B0_P3_R17_B7.

Details for clock selection can be seen in Figure Figure 2-76.

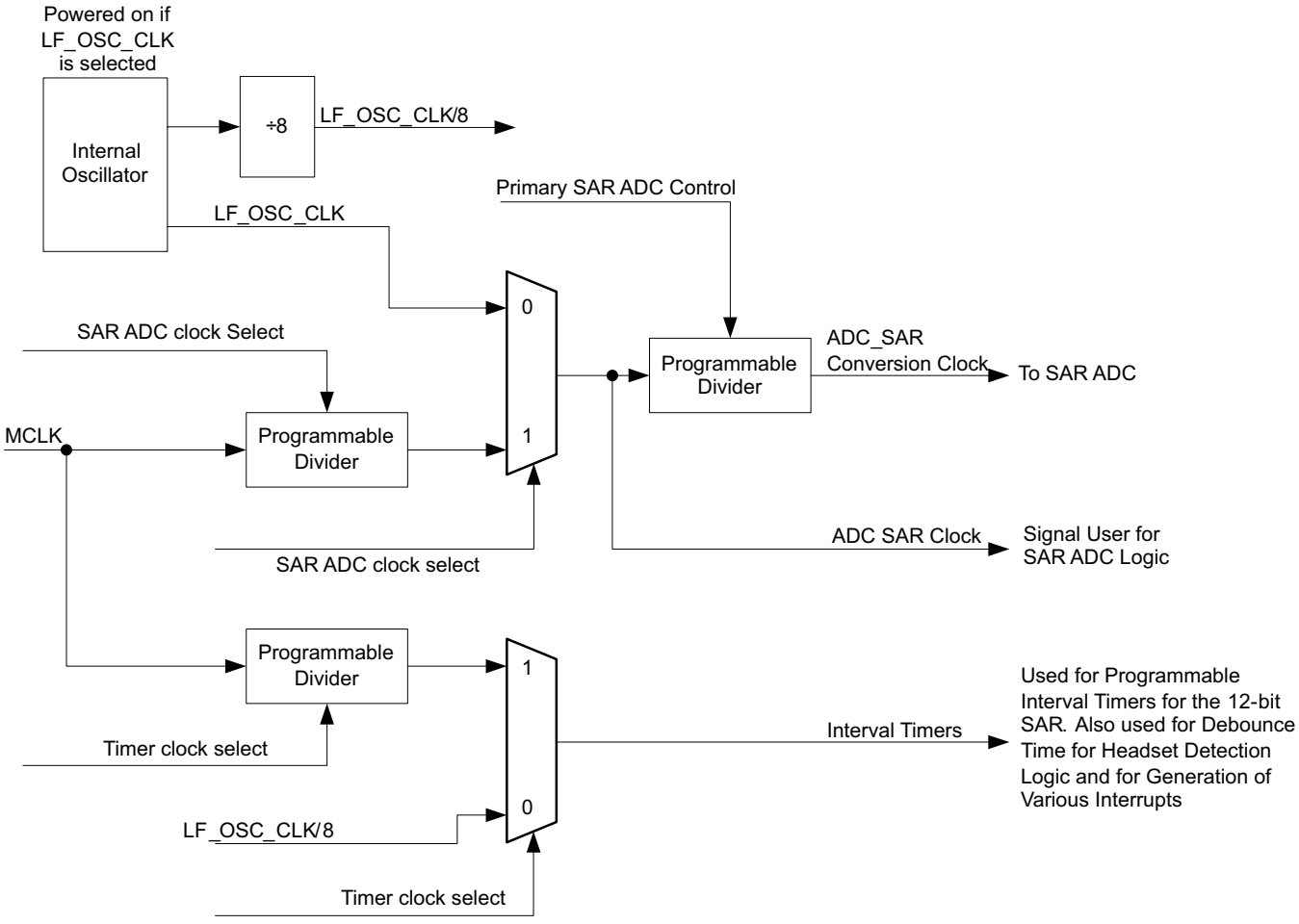


Figure 2-76. SAR ADC and Interval Timer Clock Select

Regardless of the conversion clock speed, the internal clock runs nominally at 8.2 MHz. The conversion time of the TLV320AIC3212 depends on several functions. While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles are needed for proper sampling of the signal. Conversion time can vary, depending on the mode in which the TLV320AIC3212 is used. Throughout this document, internal and conversion clock cycles are used to describe the times that many functions take to execute. Considering the total system design, these times must be taken into account by the user.

The ADC uses either the internal MCLK1 signal or the internal oscillator for the SAR conversions.

2.12.1.2 Data Available - INT1 or INT2 Programmed as $\overline{\text{DATA\_AVA}}$

The interrupt signals INT1 & INT2 can be programmed by writing to B0_P0_R50_D[7:6] (INT1) or B0_P0_R50_D[5:4] (INT2). These pins function as the $\overline{\text{DATA\_AVA}}$ signal. To enable the SAR data available interrupt, B0_P3_R3_D[1:0] must be programmed to '01'. The $\overline{\text{DATA\_AVA}}$ signal and interrupts INT1 and INT2 can be mapped to GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, or DOUT2.

2.12.1.3 Temperature Measurement

In some applications, such as battery charging, a measurement of ambient temperature is required. The temperature measurement technique used in the TLV320AIC3212 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_j) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_j voltage and then monitoring the variation of that voltage as the temperature changes.

The TLV320AIC3212 offers two modes of temperature measurement. The first mode requires a single reading to predict the ambient temperature. A diode, as shown in Figure 2-77, is used during this measurement cycle. This voltage is typically 600 mV at 25°C with a 20-µA current through it. The absolute value of this diode voltage can vary a few millivolts. The temperature coefficient of this voltage is typically 2 mV/°C. During the final test of the end product, the diode voltage at a known room temperature is stored in nonvolatile memory. Further calibration can be done to calculate the precise temperature coefficient of the particular device. This method has a temperature resolution of approximately 0.4°C/LSB and accuracy of approximately ±3°C with two-temperature calibration. Figure 2-78 and Figure 2-79 show typical plots with single and two-temperature calibration, respectively.

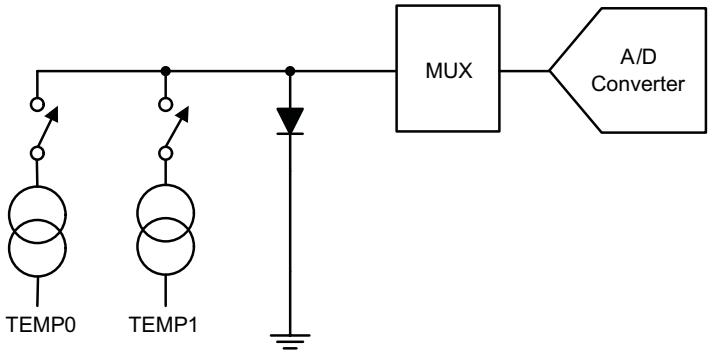


Figure 2-77. Functional Block Diagram of Temperature-Measurement Mode

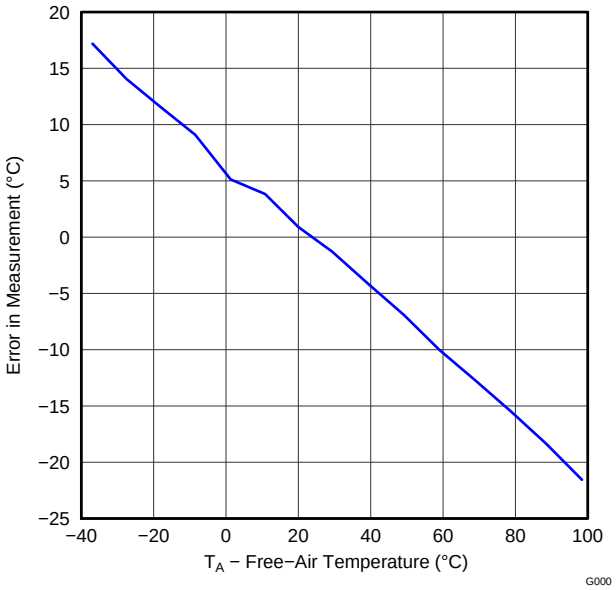


Figure 2-78. Typical Plot of Single-Measurement Method After Calibrating for Offset at Room Temperature

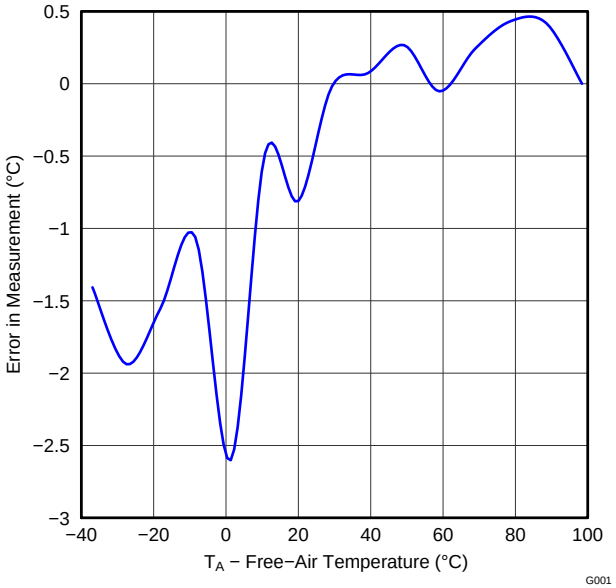


Figure 2-79. Typical Plot of Single-Measurement Method After Calibrating for Offset and Gain at Two Temperatures

The second mode uses a two-measurement (differential) method. This mode requires a second conversion with a current 82 times larger. The voltage difference between the first (TEMP1) and second (TEMP2) conversion, using 82 times the bias current, is represented by:

$$V_{(Temp1\ -\ Temp2)} = \frac{kT}{q} \times \ln(N) \tag{23}$$

where

N is the current ratio = 82
k = Boltzmann's constant (1.38054×10^{-23} electrons volts/Kelvin)
q = the electron charge (1.602189×10^{-19} C)
T = the temperature in Kelvins

The equation for the relation between differential code and temperature may vary slightly from device to device and can be calibrated at final system test by the user. This method provides resolution of approximately 2°C/LSB and accuracy of approximately ±6°C after calibrating at room temperature. A plot of typical calibration error for this method is shown in Figure 2-80.

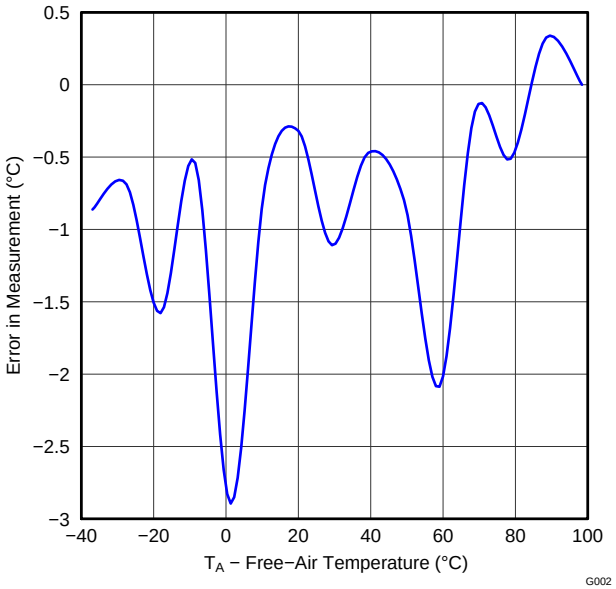


Figure 2-80. Typical Plot of Differential Measurement Method After Calibrating for Offset and Gain at Two Temperatures

The TLV320AIC3212 supports programmable auto-temperature measurement mode, which can be enabled by setting B0_P3_R19_D4. In this mode, the TLV320AIC3212 can auto-start the temperature measurement after a programmable interval. The user can program minimum and maximum threshold values through a register. In the case of temperature measurements, these thresholds are controlled in B0_P3_R30-R33. If the measurement goes outside the threshold range, the TLV320AIC3212 sets a flag in read-only B0_P3_R21, which is cleared after the flag is read. The TLV320AIC3212 can also be configured to send an active-high interrupt over INT1 or INT2 by setting bits in B0_P0_R50. The duration of the interrupt is approximately 2 ms, if B0_P0_R51_D[7:6] = '00' or B0_P0_R51_D[5:4] = '00', or these interrupt signals can be configured for alternate output signals. See Section 2.12.4 for more details on interrupt generation.

Temperature measurement can only be done in host-controlled mode.

2.12.1.4 Auxiliary Voltage Measurements

The auxiliary voltage inputs (IN1L/AUX1, IN1R/AUX2, and VBAT) are measured using the single-ended measurement method with SAR ADC.

For IN1L/AUX1 and IN1R/AUX2:
If the conversion results in an ADC output code of B, then the voltage at the input pins (IN1L/AUX1 and IN1R/AUX2) can be calculated as:

$$V_{PIN} = \frac{B}{2^N} \times VREF\_SAR \quad (24)$$

where:

N is the programmed resolution of the SAR ADC.

VREF_SAR is the applied external reference voltage.

For an example of a script for reading voltages on IN1L, see Section 4.8.1.

For VBAT:
The VBAT pin can be used for two different functions:

2.12.1.4.1 Auxiliary Battery-Voltage Measurement for VBAT

The TLV320AIC3212 can be used to measure battery voltage up to 6 V. This measurement can made using the VBAT pin, which has a voltage divider (divide by 5), as seen in Figure 2-75. This analog prescaler is available on the pin to allow higher voltages to be measured by the SAR ADC. This battery measurement function is supported in 8-bit, 10-bit, and 12-bit modes.

To enable the battery-voltage measurement mode, write a '0110' to B0_P3_R3_D[5:2].

Because the ADC code is 1/5 of the actual voltage value applied at VBAT, the correct value can be found by multiplying the ADC code by 5. For low voltages of VREF_SAR, this function can support voltages from 0 to (5 × VREF_SAR), where the upper voltage limit for VBAT is 6 V, and is also limited by the value listed in the *Absolute Maximum Ratings* table in the TLV320AIC3212 data sheet.

In the battery-voltage measurement mode, the conversion results in an ADC output code of B, where the voltage at the input pin (VBAT) can be calculated as:

$$V_{BAT} = \frac{B}{2^N} \times (5 \times VREF\_SAR) \quad (25)$$

where:

N is the programmed resolution of the SAR ADC.

VREF_SAR is the applied external reference voltage.

For an example of a script for battery voltages on VBAT, see .

2.12.1.4.2 Auxiliary Input (Normal Mode) for VBAT

The default functionality for the VBAT input is similar to IN1L/AUX1 and IN1R/AUX2. The useful measurement range is 0 V to VREF_SAR, and the maximum voltage input should be limited to 1.95 V. Because VBAT has an internal resistor divider, the internal ADC code is scaled down; however, in the normal mode, it is internally scaled back up in the digital domain, so that the normal transfer function can be realized using the SAR ADC. Although this mode is supported in 8-bit, 10-bit, and 12-bit modes, the 8-bit mode does not show any missing codes, whereas the 10-bit and 12-bit mode can have one missing code due to the analog input scaling and digital output scaling. Therefore, it is recommended to always use 8-bit mode for VBAT.

$$V_{BAT} = \frac{B}{2^N} \times VREF\_SAR \quad (26)$$

where,

N is the programmed resolution of the SAR ADC.
VREF_SAR is the applied external reference voltage.

The auxiliary input can be monitored continuously in scan mode.

2.12.1.5 Port Scan

If making voltage measurements on the inputs IN1L/AUX1, IN1R/AUX2, and VBAT is desired on a periodic basis, then the port-scan mode can be used. This mode causes the TLV320AIC3212 to sample and convert each of the auxiliary inputs. At the end of this cycle, all of the auxiliary result registers contain the updated values. Thus, with one write to the TLV320AIC3212, the host can cause three different measurements to be made. Port scan can be set up by writing to B0_P3_R3_D[5:2].

Port scan can only be used in host-controlled mode.

See *Conversion Time Calculations for the TLV320AIC3212*, Section 2.12.1.8, and *Port-Scan Operation*, Section 2.12.1.8.3, for conversion-time calculations and timing diagrams.

2.12.1.6 Buffer Mode

The TLV320AIC3212 supports a programmable buffer mode for all conversions (VBAT, IN1L/AUX1, IN1R/AUX2, TEMP1, TEMP2). Buffer mode is implemented using a circular FIFO with a depth of 64. The number of interrupts required to be serviced by a host processor can be reduced significantly in buffer mode. Buffer mode can be enabled using B0_P3_R13_D7.

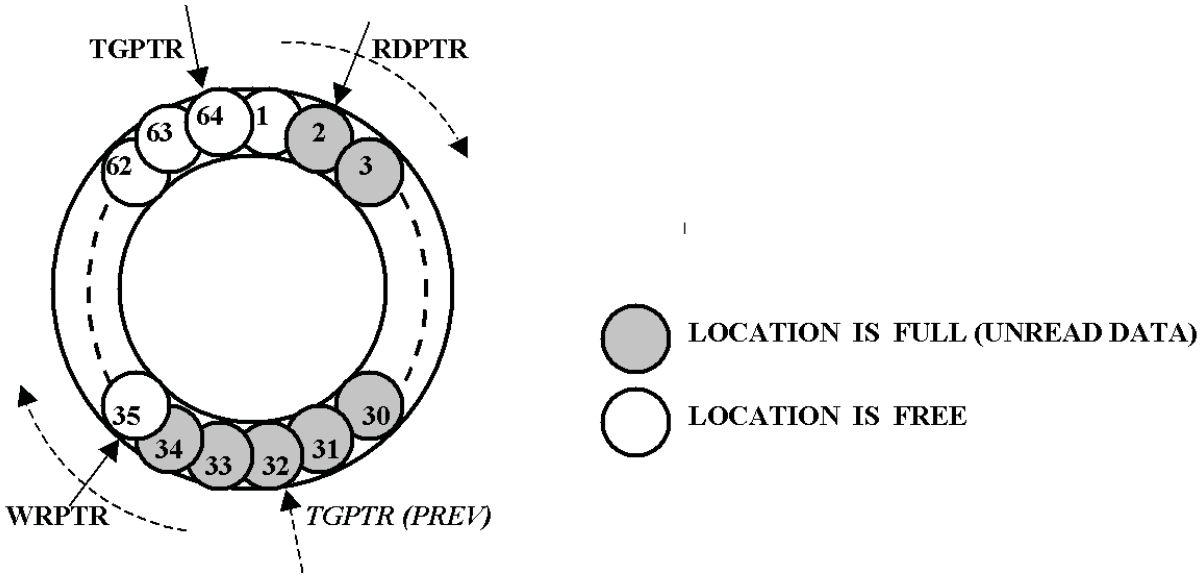


Figure 2-81. Circular Buffer

Converted data is automatically written into the FIFO. To control the writing, reading and interrupt process, a write pointer (WRPTR), a read pointer (RDPTR), and a trigger pointer (TGPTR) are used. The read pointer always shows the location that is read next. The write pointer indicates the location in which the next converted data is to be written. The trigger pointer indicates the location at which an interrupt is generated if the write pointer reaches that location. Trigger level is the number of the data values needed to be present in the FIFO before generating an interrupt. Figure 2-81 shows the case when the trigger level is programmed as 32. On resetting the buffer mode, RDPTR moves to location 1, WRPTR moves to location 1, and TGPTR moves to a location equal to the programmed trigger level.

The user can select the input or input sequence to be converted by writing to B0_P3_R3_D[5:2]. The converted values are written in a predefined sequence to the circular buffer. The user has flexibility to program a specific trigger level in order to choose the configuration which best fits the application. When the number of converted data values written in FIFO becomes equal to the programmed trigger level, then the device generates an interrupt signal on INT1 or INT2. In buffer mode, the user should program this pin as Data Available. In buffer mode, conversions (VBAT, IN1L/AUX1, IN1R/AUX2, TEMP1, TEMP2) are allowed only in host-controlled mode.

Buffer mode can be used in single-shot conversion or continuous-conversion mode.

In single-shot conversion mode, once the number of data values written reaches the programmed trigger level, the TLV320AIC3212 generates an interrupt and waits for the user to start reading. As soon as the user starts reading the first data value from the last converted set, the TLV320AIC3212 clears the interrupt and starts a new set of conversions, and the trigger pointer is incremented by the programmed trigger level. An interrupt is generated again when the trigger condition is satisfied.

In continuous-conversion mode, once the number of data values written reaches the programmed trigger level, the TLV320AIC3212 generates an interrupt. It immediately starts a new set of conversions, and the trigger pointer is incremented by the programmed trigger level. An interrupt is cleared either by writing the next converted data value into the FIFO or by starting to read from the FIFO.

Depending on how the user is reading data, the FIFO can become empty or full. If the user is trying to read data even if the FIFO is empty, then RDPTR keeps pointing to same location. If the FIFO becomes full, then the next location is overwritten with newly converted data values, and the read pointer is incremented by one.

While reading the FIFO, the TLV320AIC3212 provides FIFO-empty and -full status flags along with the data. The user can also read a status flag from B0_P3_R13_D[1:0]. See Table 2-45 for buffer-mode control and Table 2-46 for buffer-mode 16-bit read-data format.

Table 2-45. SAR/Buffer Mode Data Read Control (B0_P3_R18_D[7:5])[(1)]

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: SPI interface is used for SAR/buffer data reading. 1: I²C interface is used for SAR/buffer data reading.
D6	R/W	0	0: SAR/buffer data update is automatically halted (to avoid simultaneous buffer read and write operations) based on internal detection logic. Valid only for SPI interface. 1: SAR/buffer data update is held using software control (B0_P3_R18_D5).
D5	R/W	0	0: SAR/buffer data update is enabled all the time (valid only if B0_P3_R18_D6 = 1). 1: SAR/buffer data update is stopped so that user can read the last updated data without any data corruption (valid only if B0_P3_R18_D6 = 1).

(1) To enable buffer mode, write a 1 to B0_P3_R13_D7.

Table 2-46. Buffer Mode 16-Bit Read Data Format (B0_P252_R1 and B0_P252_R2)

BUFFER READ DATA BIT	NAME	RESET VALUE	DESCRIPTION	COMMENT
D15	FUF	0	Buffer-Full flag - This flag indicates that all the 64 locations of the buffer contain unread data.	B0_P252_R1_D7
D14	EMF	1	Buffer-Empty flag - This flag indicates that there is no un-read data available in FIFO. This is generated while reading the last converted data.	B0_P252_R1_D6
D13		X	Reserved	B0_P252_R1_D5
D12	ID	X	Data identification: 0 = VBAT or IN1R/AUX2 data in R11-R0 1= IN1L/AUX1 or TEMP data in R11-R0 Order for writing data in buffer when multiple inputs are selected: For autoscan conversion: IN1L/AUX1 (if selected), IN1R/AUX2 (if selected), VBAT, TEMP1 or TEMP2 (if selected) For port-scan conversion: IN1L/AUX1, IN1R/AUX2, VBAT	B0_P252_R1_D4
D11-D8	R11-R8	X	Converted data (MSB, 4 bits)	B0_P252_R1_D[3:0]
D7-D0	R7-R0	X	Converted data (LSB, 8 bits)	B0_P252_R2_D[7:0]

2.12.1.6.1 Buffer Mode Access through I²C for TLV320AIC3212

To enable faster data access, SPI protocol is preferred, but if I²C is required, note the following.

- In continuous buffer mode:
  - Only one measurement type, i.e. choice of IN1L, IN1R, VBAT, TEMP1 or TEMP2, can be used.
- In single-shot mode:
  - Multiple measurement types can be stored in the buffer consecutively.
  - The I²C read must completely empty the buffer. In other words, the number of bytes read must be equal to the trigger-level multiplied by 2 (for 2 bytes per converted data). If the buffer is empty, this will be reflected by bit B0_P252_R1_D6=1 in the last measurement read.
  - The I²C read must empty the buffer in a single call. Note that some I²C drivers may break auto-increment instructions into multiple, smaller calls. This can cause the SAR buffer to return invalid data, so the SAR trigger level must be less than or equal to the max I²C auto-increment size divided by 2.
- If 64 elements (128 bytes) are read, the last byte will be invalid data since I²C allows a max of 127 bytes.

2.12.1.7 Reading AUX Data in Non-Buffer Mode From SPI

Reading from the TLV320AIC3212 is done by using the protocol called out in Figure 2-82.

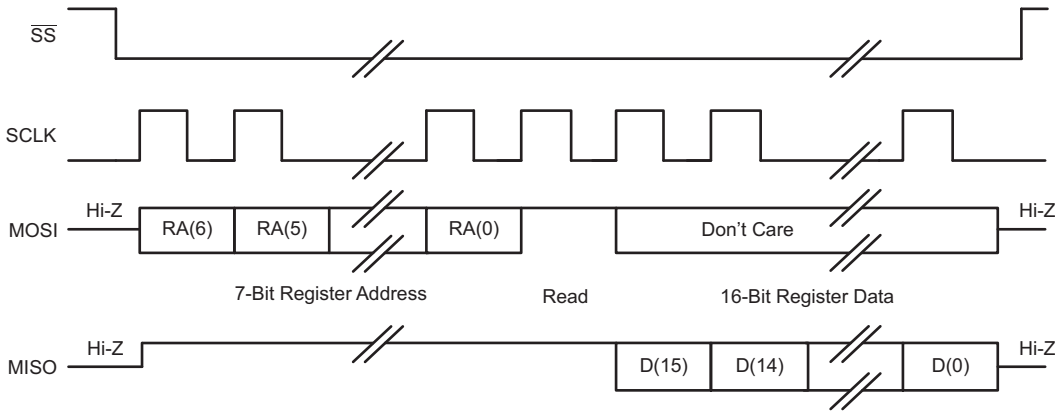


Figure 2-82. 16-Bit Data-Read Timing, 24 Clocks per 16-Bit Data Read, 8-Bit Bus Interface

This protocol uses a 24-clock sequence to get a 16-bit data read. Set the INT1 or INT2 interrupt for monitoring the data-available status by writing '01' to B0_P3_R3_D[1:0]. Reading is normally done when the interrupt is low (data is available for reading). Status from the ADC conversion can be read from B0_P3_R9. If bit D6 is 0, then the ADC is actively converting, so a BUSY status is read. If bit D5 is set, then some data is now available for reading. Next, reading from a status register on B0_P3_R10 lets us know if data is available for IN1L/AUX1, IN1R/AUX2, or VBAT. If bit D7 is set, then IN1L/AUX1 data can be read. If bit D6 is set, then IN1R/AUX2 data can be read. If bit D5 is set, then VBAT data can be read.

The first 7 bits in the read sequence are for the first register address of the two sequential 8-bit registers. The next bit is high, which specifies that a read operation follows; then the 16 remaining clocks are used to get the 16-bit data that is read out in the order of D15–D0. The register address specified in the first seven clocks of the 24-clock sequence reads out as bits D15–D8, where D15 is the MSB of the byte, then the register number is incremented by 1 and the data is read from D7–D0, where D7 is the MSB of that byte. (For reading data for IN1L/AUX1, use B0_P3_R54 and B0_P3_R55; for reading data for IN1R/AUX2, use B0_P3_R56 and B0_P3_R57; and for reading data for VBAT, use B0_P3_R58 and B0_P3_R59.) From this cycle, the first 16-bit data word has been read. This sequence can be repeated to read further values of IN1L/AUX1, IN1R/AUX2, and VBAT data.

2.12.1.8 Conversion Time Calculations for the TLV320AIC3212

This section discusses conversion time calculations for temperature, auxiliary, and battery measurements for TLV320AIC3212.

The timing signals can be programmed by B0_P3_R3. INT1 or INT2 can be programmed as $\overline{\text{DATA\_AVA}}$ by programming B0_P0_R50_D[7:4]. $\overline{\text{DATA\_AVA}}$ can also be sent to GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, or DOUT2.

2.12.1.8.1 Host-Controlled VBAT Scan Mode

The time needed to make temperature, auxiliary, or battery measurements is given by:

$$t = N_{AVG} \times (N_{BITS} + 1) \times t_{CONV} + N_{AVG} \times (n_1 + n_2) \times t_{CLK} + 17 \times t_{CLK} + n_3 \times t_{CLK}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) The programmable delay t_{REF} scales accordingly based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

where :

DIV1 = Divider setting configured in B0_P3_R2_D4:3
NBITS = SAR ADC resolution configured in B0_P3_R2_D[6:5]; or 12 if VBAT is used as normal AUX input by setting page B0_P3_R6_D0 = 0
n1 = 6 if DIV1 = 1; otherwise, n1 = 7

n2 = 24 if measurement is for TEMP1; or 13 if measurement is other than TEMP1; or 400 if measurement is for the external/internal resistance using B0_P3_R19_D[2:1] for IN1L/AUX1 and IN1R/AUX2
n3 = 0 if external reference mode is selected; or 3 if t_{REF} = 0 ms or internal reference is powered up all the time; or 1 + t_{REF}/t_{CLK} if t_{REF} is not equal to 0 ms and internal reference must power down between conversions
t_{REF} = Internal reference stablization time as configured in B0_P3_R6_D[3:2].

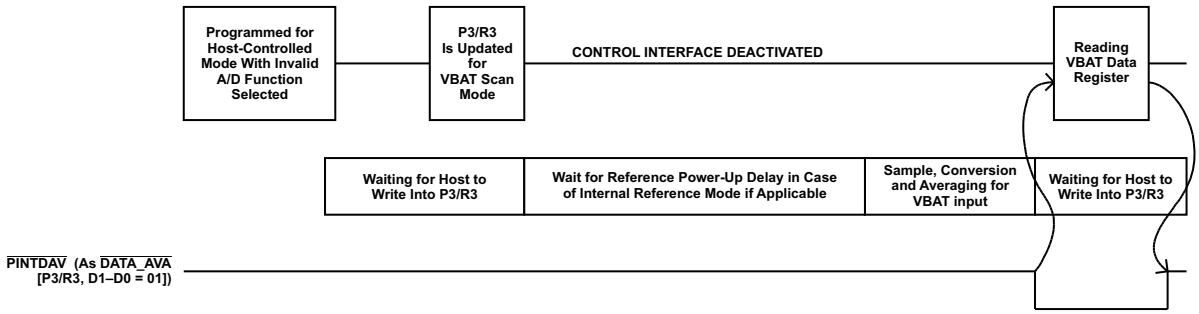


Figure 2-83. Host-Controlled VBAT Scan Mode

2.12.1.8.2 Host-Controlled Continuous Aux Scan Mode

The time needed for continuous autoscan mode is given by:

$$t = N_{INP} \times N_{AVG} \times (N_{BITS} + 1) \times t_{CONV} + N_{INP} \times N_{AVG} \times (n_1 + 13) \times t_{CLK} + N_{AVG} \times n_2 \times t_{CLK} + N_{INP} \times 9 \times t_{CLK} + (n_3 + n4) \times t_{CLK} + t_{DEL}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) This equation is valid only from the second conversion onward.

(3) All the programmable delays, t_{DEL} and t_{REF}, scale accordingly based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

where:

DIV1 = Divider setting configured in B0_P3_R2_D[4:3]
N_{BITS} = SAR ADC resolution configured in B0_P3_R2_D[6:5]
N_{INP} = 1 to 4, based on the number of inputs enabled for autoscan by using B0_P3_R19
n1 = 6 if DIV1 = 1; otherwise, n1 = 7
n2 = 11 if one of the inputs selected is TEMP1; otherwise, n2 = 0
n3 = 0 if external reference mode is selected or
t_{DEL} = 0; or 3 if t_{REF} = 0 ms or internal reference is powered up all the time; or 1 + t_{REF}/t_{CLK} if t_{REF} is not equal to 0 ms and internal reference must power down between conversions.
n4 = 0 if t_{DEL} = 0; otherwise, n4 = 7
t_{DEL} = Delay-time setting as configured in B0_P3_R15_D[2:0]; or 0 if B0_P3_R15_D3 = 0
t_{REF} = Internal reference stablization time as configured in B0_P3_R6_D[3:2].

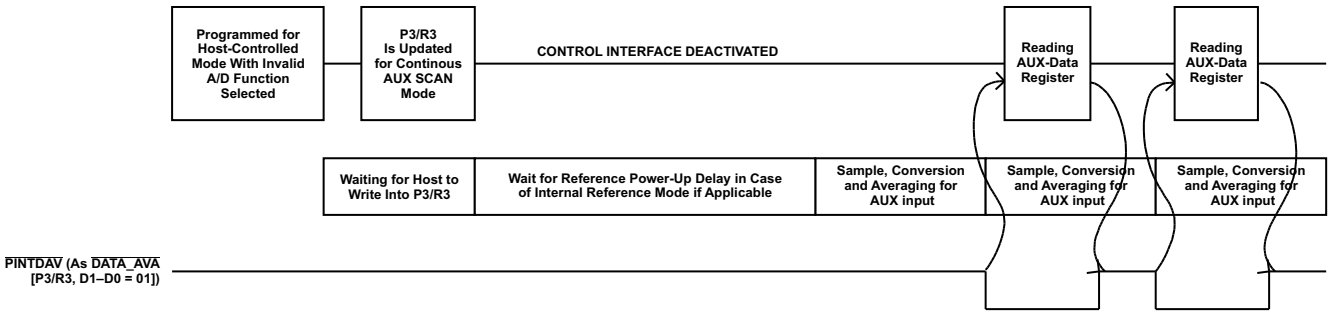


Figure 2-84. Host-Controlled Continuous Aux Scan Mode

2.12.1.8.3 Port-Scan Operation

The time needed to complete one set of port-scan conversions is given by:

$$t = 3 \times N_{AVG} \times (N_{BITS} + 1) \times t_{CONV} + 3 \times N_{AVG} \times (n_1 + 13) \times t_{CLK} + 35 \times t_{CLK} + n_2 \times t_{CLK}$$

(1) This equation is valid if B0_P3_R18_D[6:5] = 00, which means SAR data update is not kept on hold for reading converted data.

(2) The programmable delay t_{REF} scales based on the actual divider setting and time period of the clock used to generate this. See the respective control register settings to understand the scale factors.

where:

DIV1 = Divider setting as configured in B0_P3_R2_D[4:3]
N_{BITS} = SAR ADC resolution as configured in B0_P3_R2_D[6:5]
n1 = 6 if DIV1 = 1; otherwise, n1 = 7
n2 = 0 if external reference mode is selected; or 3 if t_{REF} = 0 ms or internal reference is powered up all the time; or 1 + t_{REF}/t_{CLK} if t_{REF} is not equal to 0 ms and internal reference must power down between conversions
t_{REF} = Internal reference stablization time as configured in B0_P3_R6_D[3:2].

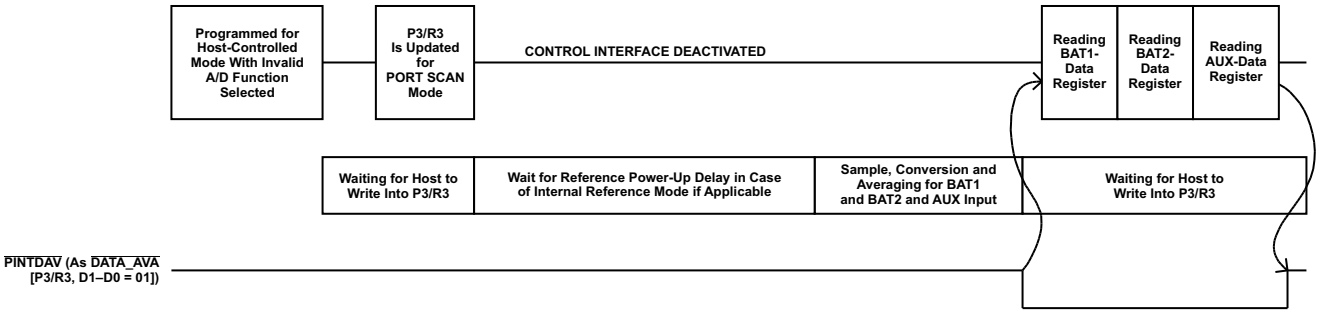


Figure 2-85. Host-Controlled Port Scan Mode

2.12.2 Headset Detection

The TLV320AIC3212 includes extensive capability to monitor a headphone, microphone, or headset jack to determine if a plug has been inserted into the jack, and then determine what type of headset/headphone is wired to the plug. The device also includes the capability to detect a button press for actions such as starting a call with headset button press. The figures below show the circuit configuration to enable this feature for stereo headphones and stereo headset with microphone and button, as well as mono headset with and without microphone. It is recommended to use IN1L or IN1R for external headset microphones.

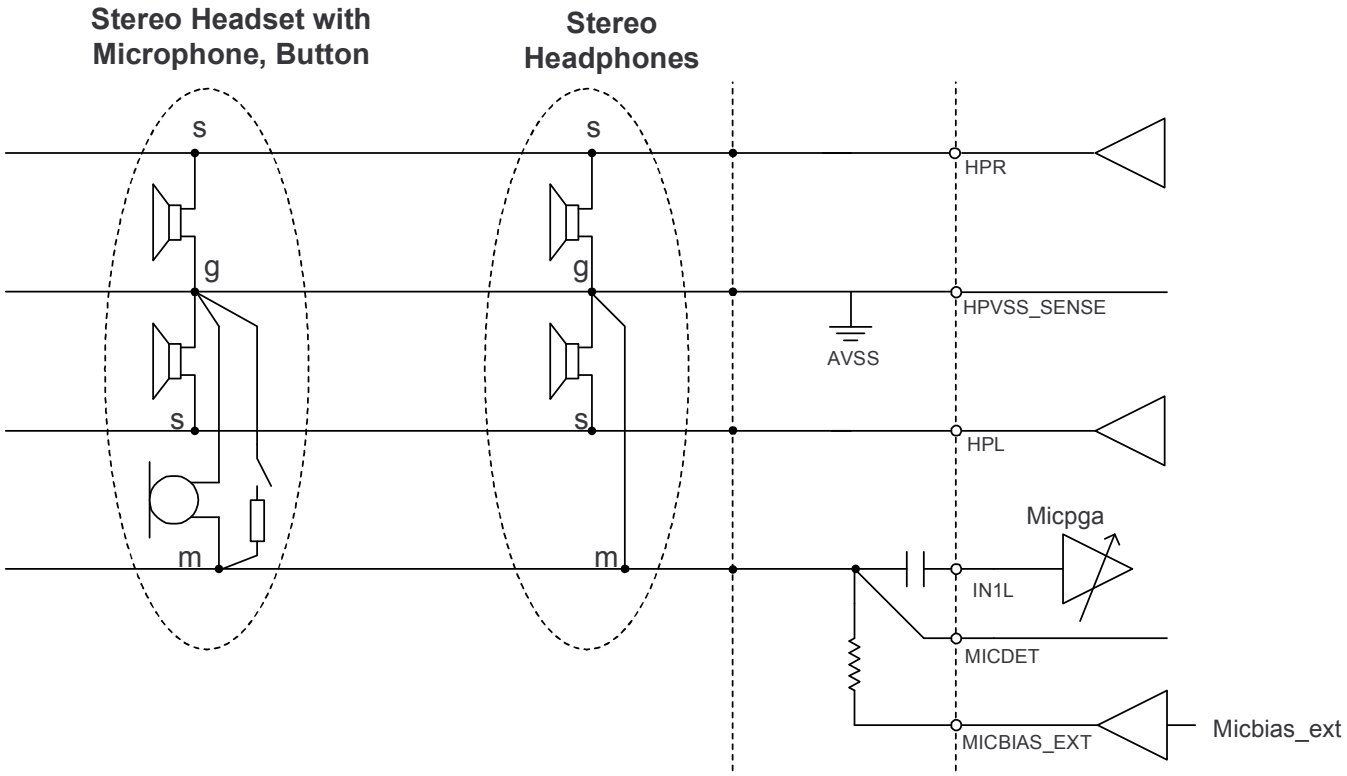


Figure 2-86. Jack Connections for Detection of Stereo Headsets

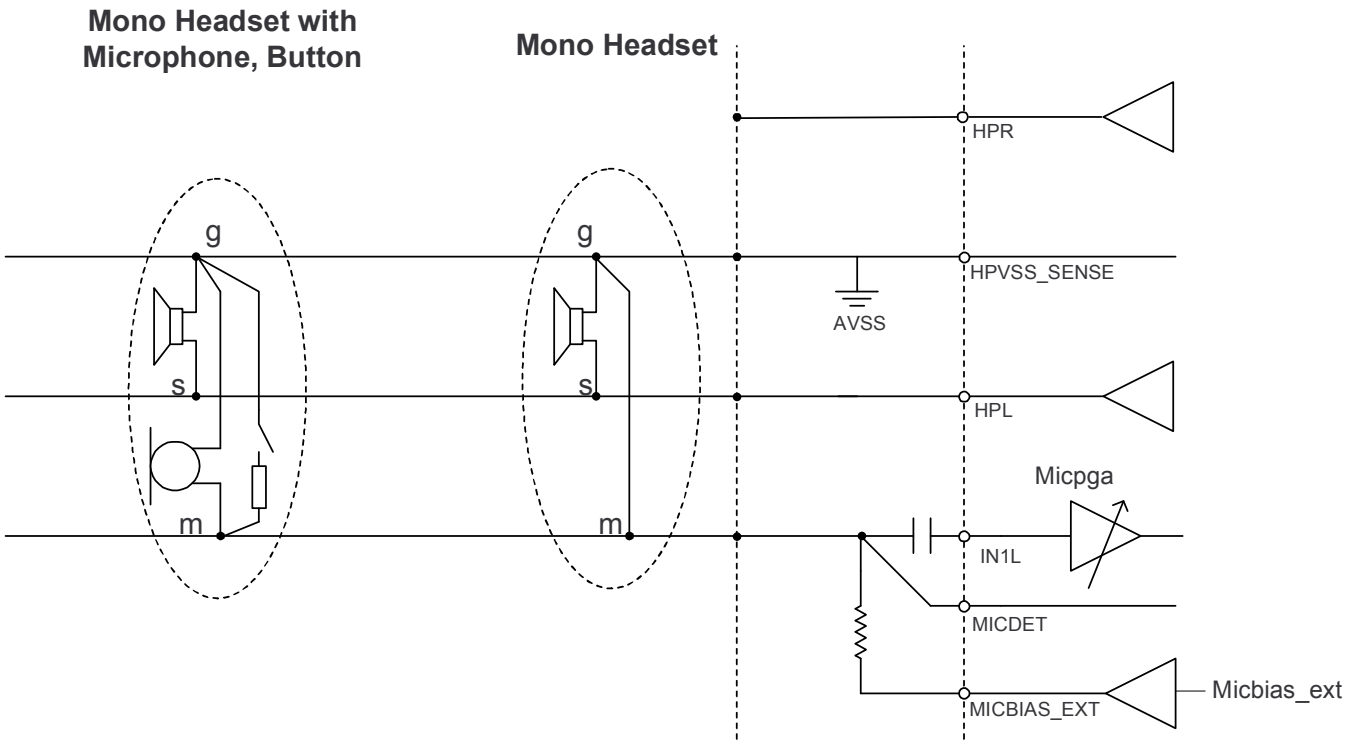


Figure 2-87. Jack Connections for Detection of Mono Headsets

This feature is enabled by programming B0_P0_R67_D7. In order to avoid false detections due to mechanical vibrations in headset jacks or microphone buttons, a debounce function is provided for glitch rejection. For the case of headset insertion/removal, a debounce function with a range of 16ms - 512ms is provided. This can be programmed via B0_P0_R67_D[4:2]. For improved button-press detection, the debounce function has a range of 8ms to 32ms by programming B0_P0_R67_D[1:0].

The TLV320AIC3212 also provides feedback to user when a button press, or a headset insertion/removal event is detected through register readable flags as well as an interrupt on the IO pins. The value in B0_P0_R46_D[5:4] provides the instantaneous state of button press and headset insertion. B0_P0_R44_D5 is a sticky (latched) flag that is set when the button-press event is detected. B0_P0_R44_D4 is a sticky flag that is set when the headset insertion or removal event is detected. These sticky flags are set by the event occurrence, and are reset only when read. This requires polling B0_P0_R44. To avoid polling and the associated overhead, the TLV320AIC3212 also provides an interrupt feature where the events can trigger the INT1 and/or INT2 interrupts. These interrupt events can be routed to one of the digital output pins. Please see Section 2.12.4 for details on interrupts (INT1 and INT2) and Section 2.12.4 for details on digital pin routing.

As shown in Figure 2-86 and Figure 2-87, the TLV320AIC3212 not only detects a headset insertion event, but also distinguishes between the different headsets inserted, such as stereo headphones, stereo cellular headsets with microphone, mono headsets with microphone, and mono headset without microphone. After the headset-detection event, the user can read B0_P0_R37_D[5:4] and B0_P0_R37_D[1:0] to determine the type of headset inserted.

Table 2-47. Headset Detection Types

Headset Type	Microphone Detection	Headset Detection
Stereo Headphones without Microphone	B0_P0_R37_D[5:4] = 01	B0_P0_R37_D[1:0] = 10
Stereo Headset with Microphone	B0_P0_R37_D[5:4] = 11	B0_P0_R37_D[1:0] = 10
Mono Headset without Microphone	B0_P0_R37_D[5:4] = 01	B0_P0_R37_D[1:0] = 01
Mono Headset with Microphone	B0_P0_R37_D[5:4] = 11	B0_P0_R37_D[1:0] = 01

For proper detection of these different types, it is important to follow the guidelines in Table 2-48

Table 2-48. Detection Specifications for Microphone, Button, Headset

Parameter	Minimum	Typical	Maximum	Unit
Headphone load resistance	16		300	Ω
Key switch resistance (includes all jack-to-plug contact resistances)			2	Ω
Effective capacitance between MICDET and ground			150	pF
Microphone effective resistance	0.8		8	kΩ
Micbias_ext resistor for microphone detection	2.09	2.2	2.31	kΩ

Table 2-49. Headset Detection Block Registers

Register	Description
B0_P0_R67_D7	Headset Detection Enable/Disable
B0_P0_R67_D[4:2]	Debounce Programmability for Headset Detection
B0_P0_R67_D[1:0]	Debounce Programmability for Button Press
B0_P0_R44_D5	Sticky Flag for Button Press Event
B0_P0_R44_D4	Sticky Flag for Headset Insertion or Removal Event
B0_P0_R46_D5	Status Flag for Button Press Event
B0_P0_R46_D4	Status Flag for Headset Insertion and Removal

Table 2-49. Headset Detection Block Registers (continued)

Register	Description
B0_P0_R37_D[5:4] and B0_P0_R37_D[1:0]	Flags for type of Headset Detected
B0_P1_R119 and B0_P1_R120	Headset Detection Tuning Registers

The headset detection block requires AVDDx_18 and AVDD3_33 to be powered. In addition, the weak connection of AVDD to DVDD should be disabled (B0_P1_R1_D3="0"), and External Analog Supplies should be enabled (B0_P1_R1_D2="0"). The headset detection feature in the TLV320AIC3212 is achieved with a very low power overhead, requiring less than 30µA of additional current from AVDDx supplies.

2.12.3 Interrupt Generation

The TLV320AIC3212 an trigger interrupts to the host processor for events that require host processor intervention. This avoids polling the status-flag registers continuously. The TLV320AIC3212 has two defined interrupts; INT1 and INT2 that can be configured by programming Page 0, Register 48 and 49. A user can configure the interrupts INT1 and INT2 to be triggered by one or many events such as

- Headset Detection
- Button Press
- DAC DRC Signal Exceeding Threshold
- Noise Detected by AGC
- Over-current Condition in Headphones
- Data Overflow in ADC and DAC Processing Blocks and Filters
- Over-temperature Condition in Speaker Drivers
- DC Measurement Data Available
- SAR ADC Data Available or Exceeding Threshold

Each of these INT1 and INT2 interrupts can be routed to output pins like GPIO1, GPIO2, GPO1, DOUT1, WCLK2, BCLK2, and DOUT2 by configuring B0_P4_R67-R96. Table 2-50 displays how to individually configure the INT1 or INT2 interrupts.

Table 2-50. Register Settings for Interrupt Routing

Pin	INT1	INT2
GPIO1	B0_P4_R86_D[5:2] = 0101	B0_P4_R86_D[5:2] = 0110
GPIO2	B0_P4_R87_D[5:2] = 0101	B0_P4_R87_D[5:2] = 0110
GPO1	B0_P4_R96_D[5:2] = 0100	B0_P4_R96_D[5:2] = 0101
DOUT1	B0_P4_R67_D[4:1] = 0100	B0_P4_R67_D[4:1] = 0101
WCLK2	B0_P4_R69_D[5:2] = 0101	B0_P4_R69_D[5:2] = 0110
BCLK2	B0_P4_R70_D[5:2] = 0101	B0_P4_R70_D[5:2] = 0101
DOUT2	B0_P4_R71_D[4:1] = 0100	B0_P4_R71_D[4:1] = 0101

These interrupt signals can either be configured as a single pulse, a series of pulses, or a change in output level by programming B0_P0_R51_D[7:6] and B0_P0_R51_D[5:4]. If the user configures the interrupts as a series of pulses, the events will trigger the start of pulses that will stop when the flag registers in B0_P0_R42, B0_P0_R44, B0_P0_R45 are read by the user to determine the cause of the interrupt. Similarly, if the user configures the interrupts as an active-high, level-based interrupt generated from these sticky flags, the interrupt port will reset low when the flag registers in B0_P0_R42, B0_P0_R44, B0_P0_R45 are read by the user.

2.12.4 Flexible Pin Muxing

The TLV320AIC3212 contains 25 digital pins. Besides the two fixed-function pins ($\overline{\text{RESET}}$ pin and SPI_SELECT pin), the remaining 23 digital pins can be configured for a wide variety of applications and systems, with different allocation possible between Control Pins, Clocking Pins, General Input/Output/Interrupts, and Audio Signal Flow. The TLV320AIC3212 provides a high level of flexibility in using digital pins for various functions, including I2C or SPI control, clocking inputs and outputs, general purpose inputs and outputs, digital microphone clocking and data, and digital audio data and clocking. For all possible digital pin muxing, see the pin muxing tables in Table 2-2 and Table 2-3 (located in Section 2.2.3). For all register settings associated with all these possible digital pin muxing, see the tables in Section 2.2.3.1. The following subsections highlight a few possible system setups.

2.12.4.1 Portable System with Three Audio Serial Interface Connections

Figure 2-88 displays a typical system for a portable media device (e.g. smartphone, tablet) with three audio serial interface connections. Depending on the connections desired for audio sinks/sources, the TLV320AIC3212 can provide a single audio codec solution across multiple end devices with different connectivity requirements.

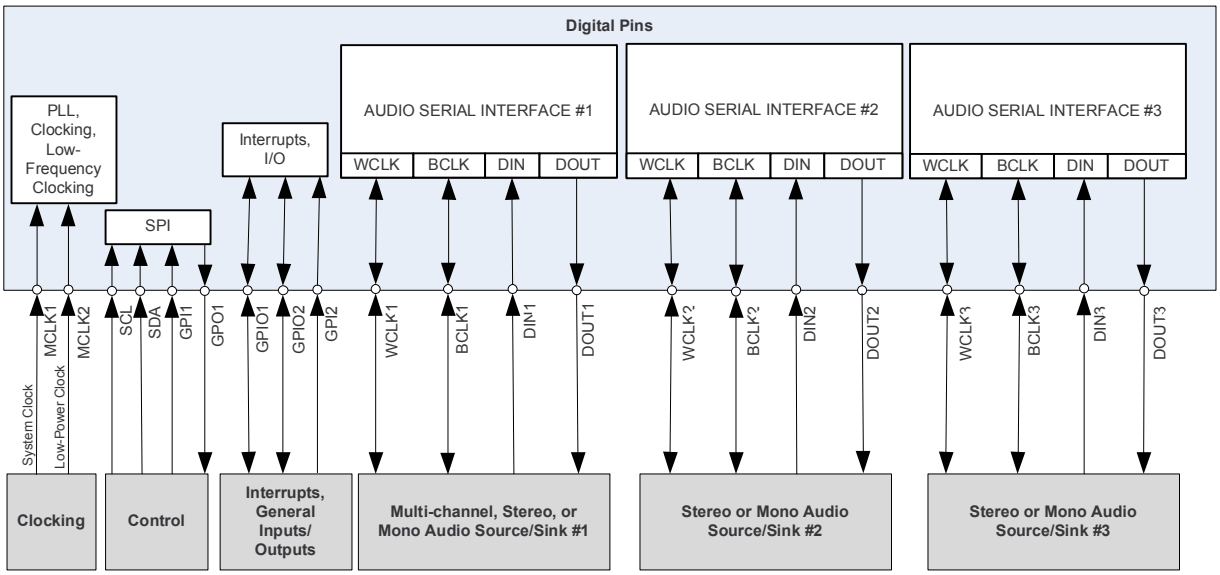


Figure 2-88. Digital Pin Connections - Example #1 (3 ASI connections)

Typically in a smartphone or tablet design, the Application Processor provides the clocking. The TLV320AIC3212 provides two input clock pins (MCLK1 and MCLK2), and in a typical system, MCLK1 would be utilized for the system master clock, and MCLK2 could be used for a low-frequency clock to support a low-power mode. If a low-power clock is not needed on MCLK2, this pin could be reconfigured to receive other clocks, audio data, or even digital microphone data. For the Control Domain, the Application Processor typically controls the audio codec. Figure 2-88 shows an SPI connection, but if the user needs additional digital pins for other functions and prefers I2C control, the GPI1 and GPO1 pins can be configured for other functions (e.g. interrupts, clocking, digital microphones). Interrupts and General Inputs/Outputs typically connect to the Application Processor also.

For the Audio Serial Interfaces, it is important to note that all these interfaces have similar functionality. It is typical in smartphones, tablets, and other portable devices for Audio Serial Interface #1 to connect to the Application Processor Audio Bus, or the dedicated App Processor Media Audio Bus (if it exists on the platform). As shown in Figure 2-88, this allows the App Processor to send monophonic or stereo music to the TLV320AIC3212. For smartphones or tablets, it is typical for Audio Source/Sink #2 and #3 to be Bluetooth or modem chipsets.Depending on the application, the TLV320AIC3212 can then select one of these interfaces to route to/from the DAC/ADC, or directly route Audio Serial Interfaces to each other.

In addition to the typical audio sinks/sources listed already, the three Audio Serial Interfaces on the TLV320AIC3212 could connect to a multitude of devices:

- S/PDIF Transceivers
- USB Audio Interface Devices
- Media Scalar Processors
- External ADCs for Additional Analog Inputs
- External DACs for Additional Analog Outputs
- Voice Processing Chips
- Digital Input Amplifiers
- Docking Connections

When selecting devices for connection to the Audio Serial Interfaces, it is important to check the IOVDD supply voltages to ensure they match the IOVDD voltage on the TLV320AIC3212.

2.12.4.2 Portable System with Two Four-Wire Audio Serial Interface Connections and One Six-Wire Audio Connection

This typical system can be augmented to include support for a Six-Wire Audio Serial Connection (see Section 2.9.2 for more details on Six-Wire Audio Interface Setup). In some systems, the communciation source/sink is separated into uplink and downlink paths, and Figure 2-89 shows that by simply using GPI3 and GPI4 for the uplink word clock and bit clock, the audio codec can perform similarly to System #1.

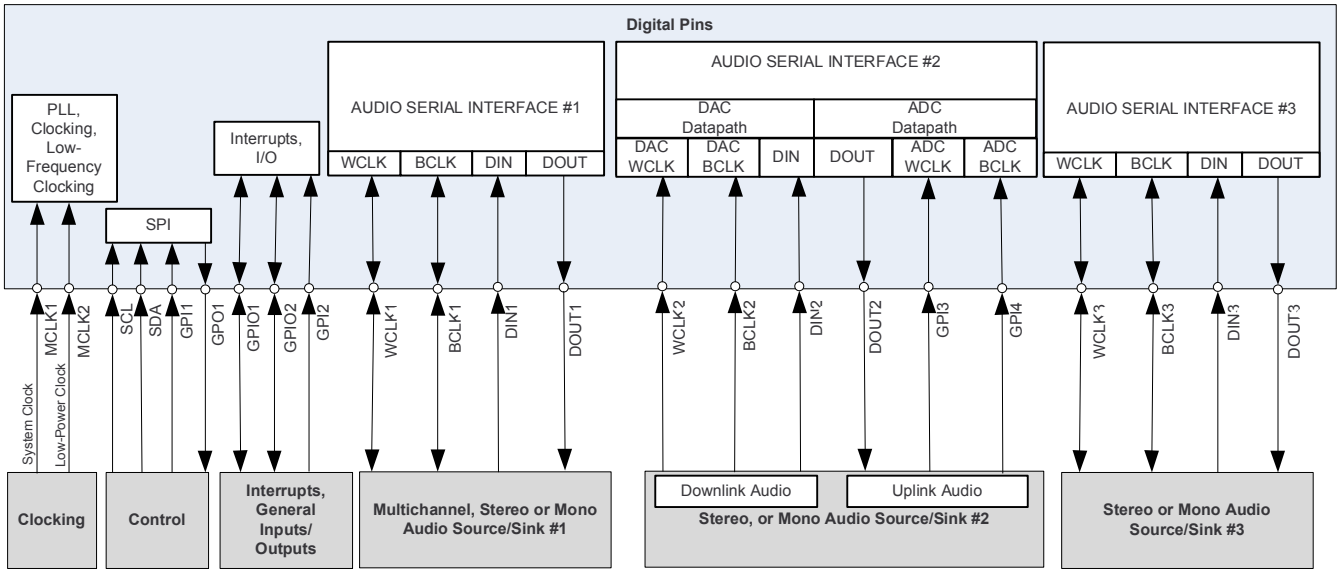


Figure 2-89. Digital Pin Connections - Example #2 (2 ASI connections + 1 Six-Wire ASI)

In this system, it is typical for Audio Source/Sink #1 to be an Application Processor Audio Bus or dedicated App Processor Media Bus. With the modem interface utilizing separate uplink and downlink clocks on Audio Source/Sink #2, it is straightforward to connect a Bluetooth chipset to Audio Serial Interface #3. However, any of the possible audio sources/sinks listed in the previous section could be utilized.

The two examples in this section do not show all the possible combinations of the highly-flexible digital pins of the TLV320AIC3212. In addition, if digital microphones are desired, this codec has many different pins from which to choose the digital microphone clock and data (i.e. choice from 7 different pins for digital microphone data and 6 different pins for digital microphone clock).

Please consult Table 2-2 and Table 2-3 (located in Section 2.2.3) for all possible digital pin muxing possibilities. For all register settings associated with all these possible digital pin muxing, see the tables in Section 2.2.3.1. In summary, the TLV320AIC3212 provides a high amount of flexibility to augment systems for new functionality over time.

Device Initialization

The requirements of the application circuit determine device setup details such as clock generation, power sources, references voltage,and special functions that may add value to the end application. Example device setups are described in the final section.

Topic **Page**

3.1 Power On Sequence **129**
3.2 Reset **132**
3.3 Device Startup Lockout Times **132**
3.4 Analog and Reference Startup **132**
3.5 PLL Startup **132**
3.6 Setting Device Common Mode Voltage **132**

3.1 Power On Sequence

There are two recommended power sequence possible for TLV320AIC3212:

1) Speaker Supplies, then Digital Supplies, then Analog Supplies

2) Speaker Supplies, then Digital and Analog Supplies

The first power on sequence is useful if the end system uses separate analog and digital supplies. This is useful to improve the efficiency of the digital rails by using a DC/DC converter, while keeping the analog supplies clean by using a low-dropout regulator(s) (LDO). While it is recommended to separate analog and digital supplies, if all the 1.8V supplies (analog and digital) must be tied together, the second power sequence can be utilized.

3.1.1 Power On Sequence 1 - Separate Digital and Analog Supplies

Figure 3-1 shows a timing diagram for the case where all supplies are provided separately. In such case, the depicted sequence should be used. The dashed lines marked in blue color refer to an internally supplied voltage.

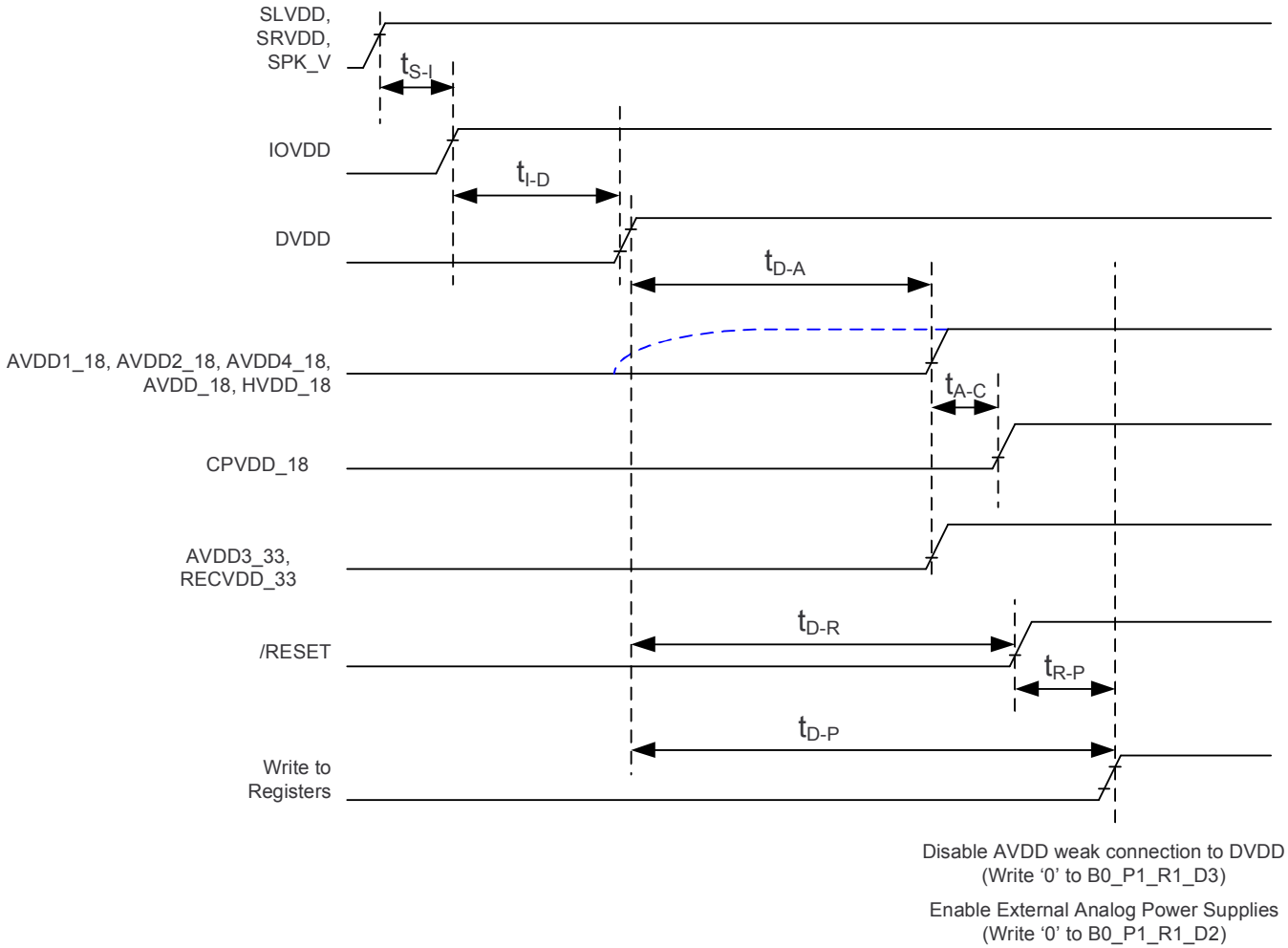


Figure 3-1. Analog Supplies provided after Digital Supplies

SLVDD, SRVDD, and SPK_V should be provided first. Next, IOVDD should be provided, and DVDD can be provided at the same time as IOVDD. Since, by default, DVDD is weakly connected to AVDD1_18 by a 10kohm resistor, AVDD*_18 and HVDD_18 (it is recommended to connect these five supplies together) will ramp up to the DVDD voltage once DVDD is provided at approximately $5*10k*C_{AVDD}$, where C_{AVDD} are the sum of the decoupling capacitors on the AVDD*_18 and HVDD_18 pins. For C_{AVDD} = 1uF, the charging

time is approximately 50ms. Parameter t_{D-A} allows analog supplies to be stable before analog supplies are provided. To prevent high currents from DVDD to the 1.8V and 3.3V analog supplies (i.e. AVDDx_18, HVDD_18, AVDD3_33, RECVDD_33), these analog supplies cannot be externally driven low by the external power source. This means that the external power source should be either high impedance or have a weak pull-down before being enabled.

Ensure that CPVDD_18 supply is provided either at same time as analog supplies or later. After /RESET is released (or a software reset is performed), no register writes should be performed within 1ms.

Table 3-1. Power Supply Timing Parameters

Parameter	Minimum	Typical	Maximum	Comments
t_{S-I}	0	0		Time between SLVDD/SRVDD/SPK_V is provided and IOVDD is provided.
t_{I-D}	0	0		Time between IOVDD is provided and DVDD is provided.
t_{D-A}	$5*10k*C_{AVDD}$	$5*10k*C_{AVDD}$		Time between DVDD is provided and the 1.8V and 3.3V analog supplies (AVDD*_18, HVDD_18, AVDD3_33, RECVDD_33) are provided. AVDDx_18 must be internally present before changing to external 1.8V analog supplies to prevent pop at headphone outputs.
t_{A-C}	0	0		Time between AVDD*_18 supplies are provided and CPVDD_18 is provided.
t_{D-R}	10ns	10ns		Time between DVDD (and IOVDD) is provided and reset can be released.
t_{D-P}	10ms	10ms		Time between DVDD (and IOVDD) is provided and when registers can be written to enable the external 1.8V analog supplies.
t_{R-P}	1ms	1ms		Time between release of the reset and when registers can be written (i.e. to enable the external 1.8V analog supplies).

3.1.2 Power On Sequence 2 - Shared 1.8V Analog Supplies

If desired, the analog supplies (AVDD1_18, AVDD2_18, AVDD4_18, AVDD_18 and HVDD_18) could also be externally supplied at the same time as DVDD. In this case, the weak pullup is not utilized. This is shown in the Figure 3-2.

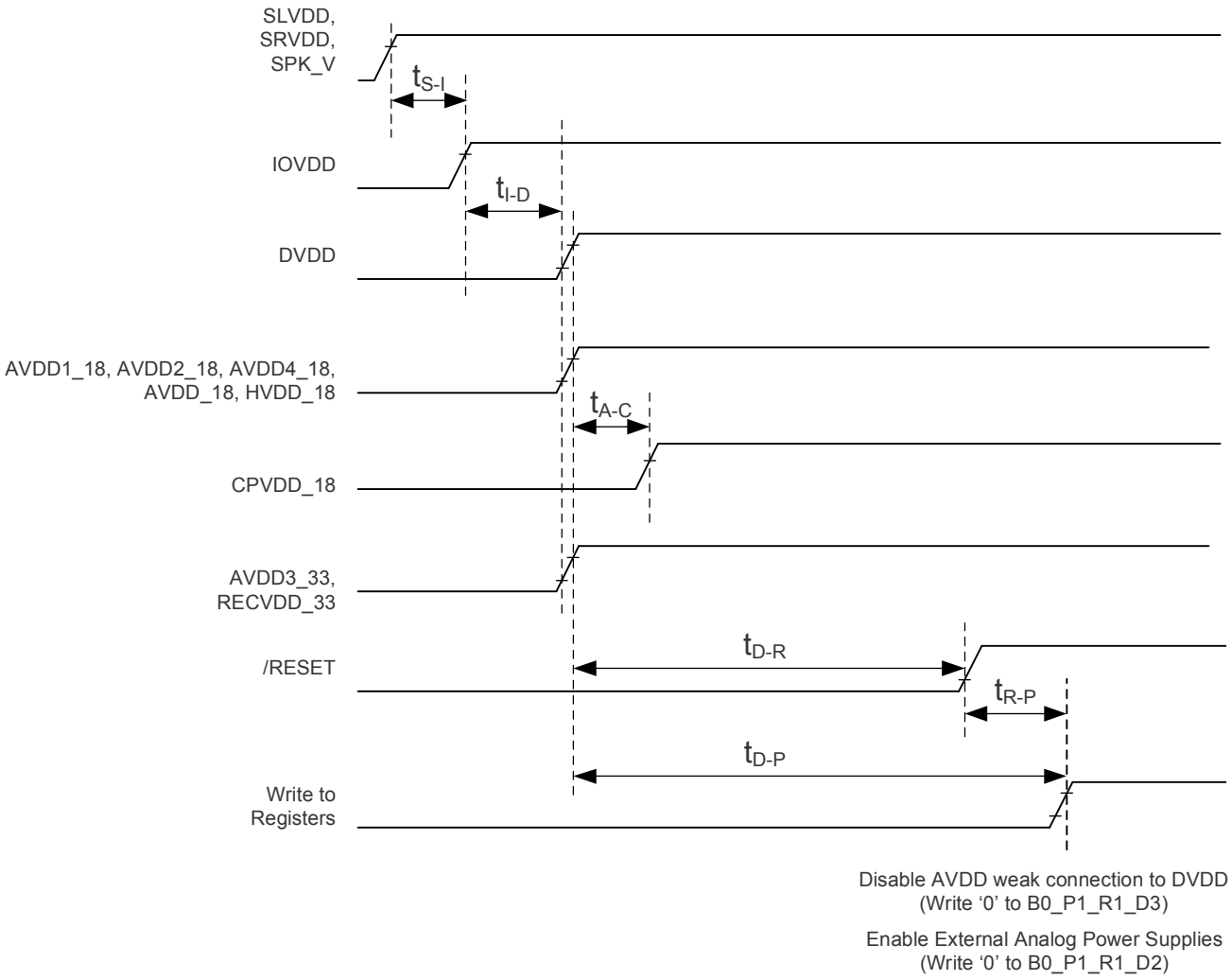


Figure 3-2. Digital and Analog 1.8V Supplies provided Together

After /RESET is released (or a software reset is performed), no register writes should be performed within 1ms.

Table 3-2. Power Supply Timing Parameters

Parameter	Minimum	Typical	Maximum	Comments
t_{S-I}	0	0		Time between SLVDD/SRVDD/SPK_V is provided and IOVDD is provided.
t_{I-D}	0	0		Time between IOVDD is provided and DVDD is provided.
t_{A-C}	0	0		Time between AVDD*_18 supplies are provided and CPVDD_18 is provided.
t_{D-R}	10ns	10ns		Time between DVDD (and IOVDD) is provided and reset can be released.
t_{D-P}	10ms	10ms		Time between DVDD (and IOVDD) is provided and when registers can be written to enable the external 1.8V analog supplies.
t_{R-P}	1ms	1ms		Time between release of the reset and when registers can be written (i.e. to enable the external 1.8V analog supplies).

3.2 Reset

The TLV320AIC3212 internal logic must be initialized to a known condition for proper device function. To initialize the device in its default operating condition, the hardware reset pin ($\overline{\text{RESET}}$) must be pulled low for at least 10ns. For this initialization to work, both the IOVDD and DVdd supplies must be powered up. It is recommended that while the DVdd supply is being powered up, the $\overline{\text{RESET}}$ pin be pulled low.

The device can also be reset via software reset. Writing '1' into B0_P0_R1_D0 resets the device. After a device reset, all registers are initialized with default values as listed in the Register Map section.

3.3 Device Startup Lockout Times

After the TLV320AIC3212 is initialized through hardware reset at power-up or software reset, the internal registers are initialized to default values. This initialization takes place within 1ms after pulling the $\overline{\text{RESET}}$ signal high. During this initialization phase, no register-read or register-write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

3.4 Analog and Reference Startup

The TLV320AIC3212 uses an external VREF_AUDIO pin for decoupling the reference voltage used for the data converters and other analog blocks. VREF_AUDIO pin requires a minimum 1uF decoupling capacitor from VREF_AUDIO to AVSSx. In order for any analog block to be powered up, the Analog Reference block must be powered up. By default, the Analog Reference block will implicitly be powered up whenever any analog block is powered up, or it can be powered up independently. Detailed descriptions of Analog Reference including fast power-up options are provided in . During the time that the reference block is not completely powered up, subsequent requests for powering up analog blocks (e.g., PLL) are queued, and executed after the reference power up is complete.

3.5 PLL Startup

Whenever the PLL is powered up, a startup delay of approx 10ms is involved after the power up command of the PLL and before the clocks are available to the codec. This delay is to ensure stable operation of PLL and clock-divider logic.

3.6 Setting Device Common Mode Voltage

The TLV320AIC3212 allows the user to set the common mode voltage for analog inputs to 0.75V or 0.9V by programming B0_P1_R8_D2. The input common-mode voltage of 0.9V works best when the analog supply voltage is centered around 1.8V or above, and offers the highest possible performance. For analog supply voltages below 1.8V, a common mode voltage of 0.75V must be used.

Table 3-3. Input Common Mode voltage and Input Signal Swing

Input Common Mode Voltage (V)	AVdd (V)	Channel Gain (dB)	Single-Ended Input Swing for 0dBFS output signal (V_{RMS})	Differential Input Swing for 0dBFS output signal (V_{RMS})
0.75	>1.5	–2	0.375	0.75
0.90	1.8 … 1.95	0	0.5	1.0

NOTE: The input common mode setting is common for DAC playback and Analog Bypass path

Example Setups

The following example setups can be taken directly for the TLV320AIC3212 EVM setup.

The # marks a comment line, w marks an I²C write command followed by the device address, the I²C register address and the value.

4.1 Stereo DAC Playback with 48ksps Sample Rate, Ground-Centered Headphone

4.1.1 Setup A - High Audio Output Power, High Performance

```
##################################################################################################
# Headphone Playback, Setup A, High Performance, High Output Power, 48kHz Sampling Rate
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V;
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 128, PRB_P1
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
##################################################################################################

##################################################################################################
# Software Reset
##################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##################################################################################################
# Power and Analog Configuration
##################################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 00        # Full chip CM = 0.9V (Setup A)
w 30 03 00        # PTM_P3, High Performance (Setup A)
w 30 04 00        # PTM_P3, High Performance (Setup A)

##################################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##################################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2 (Setup A)
w 30 0d 00 80     # Program the OSR of DAC to 128 to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

##################################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##################################################################################################
```

```
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin
w 30 08 50        # Left Channel DAC and Primary ASI's Right channel data to
                  # Right Channel DAC

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00         # Select Page 0
w 30 3c 01         # Set the DAC Mode to PRB_P1 (Setup A)

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00         # Select Page 0
w 30 3f c0         # Power up the Left and Right DAC Channels with route the Primary
                   # ASI's left channel data to Left DAC and right channel to Right DAC
w 30 40 00         # Unmute the DAC digital volume control

w 30 00 01         # Select Page 1
w 30 09 00         # HP Sizing = 100% (Setup A)
w 30 1f 85         # Headphone in Ground-centered Mode, HPL Gain=5dB (Setup A)
w 30 20 85         # HPR To have same gain as HPL, set to 5dB (Setup A)
w 30 1b 33         # Enable DAC to HPL/R and power-up HPL/R
```

4.1.2 Setup B - High Audio Output Power, Low Power Consumption

```
##############################################################################################
# Headphone Playback, Setup B, Low Power Consumption, High Output Power, 48kHz Sampling
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.26V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 64, PRB_P7
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 04        # Full chip CM = 0.75V (Setup B)
w 30 03 04        # PTM_P2, High Performance (Setup B)
w 30 04 04        # PTM_P2, High Performance (Setup B)

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
```

```
w 30 0c 84        # MDAC = 4 (Setup B)
w 30 0d 00 40     # Program the OSR of DAC to 64 to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 3.072MHz / 64 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin
w 30 08 50        # Left Channel DAC and Primary ASI's Right channel data to Right Channel DAC

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00         # Select Page 0
w 30 3c 07         # Set the DAC Mode to PRB_P7 (Setup B)

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00         # Select Page 0
w 30 3f c0         # Power up the Left and Right DAC Channels with route the Primary
                   # ASI's left channel data to Left DAC and right channel to Right DAC
w 30 40 00         # Unmute the DAC digital volume control

w 30 00 01         # Select Page 1
w 30 09 00         # HP Sizing = 100% (Setup B)
w 30 1f 8c         # Headphone in Ground-centered Mode, HPL Gain=12dB (Setup B)
w 30 20 8c         # HPR To have same gain as HPL, set to 12dB (Setup B)
w 30 1b 33         # Enable DAC to HPL/R and power-up HPL/R
```

4.1.3 Setup C - Medium Audio Output Power, High Performance

```
##############################################################################################
# Headphone Playback, Setup A, High Performance, Medium Output Power, 48kHz Sampling Rate
# AVDDx_18, HVDD_18, CPVDD_18 = 1.5V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.26V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 64, PRB_P7
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 04        # Full chip CM = 0.75V (Setup C)
w 30 03 04        # PTM_P2, High Performance (Setup C)
w 30 04 04        # PTM_P2, High Performance (Setup C)

##############################################################################################
```

```
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
###############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 84        # MDAC = 4 (Setup C)
w 30 0d 00 40     # Program the OSR of DAC to 64 (Setup C) to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 3.072MHz / 64 = 48kHz

###############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
###############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin
w 30 08 50        # Left Channel DAC and Primary ASI's Right channel data to
                  # Right Channel DAC

###############################################################################################
# Signal Processing Settings
###############################################################################################
w 30 00 00         # Select Page 0
w 30 3c 07         # Set the DAC Mode to PRB_P7 (Setup C)

###############################################################################################
# Output Channel Configuration
###############################################################################################
w 30 00 00         # Select Page 0
w 30 3f c0         # Power up the Left and Right DAC Channels with route the Primary
                   # ASI's left channel data to Left DAC and right channel to Right DAC
w 30 40 00         # Unmute the DAC digital volume control

w 30 00 01         # Select Page 1
w 30 09 00         # HP Sizing = 100% (Setup C)
w 30 1F 87         # Headphone in Ground-centered Mode, HPL Gain=7dB (Setup C)
w 30 20 87         # HPR To have same gain as HPL, set to 7dB
w 30 1b 33         # Enable DAC to HPL/R and power-up HPL/R
```

4.1.4 Setup D - Medium Audio Output Power, Lowest Power Consumption

```
###############################################################################################
# Headphone Playback, Setup D, Low Power Consumption, Reduced Output Power,
# 48kHz Sampling Rate
# AVDDx_18, HVDD_18, CPVDD_18 = 1.5V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.26V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 64, PRB_P26
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
###############################################################################################

###############################################################################################
# Software Reset
###############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

###############################################################################################
# Power and Analog Configuration
###############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
```

```
w 30 7a 01        # REF charging time = 40ms
w 30 08 04        # Full chip CM = 0.75V (Setup D)
w 30 03 08        # PTM_P1, High Performance (Setup D)
w 30 04 08        # PTM_P1, High Performance (Setup D)

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 84        # NDAC = 4 (Setup D)
w 30 0c 81        # MDAC = 1 (Setup D)
w 30 0d 00 40     # Program the OSR of DAC to 64 (Setup D) to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 3.072MHz / 64 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin
w 30 08 50        # Left Channel DAC and Primary ASI's Right channel data to
                  # Right Channel DAC

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3c 1a        # Set the DAC Mode to PRB_P26 (Setup D)

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3f c0        # Power up the Left and Right DAC Channels with route the Primary ASI's
                  # left channel data to Left DAC and right channel to Right DAC
w 30 40 00        # Unmute the DAC digital volume control

w 30 00 01        # Select Page 1
w 30 09 70        # HP Sizing = 25% (Setup D)
w 30 1f 8a        # Headphone in Ground-centered Mode, HPL Gain=10dB (Setup D)
w 30 20 8a        # HPR To have same gain as HPL, set to 10dB (Setup D)
w 30 1b 33        # Enable DAC to HPL/R and power-up HPL/R
```

4.2 PGA Analog Bypass to Ground-Centered Headphones

```
##############################################################################################
# Direct IN2L/IN2R Analog Bypass through MicPGA and Mixer Amplifiers to
# Ground-Centered Headphones
# This script routes IN2L/R inputs to Ground-Centered Headphone drivers with
# PGA gain controls (MAL/MAR + MicPGAs).
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7F 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond
```

```
##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 22 3e        # 8/8 CP sizing (Setup A)
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 00        # Full chip CM = 0.9V
d 40              # Wait for reference to power up

##############################################################################################
# Audio Bypass Routing Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 34 20        # Connect IN2L(Mic_In) to PGA with 20k input
w 30 37 20        # Connect IN2R(Mic_In) to PGA with 20k input
w 30 36 80        # Set Left common mode input resistor to 20k
w 30 39 80        # Set Right common mode input resistor to 20k
w 30 12 00        # Connect left PGA to left analog mixer
w 30 13 00        # Connect right PGA to right analog mixer
w 30 3b 00        # Unmute left PGA
w 30 3c 00        # Unmute right PGA
w 30 11 0c        # Power-on left and right analog mixers (MAL, MAR)

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 1F 80        # Headphone in Ground-centered Mode, HPL Gain=0dB
w 30 20 80        # HPR To have same gain as HPL, set to 0dB
w 30 09 00        # HP Sizing = 100%
w 30 1B c3        # Enable MAL/MAR to HPL/R and power-up HPL/R
```

4.3 Receiver Driver Example Scripts

4.3.1 Mono DAC Playback from Audio Serial Interface #1 to Right DAC Output to Differential Receiver, 48kHz

```
##############################################################################################
# Receiver Differential Playback
# Right DAC Differential Output to LOL/LOR to Differential Receiver
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 128, PRB_P1
# Primary I2S interface used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection and make analog supplies available
```

```
w 30 7a 01        # REF charging time = 40ms


##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2
w 30 0d 00 80     # Program the OSR of DAC to 128,
                  # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin


##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3c 01        # Set the DAC PRB Mode to PRB_P1


##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3f c0        # Power up the Left and Right DAC Channels
w 30 40 00        # Unmute the DAC digital volume control

w 30 00 01        # Select Page 1
w 30 03 00        # Set PTM mode for Left DAC to PTM_P3 (default, writing here optional)
w 30 04 00        # Set PTM mode for Right DAC to PTM_P3 (default, writing here optional)
w 30 16 63        # Enable Right DAC differential to LOL/R routing and power-up LOL/R
w 30 08 03        # Set output common mode for drivers (REC) to 1.65V assuming
                  # RECVDD_33 = 3.3

w 30 24 00        # Set routing of LOL to RECP to 0dB
w 30 25 80        # Set routing of LOR to RECM to follow LOL->RECP setting
w 30 2A 04        # Set offset callibration scheme for RECP/M
w 30 29 80        # Use Single Volume Control for Differential Receiver
w 30 28 C0        # Power up the RECP and RECM drivers with gain set to 0 dB
```

4.3.2 Direct Analog Bypass to Differential Receiver

```
##############################################################################################
# Direct IN1L/IN1R Analog Bypass to Differential Receiver
# This script routes IN1_L/R inputs to Differential Receiver directly.
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
```

```
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 08 00        # Full chip CM = 0.9V
d 40              # Wait for reference to power up

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 26 00        # IN1L to RECP
w 30 27 00        # IN1R to RECM
w 30 08 03        # Set output common mode for drivers (REC) to 1.65V assuming
                  # RECVDD_33 = 3.3
w 30 2A 04        # Set offset callibration scheme for RECP/M
w 30 29 80        # Use Single Volume Control for Differential Receiver
w 30 28 C0        # Power up the RECP and RECM drivers with gain set to 0 dB
```

4.4 Stereo Class-D Speakers Example Scripts

4.4.1 Primary Audio Serial Interface to Stereo DAC to Class-D, 48kHz Sampling Rate

```
##############################################################################################
# Class-D Speaker Playback, 48kHz Sampling Rate
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 128, PRB_P1
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2
w 30 0d 00 80     # Program the OSR of DAC to 128,
                  # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
```

```
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3c 01        # Set the DAC PRB Mode to PRB_P1

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 03 00        # Set PTM mode for Left DAC to PTM_P3 (default, writing here optional)
w 30 04 00        # Set PTM mode for Right DAC to PTM_P3 (default, writing here optional)
w 30 16 c3        # Enable DAC to LOL/R routing and power-up LOL/R

w 30 2E 00        # Route LOL to SPK-Left @ 0dB
w 30 2F 00        # Route LOR to SPK-Right @ 0dB
w 30 30 11        # Set Left Speaker Gain @ 6dB, Right Speaker Gain @ 6dB
w 30 2D 03        # Power-up Stereo Speaker

w 30 00 00        # Select Page 0
w 30 3f c0        # Power up the Left and Right DAC Channels
w 30 40 00        # Unmute the DAC digital volume control
```

4.4.2 PGA Analog Bypass to Stereo Class-D Speakers

```
##############################################################################################
# Direct IN2L/IN2R Analog Bypass through MicPGA and Mixer Amplifiers to Class-D Speakers
# This script routes IN2L/R inputs to Stereo Class-D Speaker drivers with
# PGA gain controls (MAL/MAR + MicPGAs).
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7F 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 08 00        # Full chip CM = 0.9V
d 40              # Wait for reference to power up

##############################################################################################
# Audio Bypass Routing Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 34 20        # Connect IN2L(Mic_In) to PGA with 20k input
w 30 37 20        # Connect IN2R(Mic_In) to PGA with 20k input
w 30 36 80        # Set Left common mode input resistor to 20k
```

```
w 30 39 80        # Set Right common mode input resistor to 20k
w 30 12 00        # Connect left PGA to left analog mixer
w 30 13 00        # Connect right PGA to right analog mixer
w 30 3b 00        # Unmute left PGA
w 30 3c 00        # Unmute right PGA
w 30 11 0c        # Power-on left and right analog mixers (MAL, MAR)

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 17 80        # Connect left analog mixer to LOL
w 30 17 c0        # Connect right analog mixer to LOR
w 30 2e 00        # Connect LOL to SPKL
w 30 2f 00        # Connect LOR to SPKR
w 30 16 03        # Power LOL, LOR
w 30 2d 03        # Power SPKL, SPKR
w 30 30 11        # Unmute SPKL,SPKR to 6dB (min) volume
```

4.5 Line Out Example Scripts

4.5.1 Stereo DAC Playback to Line Out

```
##############################################################################################
# Lineout Playback, 48kHz Sampling Rate
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288MHz
# PLL Disabled, DOSR = 128, PRB_P1
# Audio Serial Interface #1 used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2
w 30 0d 00 80     # Program the OSR of DAC to 128,
#                   DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 playback
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin
```

```
##################################################################################################
# Signal Processing Settings
##################################################################################################
w 30 00 00        # Select Page 0
w 30 3c 01        # Set the DAC PRB Mode to PRB_P1


##################################################################################################
# Output Channel Configuration
##################################################################################################
w 30 00 00        # Select Page 0
w 30 3f c0        # Power up the Left and Right DAC Channels
w 30 40 00        # Unmute the DAC digital volume control

w 30 00 01        # Select Page 1
w 30 03 00        # Set PTM mode for Left DAC to PTM_P3 (default, writing here optional)
w 30 04 00        # Set PTM mode for Right DAC to PTM_P3 (default, writing here optional)
w 30 16 c3        # Enable DAC to LOL/R routing and power-up LOL/R
```

4.6 Recording and Voice Setup Scripts

4.6.1 Stereo ADC with 48ksps Sample Rate and High Performance

```
##################################################################################################
# ADC Stereo Record - High Performance
# SE input signal from IN2L/IN2R
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, AOSR = 128, PTM_R1
# CM = 0.9V
# Primary I2S Interface used with WCLK & BCLK as inputs to the device
##################################################################################################

##################################################################################################
# Software Reset
##################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##################################################################################################
# Power and Analog Configuration
##################################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##################################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##################################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set ADC_CLKIN as MCLK1 -- default not mandatory to program
w 30 12 81        # Power Up NADC, NADC = 1
w 30 13 82        # Power Up MADC, MADC = 2
w 30 14 80        # Program the OSR of ADC to 128,
                  # ADC_FS = ADC_MOD_CLK / AOSR = 6.144MHz / 128 = 48kHz

##################################################################################################
```

```
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 recording
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3d 01        # Set the ADC PRB Mode to PRB_R1

##############################################################################################
# ADC Input Channel Configuration --- IN2L / IN2R
##############################################################################################

w 30 00 01        # Select Page 1
w 30 08 00        # Set the input common mode to 0.9V
w 30 34 20        # Route IN2L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 37 20        # Route IN2R and CM1 to RIGHT ADCPGA with 20K input impedance
w 30 39 80
w 30 3B 0C        # Left Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3C 0C        # Right Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3D 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 C0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB
```

4.6.2 Stereo ADC with 48ksps Sample Rate and Low Power

```
##############################################################################################
# ADC Stereo Record - Lower Power
# SE input signal from IN2L/IN2R
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, AOSR = 128, PTM_R1
# CM = 0.75
# Primary I2S Interface used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
```

```
w 30 04 00        # Set ADC_CLKIN as MCLK1 -- default not mandatory to program
w 30 12 81        # Power Up NADC, NADC = 1
w 30 13 84        # Power Up MADC, MADC = 4
w 30 14 40        # Program the OSR of ADC to 64,
                  # ADC_FS = ADC_MOD_CLK / AOSR = 3.072MHz / 64 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 recording
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3d 07        # Set the ADC PRB Mode to PRB_R7

##############################################################################################
# ADC Input Channel Configuration --- IN2L / IN2R
##############################################################################################

w 30 00 01        # Select Page 1
w 30 08 04        # Set the input common mode to 0.75V
w 30 34 20        # Route IN2L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 37 20        # Route IN2R and CM1 to RIGHT ADCPGA with 20K input impedance
w 30 39 80
w 30 3B 0C        # Left Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3C 0C        # Right Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3D 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 C0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB
```

4.6.3 Cellular Headset - Stereo Headphone with Mono External Microphone, 8kHz

```
##############################################################################################
#  Mono Headset - Microphone Record through IN1L with Stereo Headphone, 8kHz
#  AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
#  SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
#  MCLK = 4.096MHz
#  PLL Enabled, P=1, R=1, J=24, D=0
#  NDAC=2, MDAC=8, DOSR = 768, NADC=2, MADC=48, AOSR = 128
#  PRB_R1, PRB_P1
#  Primary I2S interface used with WCLK & BCLK as inputs to the device
##############################################################################################

##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
```

```
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##############################################################################################
# Clock configuration
# MCLK = 4.096 MHz, BCLK = 512 kHz, WCLK = 8 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 33        # Set ADC_CLKIN = PLL_CLK and DAC_CLKIN = PLL_CLK

w 30 05 00        # Set PLL_CLKIN = MCLK1
w 30 06 91        # PLL settings:  P=1, R=1
w 30 07 18        # PLL settings:  P=1, R=1, J=24
w 30 08 00        # D=0000 (MSB)
w 30 09 00        # D=0000 (LSB)

w 30 0b 82        # NDAC = 2, divider powered off
w 30 0c 88        # DAC Power MDAC = 8
w 30 0d 03        # DOSR = 768 (MSB)
w 30 0e 00        # DOSR = 768 (LSB)

w 30 12 02        # NADC Powerdown NADC=2
w 30 13 b0        # NADC Powerup, MADC=48
w 30 14 80        # AOSR = 128

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 recording
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # Audio Serial Interface #1 is set to I2S mode, 16-bit
w 30 0a 00        # Route ASI#1 WCLK and BCLK to WCLK1 pin and BCLK1 pin

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3c 01        # Set the DAC PRB Mode to PRB_P1
w 30 3d 01        # Set the ADC PRB Mode to PRB_R1

##############################################################################################
# ADC Input Channel Configuration --- IN1L
##############################################################################################
w 30 00 01        # Select Page 1
w 30 08 00        # Set the input common mode to 0.9V
w 30 33 40        # Mic Bias enabled, Source = Avdd, 1.62V
w 30 34 80        # Route IN1L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 3B 3C        # Left Channel Analog ADC PGA = 30 dB
w 30 3D 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 C0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3F C0        # Power-up the Left & Right DAC Channels
w 30 40 00        # Unmute the DAC digital volume control

w 30 00 01        # Select Page 1
w 30 03 00        # Set PTM mode for Left DAC to PTM_P3 (default, writing here optional)
w 30 04 00        # Set PTM mode for Right DAC to PTM_P3 (default, writing here optional)

w 30 1F 80        # Headphone in Ground-centered Mode, HPL Gain=0dB
```

```
w 30 20 80        # HPR To have same gain as HPL, set to 0dB
w 30 09 00        # HP Sizing = 100% (Setup A)
w 30 1B 33        # Enable DAC to HPL/R and power-up HPL/R
```

4.6.4 Recording/Playback using Low-Frequency Clocking

```
##############################################################################################
# Low-Frequency Clocking Operation
##############################################################################################
##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00       # Select Page 0
w 30 7F 00       # Select Book 0
w 30 01 01       # Software Reset
d 1              # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01       # Select Page 1
w 30 01 00       # Disable weak AVDD to DVDD connection
w 30 79 33       # MicPGA Quick Charge = 1.1/0.5 ms
w 30 7a 01       # Set the REF charging time to 30ms

##############################################################################################
# Charge Pump Configuration
##############################################################################################
w 30 00 01       # Select Page 1
w 30 21 28       # CP Clock Divider = 4 (8MHz/(6*4)) = 333kHz
w 30 22 3e       # Buffered AVSS_SENSE, 1x current, offset corr.
w 30 23 10       # Charge Pump Auto-power

##############################################################################################
# LFO Configuration
# MCLK2 = 32 kHz,
# HFO Trim Ratio = 50 MHz / MCLK2
# HF_REF_CLK Ratio = 12 MHz / MCLK2
##############################################################################################
w 30 00 04       # Select Page 4
w 30 52 10       # Enable MCLK2 pin input
w 30 00 00       # Select Page 0
w 30 18 7F       # LFR_CLKIN = MCLK2, HF_CLKIN = HF_OSC_CLK
w 30 1D 60       # HFO Source=DVDD, Enable Calibration, (25:24)
w 30 1E 00 06 1B # HFO Trim Ratio(23:0)
w 30 19 00       # HF_REF_CLK lock threshold = 2048, (27:24)
w 30 1A 00 01 77 # HF_REF_CLK Ratio(23:0)


##############################################################################################
# Clock and Interface Configuration
# PLL_CLKIN = 12 MHz, WCLK = 44.1 kHz
##############################################################################################
w 30 00 00       # Select Page 0
w 30 04 33       # DAC_CLKIN and ADC_CLKIN = PLL_CLK
w 30 05 18       # PLL Low Range, PLL_CLKIN = HF_REF_CLK
w 30 06 91       # PLL on, P=1, R=1
w 30 07 07       # J=7
w 30 08 14 90    # D=5264
w 30 0b 82 88    # NDAC = 2, MDAC = 8, powered
w 30 0D 00 80    # DOSR = 128
w 30 12 82 88    # NADC = 2, MADC = 8, powered
w 30 14 80       # AOSR = 128

##############################################################################################
```

```
# ASI Configuration
##################################################################################################
w 30 00 04       # Select Page 4
w 30 01 10       # Set ASI1 in 24-bit mode
w 30 0A 24       # BCLK1/WCLK1 are ASI1 outputs
w 30 0B 01       # ASI1_BDIV_CLKIN = DAC_MOD_CLK
w 30 0C 82       # BCLK N = 2, powered
# w 30 76 30       # ADC to DAC Loopback

##################################################################################################
# Signal Processing Configuration
##################################################################################################
w 30 00 00       # Select Page 0
w 30 3C 02 02    # PRB_P2 and PRB_R2 selected

##################################################################################################
# Audio Input Configuration
##################################################################################################
w 30 00 01       # Select Page 1
w 30 34 40       # LEFT_P  = IN1L (10K)
w 30 36 40       # LEFT_M  = CM1L (10K)
w 30 37 40       # RIGHT_P = IN1R (10K)
w 30 39 40       # RIGHT_M = CM1R (10K)
w 30 3b 00       # L_MicPGA = 0dB
w 30 3c 00       # R_MicPGA = 0dB
w 30 00 00       # Select Page 0
w 30 51 c0       # Power up LADC/RADC
w 30 52 00       # Unmute LADC/RADC

##################################################################################################
# Audio Output Configuration
##################################################################################################
w 30 00 01       # Select Page 1
w 30 09 10       # HP Output = 100%
w 30 1B 33       # Route LDAC/RDAC to HPL/HPR, Power up HPL/HPR
w 30 1F 80 80    # HPL/HPR driver = 0dB Gain
w 30 00 00       # Select Page 0
w 30 41 00 00    # DAC Gain = 0dB
w 30 3f c0       # Power up LDAC/RDAC
w 30 40 00       # Unmute LDAC/RDAC
```

4.7 Scripts for Audio Serial Interfaces #2 and #3

4.7.1 Stereo DAC Playback to Ground-Centered Headphone from Audio Serial Interface #2, 48kHz

```
##################################################################################################
# Audio Serial Interface #2 to Stereo DAC to Headphone Output
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #2 signals routed to DIN2 (DIN), BCLK2 (BCLK), DOUT2 (DOUT),
# WCLK2 (WCLK) - Codec ASI#2 is Slave
##################################################################################################

##################################################################################################
# Codec Software Reset
##################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
```

```
d 1                    # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01         # Select Page 1
w 30 01 00         # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01         # REF charging time = 40ms
w 30 22 3e         # 8/8 CP sizing (Setup A)
w 30 21 28         # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10         # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 00         # Full chip CM = 0.9V
w 30 03 00         # PTM_P3, High Performance
w 30 04 00         # PTM_P3, High Performance

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00         # Select Page 0
w 30 04 00         # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81         # NDAC = 1
w 30 0c 82         # MDAC = 2
w 30 0d 00 80      # Program the OSR of DAC to 128 to get
                   # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #2
# ASI #2 connected to BCLK2, WCLK2, DIN2, and DOUT2 pins
##############################################################################################
w 30 00 04         # Select Page 4
w 30 11 00         # Audio Serial Interface #2 = I2S mode, 16-bit
w 30 1a 00         # For Audio Serial Interface #1,
                   # Select BCLK2 as BCLK input and WCLK2 as WCLK input
w 30 17 01         # Route ADC data to Audio Serial Interface #2
w 30 18 50         # ASI#2 Left Channel data sent to Left Channel DAC,
                   # ASI#2 Right channel data sent to Right Channel DAC

w 30 45 04         # Select WCLK2 pin as WCLK for Audio Serial Interface #2
w 30 46 04         # Select BCLK2 pin as BCLK for Audio Serial Interface #2
w 30 47 22         # Select DOUT2 pin as DOUT for Audio Serial Interface #2
w 30 48 20         # Select DIN2 pin as DIN for Audio Serial Interface #2

w 30 76 16         # Only ASI#2 Routed to  DAC Data Input

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00          # Select Page 0
w 30 3c 01          # Set the DAC Mode to PRB_P1

##############################################################################################
# Output Channel Configuration
##############################################################################################
w 30 00 00          # Select Page 0
w 30 3f c0          # Power up the Left and Right DAC Channels
w 30 40 00          # Unmute the DAC digital volume control

w 30 00 01          # Select Page 1
w 30 1f 80          # Headphone in Ground-centered Mode, HPL Gain=0dB
w 30 20 80          # HPR To have same gain as HPL, set to 0dB
w 30 09 00          # HP Sizing = 100%
w 30 1b 33          # Enable DAC to HPL/R and power-up HPL/R
```

4.7.2 Stereo ADC Recording from IN2L/IN2R to Audio Serial Interface #2, 48kHz

```
##############################################################################################
# IN2L/IN2R to Stereo ADC to Audio Serial Interface #2
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #2 signals routed to DIN2 (DIN), BCLK2 (BCLK), DOUT2 (DOUT),
# WCLK2 (WCLK) - Codec ASI#2 is Slave
##############################################################################################

##############################################################################################
# Codec Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set ADC_CLKIN as MCLK1 -- default not mandatory to program
w 30 12 81        # Power Up NADC, NADC = 1
w 30 13 82        # Power Up MADC, MADC = 2
w 30 14 80        # Program the OSR of ADC to 128,
                  # ADC_FS = ADC_MOD_CLK / AOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #2
# ASI #2 connected to BCLK2, WCLK2, DIN2, and DOUT2 pins
##############################################################################################
w 30 00 04        # Select Page 4
w 30 11 00        # Audio Serial Interface #2 = I2S mode, 16-bit
w 30 1a 00        # For Audio Serial Interface #1,
                  # Select BCLK2 as BCLK input and WCLK2 as WCLK input
w 30 17 01        # Route ADC data to Audio Serial Interface #2
w 30 18 50        # ASI#2 Left Channel data sent to Left Channel DAC,
                  # ASI#2 Right channel data sent to Right Channel DAC
w 30 45 04        # Select WCLK2 pin as WCLK for Audio Serial Interface #2
w 30 46 04        # Select BCLK2 pin as BCLK for Audio Serial Interface #2
w 30 47 22        # Select DOUT2 pin as DOUT for Audio Serial Interface #2
w 30 48 20        # Select DIN2 pin as DIN for Audio Serial Interface #2

w 30 76 16        # Only ASI#2 Routed to  DAC Data Input

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3d 01        # Set the ADC PRB Mode to PRB_R1

##############################################################################################
# ADC Input Channel Configuration --- IN2L / IN2R
```

```
##################################################################################################
w 30 00 01        # Select Page 1
w 30 08 00        # Set the input common mode to 0.9V
w 30 34 20        # Route IN2L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 37 20        # Route IN2R and CM1 to RIGHT ADCPGA with 20K input impedance
w 30 39 80
w 30 3b 0c        # Left Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3c 0c        # Right Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3d 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 c0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB
```

4.7.3 Stereo DAC Playback to Ground-Centered Headphone from Audio Serial Interface #3, 48kHz

```
##################################################################################################
# Audio Serial Interface #3 to Stereo DAC to Headphone Output
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #3 signals routed to DIN3 (DIN), BCLK3 (BCLK), DOUT3 (DOUT),
# WCLK3 (WCLK) - Codec ASI#3 is Slave
##################################################################################################

##################################################################################################
# Codec Software Reset
##################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##################################################################################################
# Power and Analog Configuration
##################################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 22 3e        # 8/8 CP sizing (Setup A)
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 00        # Full chip CM = 0.9V
w 30 03 00        # PTM_P3, High Performance
w 30 04 00        # PTM_P3, High Performance

##################################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##################################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2
w 30 0d 00 80     # Program the OSR of DAC to 128 to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz


##################################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #3
# ASI #3 connected to BCLK3, WCLK3, DIN3, and DOUT3 pins
```

```
##################################################################################################
w 30 00 04        # Select Page 4
w 30 21 00        # Audio Serial Interface #3 = I2S mode, 16-bit
w 30 2a 00        # For Audio Serial Interface #1,
                  # Select BCLK3 as BCLK input and WCLK3 as WCLK input
w 30 27 01        # Route ADC data to Audio Serial Interface #3
w 30 28 50        # ASI#3 Left Channel data sent to Left Channel DAC,
                  # ASI#3 Right channel data sent to Right Channel DAC
w 30 49 04        # Select WCLK3 pin as WCLK for Audio Serial Interface #3
w 30 4a 04        # Select BCLK3 pin as BCLK for Audio Serial Interface #3
w 30 4b 22        # Select DOUT3 pin as DOUT for Audio Serial Interface #3
w 30 4c 20        # Select DIN3 pin as DIN for Audio Serial Interface #3

w 30 76 2a        # Only ASI#3 Routed to  DAC Data Input

##################################################################################################
# Signal Processing Settings
##################################################################################################
w 30 00 00         # Select Page 0
w 30 3c 01         # Set the DAC Mode to PRB_P1

##################################################################################################
# Output Channel Configuration
##################################################################################################
w 30 00 00         # Select Page 0
w 30 3f c0         # Power up the Left and Right DAC Channels
w 30 40 00         # Unmute the DAC digital volume control

w 30 00 01         # Select Page 1
w 30 1f 80         # Headphone in Ground-centered Mode, HPL Gain=0dB
w 30 20 80         # HPR To have same gain as HPL, set to 0dB
w 30 09 00         # HP Sizing = 100%
w 30 1b 33         # Enable DAC to HPL/R and power-up HPL/R
```

4.7.4 Stereo ADC Recording from IN2L/IN2R to Audio Serial Interface #3, 48kHz

```
##################################################################################################
# IN2L/IN2R to Stereo ADC to Audio Serial Interface #3
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #3 signals routed to DIN3 (DIN), BCLK3 (BCLK), DOUT3 (DOUT),
# WCLK3 (WCLK) - Codec ASI#3 is Slave
##################################################################################################

##################################################################################################
# Codec Software Reset
##################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##################################################################################################
# Power and Analog Configuration
##################################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##################################################################################################
# Clock configuration
```

```
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##################################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set ADC_CLKIN as MCLK1 -- default not mandatory to program
w 30 12 81        # Power Up NADC, NADC = 1
w 30 13 82        # Power Up MADC, MADC = 2
w 30 14 80        # Program the OSR of ADC to 128,
                  # ADC_FS = ADC_MOD_CLK / AOSR = 6.144MHz / 128 = 48kHz

##################################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #3
# ASI #3 connected to BCLK3, WCLK3, DIN3, and DOUT3 pins
##################################################################################################
w 30 00 04        # Select Page 4
w 30 21 00        # Audio Serial Interface #3 = I2S mode, 16-bit
w 30 2a 00        # For Audio Serial Interface #3,
                  # Select BCLK3 as BCLK input and WCLK3 as WCLK input
w 30 27 01        # Route ADC data to Audio Serial Interface #3
w 30 28 50        # ASI#3 Left Channel data sent to Left Channel DAC,
                  # ASI#3 Right channel data sent to Right Channel DAC

w 30 49 04        # Select WCLK3 pin as WCLK for Audio Serial Interface #3
w 30 4a 04        # Select BCLK3 pin as BCLK for Audio Serial Interface #3
w 30 4b 22        # Select DOUT3 pin as DOUT for Audio Serial Interface #3
w 30 4c 20        # Select DIN3 pin as DIN for Audio Serial Interface #3

w 30 76 2a        # Only ASI#3 Routed to  DAC Data Input

##################################################################################################
# Signal Processing Settings
##################################################################################################
w 30 00 00        # Select Page 0
w 30 3d 01        # Set the ADC PRB Mode to PRB_R1

##################################################################################################
# ADC Input Channel Configuration --- IN2L / IN2R
##################################################################################################
w 30 00 01        # Select Page 1
w 30 08 00        # Set the input common mode to 0.9V
w 30 34 20        # Route IN2L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 37 20        # Route IN2R and CM1 to RIGHT ADCPGA with 20K input impedance
w 30 39 80
w 30 3b 0c        # Left Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3c 0c        # Right Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3d 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 c0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB
```

4.7.5 Stereo DAC Playback to Ground-Centered Headphone from Audio Serial Interface #1 Through GPIO pins, 48kHz

```
##################################################################################################
# Audio Serial Interface #1 to Stereo DAC to Headphone Output Through
# GPI2, GPIO2, GPIO1, GPO1 (I2C Mode Only)
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #1 signals routed to GPI2 (DIN), GPIO2 (BCLK), GPO1 (DOUT),
# GPIO1 (WCLK) - Codec ASI#1 is Slave
##################################################################################################
```

```
################################################################################################
# Codec Software Reset
################################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1               # Delay 1 millisecond

################################################################################################
# Power and Analog Configuration
################################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 22 3e        # 8/8 CP sizing (Setup A)
w 30 21 28        # CP divider = 4, 500kHz, Runs off 8MHz oscillator
w 30 23 10        # Charge Pump to power up on Ground-Centered Headphone Power-up
w 30 08 00        # Full chip CM = 0.9V
w 30 03 00        # PTM_P3, High Performance
w 30 04 00        # PTM_P3, High Performance

################################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
################################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set DAC_CLKIN as MCLK1 -- default not mandatory to program
w 30 0b 81        # NDAC = 1
w 30 0c 82        # MDAC = 2
w 30 0d 00 80     # Program the OSR of DAC to 128 to get
                  # DAC_FS = DAC_MOD_CLK / DOSR = 6.144MHz / 128 = 48kHz

################################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 connected to GPIO1, GPIO2, GPI2, and GPO1 pins
################################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 48        # For Audio Serial Interface #1, Select GPIO2 as BCLK input and
                  # GPIO1 as WCLK input
w 30 05 0b        # All Channels for Audio Serial Interface #1 Data Input from GPI2
w 30 06 0c        # All Channels for Audio Serial Interface #1 Data Output to GPO1
w 30 07 01        # Route ADC data to Audio Serial Interface #1
w 30 08 50        # ASI#1 Left Channel data sent to Left Channel DAC,
                  # ASI#1 Right channel data sent to Right Channel DAC

w 30 56 04        # Select GPIO1 pin as General Purpose Input to receive WCLK for ASI #1
w 30 57 04        # Select GPIO2 pin as General Purpose Input to receive BCLK for ASI #1
w 30 60 1e        # Select GPO1 pin as Audio Serial Interface #1 DOUT
w 30 5c 10        # Enable the GPI2 pin in order to receive DIN for ASI #1

w 30 76 06        # ASI#1 Routed to  DAC Data Input (Default)

################################################################################################
# Signal Processing Settings
################################################################################################
w 30 00 00         # Select Page 0
w 30 3c 01         # Set the DAC Mode to PRB_P1

################################################################################################
# Output Channel Configuration
################################################################################################
w 30 00 00         # Select Page 0
w 30 3f c0         # Power up the Left and Right DAC Channels
w 30 40 00         # Unmute the DAC digital volume control
```

```
w 30 00 01         # Select Page 1
w 30 1f 80         # Headphone in Ground-centered Mode, HPL Gain=0dB
w 30 20 80         # HPR To have same gain as HPL, set to 0dB
w 30 09 00         # HP Sizing = 100%
w 30 1b 33         # Enable DAC to HPL/R and power-up HPL/R
```

4.7.6 Stereo ADC Recording from IN2L/IN2R to Audio Serial Interface #1 Through GPIO pins, 48kHz

```
##############################################################################################
# IN2L/IN2R to Stereo ADC to Audio Serial Interface #1 Through GPIO pins
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288, Fs = 48kHz
# PLL Disabled, DOSR = 128, PTM_P3
# CM = 0.9
# Audio Serial Interface #1 signals routed to GPI2 (DIN), GPIO2 (BCLK), GPO1 (DOUT),
# GPIO1 (WCLK) - Codec ASI#1 is Slave
##############################################################################################

##############################################################################################
# Codec Software Reset
##############################################################################################
w 30 00 00        # Initialize to Page 0
w 30 7f 00        # Initialize to Book 0
w 30 01 01        # Initialize the device through software reset
d 1                    # Delay 1 millisecond

##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01        # Select Page 1
w 30 01 00        # Disable weak AVDD to DVDD connection, make analog supplies available
w 30 7a 01        # REF charging time = 40ms
w 30 79 33        # Set the quick charge of input coupling cap for analog inputs

##############################################################################################
# Clock configuration
# MCLK = 12.288 MHz, BCLK = 3.072 MHz, WCLK = 48 kHz (slave)
##############################################################################################
w 30 00 00        # Select Page 0
w 30 04 00        # Set ADC_CLKIN as MCLK1 -- default not mandatory to program
w 30 12 81        # Power Up NADC, NADC = 1
w 30 13 82        # Power Up MADC, MADC = 2
w 30 14 80        # Program the OSR of ADC to 128,
                  # ADC_FS = ADC_MOD_CLK / AOSR = 6.144MHz / 128 = 48kHz

##############################################################################################
# Audio Serial Interface Routing Configuration - Audio Serial Interface #1
# ASI #1 connected to GPIO1, GPIO2, GPI2, and GPO1 pins
##############################################################################################
w 30 00 04        # Select Page 4
w 30 01 00        # I2S mode, 16-bit
w 30 0a 48        # For ASI #1, Select GPIO2 as BCLK input and GPIO1 as WCLK input
w 30 05 0b        # All Channels for Audio Serial Interface #1 Data Input from GPI2
w 30 06 0c        # All Channels for Audio Serial Interface #1 Data Output to GPO1
w 30 07 01        # Route ADC data to Audio Serial Interface #1
w 30 08 50        # ASI#1 Left Channel data sent to Left Channel DAC,
                  # ASI#1 Right channel data sent to Right Channel DAC
w 30 56 04        # Select GPIO1 pin as General Purpose Input to receive WCLK for ASI #1
w 30 57 04        # Select GPIO2 pin as General Purpose Input to receive BCLK for ASI #1
w 30 60 1e        # Select GPO1 pin as Audio Serial Interface #1 DOUT
w 30 5c 10        # Enable the GPI2 pin in order to receive DIN for ASI #1
```

```
w 30 76 06        # ASI#1 Routed to  DAC Data Input (Default)

##############################################################################################
# Signal Processing Settings
##############################################################################################
w 30 00 00        # Select Page 0
w 30 3d 01        # Set the ADC PRB Mode to PRB_R1

##############################################################################################
# ADC Input Channel Configuration --- IN2L / IN2R
##############################################################################################
w 30 00 01        # Select Page 1
w 30 08 00        # Set the input common mode to 0.9V
w 30 34 20        # Route IN2L and CM1 to LEFT ADCPGA with 20K input impedance
w 30 36 80
w 30 37 20        # Route IN2R and CM1 to RIGHT ADCPGA with 20K input impedance
w 30 39 80
w 30 3b 0c        # Left Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3c 0c        # Right Channel Analog ADC PGA = 6 dB -> Overall Channel Gain of 0dB
w 30 3d 00        # ADC Analog programmed for PTM_R4

w 30 00 00        # Select Page 0
w 30 51 c0        # Power-up ADC Channel
w 30 52 00        # Unmute ADC channel and Fine Gain = 0dB
```

4.8 SAR ADC Scripts

4.8.1 Voltage Measurement through IN1L

```
##############################################################################################
# SAR ADC Voltage Measurement
# Voltage on IN1L
#    To modify for VBAT:  Ensure W14 = 1-2 for measurement
#                         and JP2 = 2-3 and JP3 = 2-3 for USB 5V supply
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V;
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288
##############################################################################################
##############################################################################################
# Software Reset
##############################################################################################
w 30 00 00     # Initialize to Page 0
w 30 01 01     # Initialize the device through software reset
d 1            # Delay 1 millisecond
##############################################################################################
# Power and Analog Configuration
##############################################################################################
w 30 00 01     # Select Page 1
w 30 01 00     # Disable weak AVDD to DVDD connection and make analog supplies available
##############################################################################################
# SAR Setup Configuration
##############################################################################################
w 30 00 03     # Select Page 3
w 30 02 18     # Set SAR ADC resolution to 12-bit,
               # Set SAR ADC Clock Divider = 8 (Recommended for 12-bit mode)
w 30 06 a8     # Use Internal 1.25V Reference for SAR Measurement,
               # Automatic Power-Up during Conversions (default),
               # SAR Reference Stabilization time = 4 milliseconds (default)
w 30 11 01     # SAR ADC Clock from Internal Oscillator
w 30 13 80     # Enable IN1 measurement(Replace with "w 30 13 20" for VBAT measurement)
w 30 12 C0     # I2C used for SAR reading, SAR data update using software control,
               # SAR data update enabled continuously
w 30 03 25     # Set conversion mode to Auto Scan, Enable Data-Available Interrupt
##############################################################################################
# SAR Threshold Setup
```

```
##########################################################################################
w 30 16 1c     # Set IN1L Maximum Threshold to 0.9375V (MSB)
w 30 17 00     # Set IN1L Maximum Threshold to 0.9375V (LSB)
w 30 18 16     # Set IN1L Minimum Threshold to 0.5V (MSB)
w 30 19 67     # Set IN1L Minimum Threshold to 0.5V (LSB)
##########################################################################################
# SAR Data and Threshold Flag Reading
##########################################################################################
w 30 12 E0     # Stop SAR Conversion briefly in order to read value
r 30 36 02     # Read IN1L Measurement Data (Replace with "r 30 3a 02" to read VBAT data)
r 30 15 01     # Read Threshold Flags,
# If IN1L reads >= 0.9375V, then B0_P3_R21_D5 becomes 1;
# If IN1L reads <= 0.5V, then B0_P3_R21_D4 becomes 1
w 30 12 C0     # Re-enable automatic updating of SAR ADC measurements
```

4.8.2 Single-Shot Buffer Mode Measurement of IN1L and VBAT

```
##########################################################################################
# SAR ADC Voltage Measurement
# Voltage on IN1L
# AVDDx_18, HVDD_18, CPVDD_18 = 1.8V; IOVDD, AVDD3_33, RECVDD_33 = 3.3V;
# SLVDD, SRVDD, SPK_V = 5V, DVdd = 1.8V
# MCLK = 12.288
##########################################################################################
##########################################################################################
# Software Reset
##########################################################################################
w 30 00 00     # Initialize to Page 0
w 30 01 01     # Initialize the device through software reset
d 1 # Delay 1 millisecond
##########################################################################################
# Power and Analog Configuration
##########################################################################################
w 30 00 01     # Select Page 1
w 30 01 00     # Disable weak AVDD to DVDD connection and make analog supplies available
##########################################################################################
# SAR Setup Configuration
##########################################################################################
w 30 00 03     # Select Page 3
w 30 02 18     # Set SAR ADC resolution to 12-bit,
               # Set SAR ADC Clock Divider = 8 (Recommended for 12-bit mode)
w 30 06 a8     # Use Internal 1.25V Reference for SAR Measurement,
               # Automatic Power-Up during Conversions (default),
                       # SAR Reference Stabilization time = 4 milliseconds (default)
w 30 11 01     # SAR ADC Clock from Internal Oscillator
w 30 13 a0     # Enable IN1L and VBAT measurments
w 30 0d c0     # Enable single-shot buffer mode, set trigger to 8 x number sampled data
w 30 03 25     # Enable auto-scan
w 30 12 c0     # I2C used for SAR reading, SAR data update using software control,
                     # SAR data update enabled continuously

##########################################################################################
# SAR Data and Read
##########################################################################################
w 30 00 03     # Change to Book 0 Page 3
w 30 12 e0     # Set interface to I2C
               # Set SAR Data update to software control
                       # SAR Data is stopped so the user can read data without corruption
w 30 00 fc     # Change to Book 0 Page 252
r 30 01 10     # Read b0_p252_r1,r2
# Read again
w 30 00 03     # Change to Book 0 Page 3
w 30 12 c0     # Restart SAR Data so the user can read data without corruption
d 100
w 30 12 e0     # SAR Data is stopped so the user can read data without corruption
```

```
w 30 00 fc     # Change to Book 0 Page 252
r 30 01 10     # Read b0_p252_r1,r2
# Read again
w 30 00 03     # Change to Book 0 Page 3
w 30 12 c0     # Restart SAR Data so the user can read data without corruption
d 100
w 30 12 e0     # SAR Data is stopped so the user can read data without corruption
w 30 00 fc     # Change to Book 0 Page 252
r 30 01 10     # Read b0_p252_r1,r2
```

Register Map and Descriptions

The TLV320AIC3212 contains 43 pages of 8-bit registers, each page can contain up to 128 registers. The register pages are divided up based on functional blocks for this device. Page 0 is the default home page after hardware reset.

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5.1 Register Map Summary

Table 5-1. Summary of Register Map

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	0	0x00	0x00	0x00	Page Select Register
0	0	1	0x00	0x00	0x01	Software Reset Register
0	0	2-3	0x00	0x00	0x02-0x03	Reserved Registers
0	0	4	0x00	0x00	0x04	Clock Control Register 1, Clock Input Multiplexers
0	0	5	0x00	0x00	0x05	Clock Control Register 2, PLL Input Multiplexer
0	0	6	0x00	0x00	0x06	Clock Control Register 3, PLL P and R Values
0	0	7	0x00	0x00	0x07	Clock Control Register 4, PLL J Value
0	0	8	0x00	0x00	0x08	Clock Control Register 5, PLL D Values (MSB)
0	0	9	0x00	0x00	0x09	Clock Control Register 6, PLL D Values (LSB)
0	0	10	0x00	0x00	0x0A	Clock Control Register 7, PLL_CLKIN Divider
0	0	11	0x00	0x00	0x0B	Clock Control Register 8, NDAC Divider Values
0	0	12	0x00	0x00	0x0C	Clock Control Register 9, MDAC Divider Values
0	0	13	0x00	0x00	0x0D	DAC OSR Control Register 1, MSB Value
0	0	14	0x00	0x00	0x0E	DAC OSR Control Register 2, LSB Value
0	0	15-17	0x00	0x00	0x0F-0x11	Reserved Registers
0	0	18	0x00	0x00	0x12	Clock Control Register 10, NADC Values
0	0	19	0x00	0x00	0x13	Clock Control Register 11, MADC Values
0	0	20	0x00	0x00	0x14	ADC Oversampling (AOSR) Register
0	0	21	0x00	0x00	0x15	CLKOUT MUX
0	0	22	0x00	0x00	0x16	Clock Control Register 12, CLKOUT M Divider Value
0	0	23	0x00	0x00	0x17	Timer clock
0	0	24	0x00	0x00	0x18	Low Frequency Clock Generation Control
0	0	25	0x00	0x00	0x19	High Frequency Clock Generation Control 1
0	0	26	0x00	0x00	0x1A	High Frequency Clock Generation Control 2
0	0	27	0x00	0x00	0x1B	High Frequency Clock Generation Control 3
0	0	28	0x00	0x00	0x1C	High Frequency Clock Generation Control 4
0	0	29	0x00	0x00	0x1D	High Frequency Clock Trim Control 1
0	0	30	0x00	0x00	0x1E	High Frequency Clock Trim Control 2
0	0	31	0x00	0x00	0x1F	High Frequency Clock Trim Control 3
0	0	32	0x00	0x00	0x20	High Frequency Clock Trim Control 4
0	0	33-35	0x00	0x00	0x21-0x23	Reserved Registers
0	0	36	0x00	0x00	0x24	ADC Flag Register
0	0	37	0x00	0x00	0x25	DAC Flag Register
0	0	38	0x00	0x00	0x26	DAC Flag Register
0	0	39-41	0x00	0x00	0x27-0x29	Reserved Registers
0	0	42	0x00	0x00	0x2A	Sticky Flag Register 1
0	0	43	0x00	0x00	0x2B	Interrupt Flag Register 1
0	0	44	0x00	0x00	0x2C	Sticky Flag Register 2
0	0	45	0x00	0x00	0x2D	Sticky Flag Register 3
0	0	46	0x00	0x00	0x2E	Interrupt Flag Register 2
0	0	47	0x00	0x00	0x2F	Interrupt Flag Register 3

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	48	0x00	0x00	0x30	INT1 Interrupt Control
0	0	49	0x00	0x00	0x31	INT2 Interrupt Control
0	0	50	0x00	0x00	0x32	SAR Control 1
0	0	51	0x00	0x00	0x33	Interrupt Format Control Register
0	0	52-59	0x00	0x00	0x34-0x3B	Reserved Registers
0	0	60	0x00	0x00	0x3C	DAC Processing Block Control
0	0	61	0x00	0x00	0x3D	ADC Processing Block Control
0	0	62	0x00	0x00	0x3E	Reserved Register
0	0	63	0x00	0x00	0x3F	Primary DAC Power and Soft-Stepping Control
0	0	64	0x00	0x00	0x40	Primary DAC Master Volume Configuration
0	0	65	0x00	0x00	0x41	Primary DAC Left Volume Control Setting
0	0	66	0x00	0x00	0x42	Primary DAC Right Volume Control Setting
0	0	67	0x00	0x00	0x43	Headset Detection
0	0	68	0x00	0x00	0x44	DRC Control Register 1
0	0	69	0x00	0x00	0x45	DRC Control Register 2
0	0	70	0x00	0x00	0x46	DRC Control Register 3
0	0	71	0x00	0x00	0x47	Beep Generator Register 1
0	0	72	0x00	0x00	0x48	Beep Generator Register 2
0	0	73	0x00	0x00	0x49	Beep Generator Register 3
0	0	74	0x00	0x00	0x4A	Beep Generator Register 4
0	0	75	0x00	0x00	0x4B	Beep Generator Register 5
0	0	76	0x00	0x00	0x4C	Beep Sin(x) MSB
0	0	77	0x00	0x00	0x4D	Beep Sin(x) LSB
0	0	78	0x00	0x00	0x4E	Beep Cos(x) MSB
0	0	79	0x00	0x00	0x4F	Beep Cos(x) LSB
0	0	80	0x00	0x00	0x50	Reserved Register
0	0	81	0x00	0x00	0x51	ADC Channel Power Control
0	0	82	0x00	0x00	0x52	ADC Fine Gain Volume Control
0	0	83	0x00	0x00	0x53	Left ADC Volume Control
0	0	84	0x00	0x00	0x54	Right ADC Volume Control
0	0	85	0x00	0x00	0x55	ADC Phase Control
0	0	86	0x00	0x00	0x56	Left AGC Control 1
0	0	87	0x00	0x00	0x57	Left AGC Control 2
0	0	88	0x00	0x00	0x58	Left AGC Control 3
0	0	89	0x00	0x00	0x59	Left AGC Attack Time
0	0	90	0x00	0x00	0x5A	Left AGC Decay Time
0	0	91	0x00	0x00	0x5B	Left AGC Noise Debounce
0	0	92	0x00	0x00	0x5C	Left AGC Signal Debounce
0	0	93	0x00	0x00	0x5D	Left AGC Gain
0	0	94	0x00	0x00	0x5E	Right AGC Control 1
0	0	95	0x00	0x00	0x5F	Right AGC Control 2
0	0	96	0x00	0x00	0x60	Right AGC Control 3
0	0	97	0x00	0x00	0x61	Right AGC Attack Time
0	0	98	0x00	0x00	0x62	Right AGC Decay Time
0	0	99	0x00	0x00	0x63	Right AGC Noise Debounce

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	0	100	0x00	0x00	0x64	Right AGC Signal Debounce
0	0	101	0x00	0x00	0x65	Right AGC Gain
0	0	102	0x00	0x00	0x66	ADC DC Measurement Control Register 1
0	0	103	0x00	0x00	0x67	ADC DC Measurement Control Register 2
0	0	104	0x00	0x00	0x68	Left Channel DC Measurement Output Register 1 (MSB Byte)
0	0	105	0x00	0x00	0x69	Left Channel DC Measurement Output Register 2 (Middle Byte)
0	0	106	0x00	0x00	0x6A	Left Channel DC Measurement Output Register 3 (LSB Byte)
0	0	107	0x00	0x00	0x6B	Right Channel DC Measurement Output Register 1 (MSB Byte)
0	0	108	0x00	0x00	0x6C	Right Channel DC Measurement Output Register 2 (Middle Byte)
0	0	109	0x00	0x00	0x6D	Right Channel DC Measurement Output Register 3 (LSB Byte)
0	0	110-114	0x00	0x00	0x6E-0x72	Reserved Registers
0	0	115	0x00	0x00	0x73	I2C Interface Miscellaneous Control
0	0	116-126	0x00	0x00	0x74-0x7E	Reserved Registers
0	0	127	0x00	0x00	0x7F	Book Selection Register
0	1	0	0x00	0x01	0x00	Page Select Register
0	1	1	0x00	0x01	0x01	Power Configuration Register
0	1	2	0x00	0x01	0x02	Reserved Register
0	1	3	0x00	0x01	0x03	Left DAC PowerTune Configuration Register
0	1	4	0x00	0x01	0x04	Right DAC PowerTune Configuration Register
0	1	5-7	0x00	0x01	0x05-0x07	Reserved Registers
0	1	8	0x00	0x01	0x08	Common Mode Register
0	1	9	0x00	0x01	0x09	Headphone Output Driver Control
0	1	10	0x00	0x01	0x0A	Receiver Output Driver Control
0	1	11	0x00	0x01	0x0B	Headphone Output Driver De-pop Control
0	1	12	0x00	0x01	0x0C	Receiver Output Driver De-Pop Control
0	1	13-16	0x00	0x01	0x0D-0x10	Reserved Registers
0	1	17	0x00	0x01	0x11	Mixer Amplifier Control
0	1	18	0x00	0x01	0x12	Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control
0	1	19	0x00	0x01	0x13	Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control
0	1	20-21	0x00	0x01	0x14-0x15	Reserved Registers
0	1	22	0x00	0x01	0x16	Lineout Amplifier Control 1
0	1	23	0x00	0x01	0x17	Lineout Amplifier Control 2
0	1	24-26	0x00	0x01	0x18-0x1A	Reserved
0	1	27	0x00	0x01	0x1B	Headphone Amplifier Control 1
0	1	28	0x00	0x01	0x1C	Headphone Amplifier Control 2
0	1	29	0x00	0x01	0x1D	Headphone Amplifier Control 3
0	1	30	0x00	0x01	0x1E	Reserved Register
0	1	31	0x00	0x01	0x1F	HPL Driver Volume Control
0	1	32	0x00	0x01	0x20	HPR Driver Volume Control
0	1	33	0x00	0x01	0x21	Charge Pump Control 1
0	1	34	0x00	0x01	0x22	Charge Pump Control 2

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	1	35	0x00	0x01	0x23	Charge Pump Control 3
0	1	36	0x00	0x01	0x24	Receiver Amplifier Control 1
0	1	37	0x00	0x01	0x25	Receiver Amplifier Control 2
0	1	38	0x00	0x01	0x26	Receiver Amplifier Control 3
0	1	39	0x00	0x01	0x27	Receiver Amplifier Control 4
0	1	40	0x00	0x01	0x28	Receiver Amplifier Control 5
0	1	41	0x00	0x01	0x29	Receiver Amplifier Control 6
0	1	42	0x00	0x01	0x2A	Receiver Amplifier Control 7
0	1	43-44	0x00	0x01	0x2B-0x2C	Reserved Registers
0	1	45	0x00	0x01	0x2D	Speaker Amplifier Control 1
0	1	46	0x00	0x01	0x2E	Speaker Amplifier Control 2
0	1	47	0x00	0x01	0x2F	Speaker Amplifier Control 3
0	1	48	0x00	0x01	0x30	Speaker Amplifier Volume Controls
0	1	49-50	0x00	0x01	0x31-0x32	Reserved Registers
0	1	51	0x00	0x01	0x33	Microphone Bias Control
0	1	52	0x00	0x01	0x34	Input Select 1 for Left Microphone PGA P-Terminal
0	1	53	0x00	0x01	0x35	Input Select 2 for Left Microphone PGA P-Terminal
0	1	54	0x00	0x01	0x36	Input Select for Left Microphone PGA M-Terminal
0	1	55	0x00	0x01	0x37	Input Select 1 for Right Microphone PGA P-Terminal
0	1	56	0x00	0x01	0x38	Input Select 2 for Right Microphone PGA P-Terminal
0	1	57	0x00	0x01	0x39	Input Select for Right Microphone PGA M-Terminal
0	1	58	0x00	0x01	0x3A	Input Common Mode Control
0	1	59	0x00	0x01	0x3B	Left Microphone PGA Control
0	1	60	0x00	0x01	0x3C	Right Microphone PGA Control
0	1	61	0x00	0x01	0x3D	ADC PowerTune Configuration Register
0	1	62	0x00	0x01	0x3E	ADC Analog PGA Gain Flag Register
0	1	63	0x00	0x01	0x3F	DAC Analog Gain Flags Register 1
0	1	64	0x00	0x01	0x40	DAC Analog Gain Flags Register 2
0	1	65	0x00	0x01	0x41	Analog Bypass Gain Flags Register
0	1	66	0x00	0x01	0x42	Driver Power-Up Flags Register
0	1	67-118	0x00	0x01	0x43-0x76	Reserved Registers
0	1	119	0x00	0x01	0x77	Headset Detection Tuning Register 1
0	1	120	0x00	0x01	0x78	Headset Detection Tuning Register 2
0	1	121	0x00	0x01	0x79	Microphone PGA Power-Up Control Register
0	1	122	0x00	0x01	0x7A	Reference Powerup Delay Register
0	1	123-127	0x00	0x01	0x7B-0x7F	Reserved Registers
0	3	0	0x00	0x03	0x00	Page Select Register
0	3	1	0x00	0x03	0x01	Reserved Register
0	3	2	0x00	0x03	0x02	Primary SAR ADC Control
0	3	3	0x00	0x03	0x03	Primary SAR ADC Conversion Mode
0	3	4-5	0x00	0x03	0x04-0x05	Reserved Registers
0	3	6	0x00	0x03	0x06	SAR Reference Control

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	3	7-8	0x00	0x03	0x07-0x08	Reserved Registers
0	3	9	0x00	0x03	0x09	SAR ADC Flags Register 1
0	3	10	0x00	0x03	0x0A	SAR ADC Flags Register 2
0	3	11-12	0x00	0x03	0x0B-0x0C	Reserved Registers
0	3	13	0x00	0x03	0x0D	SAR ADC Buffer Mode Control
0	3	14	0x00	0x03	0x0E	Reserved Register
0	3	15	0x00	0x03	0x0F	Scan Mode Timer Control
0	3	16	0x00	0x03	0x10	Reserved Register
0	3	17	0x00	0x03	0x11	SAR ADC Clock Control
0	3	18	0x00	0x03	0x12	SAR ADC Buffer Mode Data Read Control
0	3	19	0x00	0x03	0x13	SAR ADC Measurement Control
0	3	20	0x00	0x03	0x14	Reserved Register
0	3	21	0x00	0x03	0x15	SAR ADC Measurement Threshold Flags
0	3	22	0x00	0x03	0x16	IN1L Max Threshold Check Control 1
0	3	23	0x00	0x03	0x17	IN1L Max Threshold Check Control 2
0	3	24	0x00	0x03	0x18	IN1L Min Threshold Check Control 1
0	3	25	0x00	0x03	0x19	IN1L Min Threshold Check Control 2
0	3	26	0x00	0x03	0x1A	IN1R Max Threshold Check Control 1
0	3	27	0x00	0x03	0x1B	IN1R Max Threshold Check Control 2
0	3	28	0x00	0x03	0x1C	IN1R Min Threshold Check Control 1
0	3	29	0x00	0x03	0x1D	IN1R Min Threshold Check Control 2
0	3	30	0x00	0x03	0x1E	TEMP Max Threshold Check Control 1
0	3	31	0x00	0x03	0x1F	TEMP Max Threshold Check Control 2
0	3	32	0x00	0x03	0x20	TEMP Min Threshold Check Control 1
0	3	33	0x00	0x03	0x21	TEMP Min Threshold Check Control 2
0	3	34-53	0x00	0x03	0x22-0x35	Reserved Registers
0	3	54	0x00	0x03	0x36	IN1L Measurement Data (MSB)
0	3	55	0x00	0x03	0x37	IN1L Measurement Data (LSB)
0	3	56	0x00	0x03	0x38	IN1R Measurement Data (MSB)
0	3	57	0x00	0x03	0x39	IN1R Measurement Data (LSB)
0	3	58	0x00	0x03	0x3A	VBAT Measurement Data (MSB)
0	3	59	0x00	0x03	0x3B	VBAT Measurement Data (LSB)
0	3	60-65	0x00	0x03	0x3C-0x41	Reserved Registers
0	3	66	0x00	0x03	0x42	TEMP1 Measurement Data (MSB)
0	3	67	0x00	0x03	0x43	TEMP1 Measurement Data (LSB)
0	3	68	0x00	0x03	0x44	TEMP2 Measurement Data (MSB)
0	3	69	0x00	0x03	0x45	TEMP2 Measurement Data (LSB)
0	3	70-127	0x00	0x03	0x46-0x7F	Reserved Registers
0	4	0	0x00	0x04	0x00	Page Select Register
0	4	1	0x00	0x04	0x01	Audio Serial Interface 1, Audio Bus Format Control Register
0	4	2	0x00	0x04	0x02	Audio Serial Interface 1, Left Ch_Offset_1 Control Register
0	4	3	0x00	0x04	0x03	Audio Serial Interface 1, Right Ch_Offset_2 Control Register

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	4	4	0x00	0x04	0x04	Audio Serial Interface 1, Channel Setup Register
0	4	5-6	0x00	0x04	0x05-0x06	Reserved Registers
0	4	7	0x00	0x04	0x07	Audio Serial Interface 1, ADC Input Control
0	4	8	0x00	0x04	0x08	Audio Serial Interface 1, DAC Output Control
0	4	9	0x00	0x04	0x09	Audio Serial Interface 1, Control Register 9, ADC Slot Tristate Control
0	4	10	0x00	0x04	0x0A	Audio Serial Interface 1, WCLK and BCLK Control Register
0	4	11	0x00	0x04	0x0B	Audio Serial Interface 1, Bit Clock N Divider Input Control
0	4	12	0x00	0x04	0x0C	Audio Serial Interface 1, Bit Clock N Divider
0	4	13	0x00	0x04	0x0D	Audio Serial Interface 1, Word Clock N Divider
0	4	14	0x00	0x04	0x0E	Audio Serial Interface 1, BCLK and WCLK Output
0	4	15	0x00	0x04	0x0F	Audio Serial Interface 1, Data Output
0	4	16	0x00	0x04	0x10	Audio Serial Interface 1, ADC WCLK and BCLK Control
0	4	17	0x00	0x04	0x11	Audio Serial Interface 2, Audio Bus Format Control Register
0	4	18	0x00	0x04	0x12	Audio Serial Interface 2, Data Offset Control Register
0	4	19-22	0x00	0x04	0x13-0x16	Reserved Registers
0	4	23	0x00	0x04	0x17	Audio Serial Interface 2, ADC Input Control
0	4	24	0x00	0x04	0x18	Audio Serial Interface 2, DAC Output Control
0	4	25	0x00	0x04	0x19	Reserved Register
0	4	26	0x00	0x04	0x1A	Audio Serial Interface 2, WCLK and BCLK Control Register
0	4	27	0x00	0x04	0x1B	Audio Serial Interface 2, Bit Clock N Divider Input Control
0	4	28	0x00	0x04	0x1C	Audio Serial Interface 2, Bit Clock N Divider
0	4	29	0x00	0x04	0x1D	Audio Serial Interface 2, Word Clock N Divider
0	4	30	0x00	0x04	0x1E	Audio Serial Interface 2, BCLK and WCLK Output
0	4	31	0x00	0x04	0x1F	Audio Serial Interface 2, Data Output
0	4	32	0x00	0x04	0x20	Audio Serial Interface 2, ADC WCLK and BCLK Control
0	4	33	0x00	0x04	0x21	Audio Serial Interface 3, Audio Bus Format Control Register
0	4	34	0x00	0x04	0x22	Audio Serial Interface 3, Data Offset Control Register
0	4	35-38	0x00	0x04	0x23-0x26	Reserved Registers
0	4	39	0x00	0x04	0x27	Audio Serial Interface 3, ADC Input Control
0	4	40	0x00	0x04	0x28	Audio Serial Interface 3, DAC Output Control
0	4	41	0x00	0x04	0x29	Reserved Register
0	4	42	0x00	0x04	0x2A	Audio Serial Interface 3, WCLK and BCLK Control Register
0	4	43	0x00	0x04	0x2B	Audio Serial Interface 3, Bit Clock N Divider Input Control
0	4	44	0x00	0x04	0x2C	Audio Serial Interface 3, Bit Clock N Divider
0	4	45	0x00	0x04	0x2D	Audio Serial Interface 3, Word Clock N Divider
0	4	46	0x00	0x04	0x2E	Audio Serial Interface 3, BCLK and WCLK Output
0	4	47	0x00	0x04	0x2F	Audio Serial Interface 3, Data Output
0	4	48	0x00	0x04	0x30	Audio Serial Interface 3, ADC WCLK and BCLK Control
0	4	49-64	0x00	0x04	0x31-0x40	Reserved Registers
0	4	65	0x00	0x04	0x41	WCLK1 (Input/Output) Pin Control
0	4	66	0x00	0x04	0x42	Reserved Register
0	4	67	0x00	0x04	0x43	DOUT1 (Output) Pin Control

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
0	4	68	0x00	0x04	0x44	DIN1 (Input) Pin Control
0	4	69	0x00	0x04	0x45	WCLK2 (Input/Output) Pin Control
0	4	70	0x00	0x04	0x46	BCLK2 (Input/Output) Pin Control
0	4	71	0x00	0x04	0x47	DOUT2 (Output) Pin Control
0	4	72	0x00	0x04	0x48	DIN2 (Input) Pin Control
0	4	73	0x00	0x04	0x49	WCLK3 (Input/Output) Pin Control
0	4	74	0x00	0x04	0x4A	BCLK3 (Input/Output) Pin Control
0	4	75	0x00	0x04	0x4B	DOUT3 (Output) Pin Control
0	4	76	0x00	0x04	0x4C	DIN3 (Input) Pin Control
0	4	77-81	0x00	0x04	0x4D-0x51	Reserved Registers
0	4	82	0x00	0x04	0x52	MCLK2 (Input) Pin Control
0	4	83-85	0x00	0x04	0x53-0x55	Reserved Registers
0	4	86	0x00	0x04	0x56	GPIO1 (Input/Output) Pin Control
0	4	87	0x00	0x04	0x57	GPIO2 (Input/Output) Pin Control
0	4	88-90	0x00	0x04	0x58-0x5A	Reserved Registers
0	4	91	0x00	0x04	0x5B	GPI1 (Input) Pin Control
0	4	92	0x00	0x04	0x5C	GPI2 (Input) Pin Control
0	4	93-95	0x00	0x04	0x5D-0x5F	Reserved Registers
0	4	96	0x00	0x04	0x60	GPO1 (Output) Pin Control
0	4	97-100	0x00	0x04	0x61-0x64	Reserved Registers
0	4	101	0x00	0x04	0x65	Digital Microphone Input Pin Control
0	4	102-117	0x00	0x04	0x66-0x75	Reserved Registers
0	4	118	0x00	0x04	0x76	ADC/DAC Data Port Control
0	4	119	0x00	0x04	0x77	Digital Audio Engine Synchronization Control
0	4	120-127	0x00	0x04	0x78-0x7F	Reserved Registers
0	252	0	0x00	0xFC	0x00	Page Select Register
0	252	1	0x00	0xFC	0x01	SAR Buffer Mode Data (MSB) and Buffer Flags
0	252	2	0x00	0xFC	0x02	SAR Buffer Mode Data (LSB)
0	252	3-127	0x00	0xFC	0x03-0x7F	Reserved Registers
40	0	0	0x28	0x00	0x00	Page Select Register
40	0	1	0x28	0x00	0x01	ADC Adaptive CRAM Configuration Register
40	0	2-126	0x28	0x00	0x02-0x7E	Reserved Registers
40	0	127	0x28	0x00	0x7F	Book Selection Register
40	1-17	0	0x28	0x01-0x11	0x00	Page Select Register
40	1-17	1-7	0x28	0x01-0x11	0x01-0x07	Reserved Registers
40	1-17	8-127	0x28	0x01-0x11	0x08-0x7F	ADC Adaptive Coefficients C(0:509)
40	18	0	0x28	0x12	0x00	Page Select Register

Table 5-1. Summary of Register Map (continued)

Decimal			Hex			DESCRIPTION
BOOK NO.	PAGE NO.	REG. NO.	BOOK NO.	PAGE NO.	REG. NO.	
40	18	1-7	0x28	0x12	0x01-0x07	Reserved Registers
40	18	8-15	0x28	0x12	0x08-0x0F	ADC Adaptive Coefficients C(510:511)
40	18	16-127	0x28	0x12	0x10-0x7F	Reserved Registers
80	0	0	0x50	0x00	0x00	Page Select Register
80	0	1	0x50	0x00	0x01	DAC Adaptive Coefficient Bank Configuration Register
80	0	2-126	0x50	0x00	0x02-0x7E	Reserved Registers
80	0	127	0x50	0x00	0x7F	Book Selection Register
80	1-17	0	0x50	0x01-0x11	0x00	Page Select Register
80	1-17	1-7	0x50	0x01-0x11	0x01-0x07	Reserved Registers
80	1-17	8-127	0x50	0x01-0x11	0x08-0x7F	DAC Adaptive Coefficient Bank C(0:509)
80	18	0	0x50	0x12	0x00	Page Select Register
80	18	1-7	0x50	0x12	0x01-0x07	Reserved Registers
80	18	8-15	0x50	0x12	0x08-0x0F	DAC Adaptive Coefficient Bank C(510:511)
80	18	16-127	0x50	0x12	0x10-0x7F	Reserved Registers

5.2 Book 0 Page 0

5.2.1 Book 0 / Page 0 / Register 0: Page Select Register - 0x00 / 0x00 / 0x00 (B0_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.2.2 Book 0 / Page 0 / Register 1: Software Reset Register - 0x00 / 0x00 / 0x01 (B0_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R	0000 000	Reserved. Write only reset values.
D0	R/W	0	Self clearing software reset bit 0: Don't care 1: Self clearing software reset

5.2.3 Book 0 / Page 0 / Register 2-3: Reserved Registers - 0x00 / 0x00 / 0x02-0x03 (B0_P0_R2-3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

5.2.4 Book 0 / Page 0 / Register 4: Clock Control Register 1, Clock Input Multiplexers - 0x00 /

0x00 / 0x04 (B0_P0_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	DAC_CLKIN Selection Control 0000: DAC_CLKIN = MCLK1 (Device Pin) **** Refer the clocking diagram 0001: DAC_CLKIN = BCLK1 (Device Pin) **** Refer the clocking diagram 0010: DAC_CLKIN = GPIO1 (Device Pin) **** Refer the clocking diagram 0011: DAC_CLKIN = PLL_CLK (Generated On-Chip) **** Refer the clocking diagram 0100: DAC_CLKIN = BCLK2 (Device Pin) **** Refer the clocking diagram 0101: DAC_CLKIN = GPI1 (Device Pin) **** Refer the clocking diagram 0110: DAC_CLKIN = HF_REF_CLK **** Refer the clocking diagram 0111: DAC_CLKIN = HF_OSC_CLK **** Refer the clocking diagram 1000: DAC_CLKIN = MCLK2 (Device Pin) **** Refer the clocking diagram 1001: DAC_CLKIN = GPIO2 (Device Pin) **** Refer the clocking diagram 1010: DAC_CLKIN = GPI2 (Device Pin) **** Refer the clocking diagram 1011-1111: Reserved. Do not use.
D3-D0	R/W	0000	ADC_CLKIN Selection Control 0000: ADC_CLKIN = MCLK1 (Device Pin) **** Refer the clocking diagram 0001: ADC_CLKIN = BCLK1 (Device Pin) **** Refer the clocking diagram 0010: ADC_CLKIN = GPIO1 (Device Pin) **** Refer the clocking diagram 0011: ADC_CLKIN = PLL_CLK (Generated On-Chip) **** Refer the clocking diagram 0100: ADC_CLKIN = BCLK2 (Device Pin) **** Refer the clocking diagram 0101: ADC_CLKIN = GPI1 (Device Pin) **** Refer the clocking diagram 0110: ADC_CLKIN = HF_REF_CLK **** Refer the clocking diagram 0111: ADC_CLKIN = HF_OSC_CLK **** Refer the clocking diagram 1000: ADC_CLKIN = MCLK2 (Device Pin) **** Refer the clocking diagram 1001: ADC_CLKIN = GPIO2 (Device Pin) **** Refer the clocking diagram 1010: ADC_CLKIN = GPI2 (Device Pin) **** Refer the clocking diagram 1011-1111: Reserved. Do not use.

5.2.5 Book 0 / Page 0 / Register 5: Clock Control Register 2, PLL Input Multiplexer - 0x00 / 0x00 / 0x05 (B0_P0_R5)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	0	PLL Clock Range Selection Control 0: Low PLL Clock Range 1: High PLL Clock Range
D5-D2	R/W	00 00	PLL_CLKIN Selection Control 0000: PLL_CLKIN = MCLK1 (Device Pin) 0001: PLL_CLKIN = BCLK1 (Device Pin) 0010: PLL_CLKIN = GPIO1 (Device Pin) 0011: PLL_CLKIN = DIN1 (can be used for the system where DAC is not used) 0100: PLL_CLKIN = BCLK2 (Device Pin) 0101: PLL_CLKIN = GPI1 (Device Pin) 0110: PLL_CLKIN = HF_REF_CLK **** Refer the clocking diagram 0111: PLL_CLKIN = GPIO2 (Device Pin) **** Refer the clocking diagram 1000: PLL_CLKIN = GPI2 (Device Pin) **** Refer the clocking diagram 1001: PLL_CLKIN = MCLK2 (Device Pin) **** Refer the clocking diagram 1010-1111: Reserved. Do not use.
D1-D0	R	00	Reserved. Write only reset values.

5.2.6 Book 0 / Page 0 / Register 6: Clock Control Register 3, PLL P and R Values - 0x00 / 0x00 / 0x06 (B0_P0_R6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Power Control 0: PLL Power Down 1: PLL Power Up

Book 0 / Page 0 / Register 6: Clock Control Register 3, PLL P and R Values - 0x00 / 0x00 / 0x06 (B0_P0_R6) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D4	R/W	001	PLL Divider P Control 000: P=8 001: P=1 010: P=2 011: P=3 100: P=4 101: P=5 110: P=6 111: P=7
D3-D0	R/W	0001	PLL Multiplier R Control 0000: R = 16 0001: R = 1 0010: R = 2 ... 1110: R = 14 1111: R = 15

5.2.7 Book 0 / Page 0 / Register 7: Clock Control Register 4, PLL J Value - 0x00 / 0x00 / 0x07 (B0_P0_R7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Reserved. Write only reset values.
D5-D0	R/W	00 0100	PLL Multiplier J 00 0000: Reserved. Do not use. 00 0001: J=1 00 0010: J=2 … 11 1110: J=62 11 1111: J=63

5.2.8 Book 0 / Page 0 / Register 8: Clock Control Register 5, PLL D Values (MSB) - 0x00 / 0x00 / 0x08 (B0_P0_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D0	R/W	00 0000	PLL D Value MSB 6 Bits of 14-Bit Fraction 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 ... 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000 ... 11 1111 1111 1111: Do not use Note: This register will be updated only when the B0_P0_R9 is written immediately after B0_P0_R8

5.2.9 Book 0 / Page 0 / Register 9: Clock Control Register 6, PLL D Values (LSB) - 0x00 / 0x00 / 0x09 (B0_P0_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	PLL D Value LSB 8 Bits of 14-Bit Fraction 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 ... 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000 ...11 1111 1111 1111: Do not use Note: B0_P0_R9 should be written immediately after B0_P0_R8.

5.2.10 Book 0 / Page 0 / Register 10: Clock Control Register 7, PLL_CLKIN Divider - 0x00 /

0x00 / 0x0A (B0_P0_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0001	PLL_CLKIN Divider (Generates Input Clock for PLL P Divider) 000 0000: PLL_CLKIN Divider = 128 000 0001: PLL_CLKIN Divider = 1 000 0010: PLL_CLKIN Divider = 2 ... 111 1110: PLL_CLKIN Divider = 126 111 1111: PLL_CLKIN Divider = 127

5.2.11 Book 0 / Page 0 / Register 11: Clock Control Register 8, NDAC Divider Values - 0x00 / 0x00 / 0x0B (B0_P0_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NDAC Divider Power Control 0: NDAC divider powered down 1: NDAC divider powered up
D6-D0	R/W	000 0001	NDAC Value 000 0000: NDAC=128 000 0001: NDAC=1 000 0010: NDAC=2 ... 111 1110: NDAC=126 111 1111: NDAC=127 Note: Please check the clock frequency requirements in the Overview section

5.2.12 Book 0 / Page 0 / Register 12: Clock Control Register 9, MDAC Divider Values - 0x00 / 0x00 / 0x0C (B0_P0_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MDAC Divider Power Control 0: MDAC divider powered down 1: MDAC divider powered up
D6-D0	R/W	000 0001	MDAC Value 000 0000: MDAC=128 000 0001: MDAC=1 000 0010: MDAC=2 ... 111 1110: MDAC=126 111 1111: MDAC=127 Note: Please check the clock frequency requirements in the Overview section

5.2.13 Book 0 / Page 0 / Register 13: DAC OSR Control Register 1, MSB Value - 0x00 / 0x00 / 0x0D (B0_P0_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1-D0	R/W	00	DAC OSR (DOSR) Control DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 ... 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register is updated when B0_P0_R14 is written to immediately after B0_P0_R13.

5.2.14 Book 0 / Page 0 / Register 14: DAC OSR Control Register 2, LSB Value - 0x00 / 0x00 /

0x0E (B0_P0_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1000 0000	DAC OSR (DOSR) Control DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: DOSR=1 00 0000 0010: DOSR=2 ... 11 1111 1110: DOSR=1022 11 1111 1111: DOSR=1023 Note: This register should be written immediately after B0_P0_R13.

5.2.15 Book 0 / Page 0 / Register 15-17: Reserved Registers - 0x00 / 0x00 / 0x0F-0x11 (B0_P0_R15-17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.2.16 Book 0 / Page 0 / Register 18: Clock Control Register 10, NADC Values - 0x00 / 0x00 / 0x12 (B0_P0_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NADC Clock Divider Power Control 0: NADC divider powered down, ADC_CLK is same as DAC_CLK 1: NADC divider powered up
D6-D0	R/W	000 0001	NADC Value 000 0000: NADC=128 000 0001: NADC=1 ... 111 1110: NADC=126 111 1111: NADC=127

5.2.17 Book 0 / Page 0 / Register 19: Clock Control Register 11, MADC Values - 0x00 / 0x00 / 0x13 (B0_P0_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MADC Clock Divider Power Control 0: MADC divider powered down, ADC_MOD_CLK is same as DAC_MOD_CLK 1: MADC divider powered up
D6-D0	R/W	000 0001	MADC Value 000 0000: MADC=128 000 0001: MADC=1 ... 111 1110: MADC=126 111 1111: MADC=127

5.2.18 Book 0 / Page 0 / Register 20: ADC Oversampling (AOSR) Register - 0x00 / 0x00 / 0x14

(B0_P0_R20)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001: ADC AOSR = 1 0000 0010: ADC AOSR = 2 ... 0010 0000: ADC AOSR=32 (Use with PRB_R13 to PRB_R18, ADC Filter Type C) ... 0100 0000: AOSR=64 (Use with PRB_R1 to PRB_R12, ADC Filter Type A or B) ... 1000 0000: AOSR=128 (Use with PRB_R1 to PRB_R6, ADC Filter Type A) ... 1111 1110: ADC AOSR = 254 1111 1111: ADC AOSR = 255

5.2.19 Book 0 / Page 0 / Register 21: CLKOUT MUX - 0x00 / 0x00 / 0x15 (B0_P0_R21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3-D0	R/W	0000	0000: CDIV_CLKIN = MCLK1 (Device Pin) 0001: CDIV_CLKIN = BCLK1 (Device Pin) 0010: CDIV_CLKIN = DIN1 (Can be used for the systems where DAC is not required) 0011: CDIV_CLKIN = PLL_CLK (Generated On-Chip) 0100: CDIV_CLKIN = DAC_CLK (Generated On-Chip) 0101: CDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 0110: CDIV_CLKIN = ADC_CLK (Generated On-Chip) 0111: CDIV_CLKIN = ADC_MOD_MCLK (Generated On-Chip) 1000: CDIV_CLKIN = BCLK2 (Device Pin) 1001: CDIV_CLKIN = GPI1 (Device Pin) 1010: CDIV_CLKIN = High Frequency Reference Clock Generated On-Chip using HF_OSC_CLK and LFR_CLKIN 1011: CDIV_CLKIN = High Frequency Oscillator Clock (Generated On-Chip) 1100: CDIV_CLKIN = MCLK2 (Device Pin) 1101: CDIV_CLKIN = GPI2 (Device Pin) 1110 - 1111: Reserved. Do not use.

5.2.20 Book 0 / Page 0 / Register 22: Clock Control Register 12, CLKOUT M Divider Value - 0x00 / 0x00 / 0x16 (B0_P0_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	CLKOUT M Divider Power Control 0: CLKOUT M divider powered down 1: CLKOUT M divider powered up
D6-D0	R/W	000 0001	CLKOUT M Divider Value 000 0000: CLKOUT M divider = 128 000 0001: CLKOUT M divider = 1 000 0010: CLKOUT M divider = 2 ... 111 1110: CLKOUT M divider = 126 111 1111: CLKOUT M divider = 127 Note: Please check the clock frequency requirments in the application overview section.

5.2.21 Book 0 / Page 0 / Register 23: Timer clock - 0x00 / 0x00 / 0x17 (B0_P0_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	This timer clock of 1MHz is used for multiple purpose like all the interrupt generation for GPIO1, GPIO2, debounce logic, and headset detection. Select the 1MHz Timer Clock Source 0: REF_1MHZ_CLK = LF_OSC_CLK / 8 1: REF_1MHZ_CLK = MCLK1 / M (M as defined in D6:0 below)

Book 0 / Page 0 / Register 23: Timer clock - 0x00 / 0x00 / 0x17 (B0_P0_R23) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0001	MCLK Divider (M) Used to Generate REF_1MHZ_CLK 000 0000: M = 128 000 0001: M = 1 000 0010: M = 2 … 111 1110: M = 126 111 1111: M = 127

5.2.22 Book 0 / Page 0 / Register 24: Low Frequency Clock Generation Control - 0x00 / 0x00 / 0x18 (B0_P0_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	0000: LFR_CLKIN (Low frequency reference clock) = MCLK1 (Device Pin) 0001: LFR_CLKIN = WCLK1 (Device Pin) 0010: LFR_CLKIN = GPIO1 (Device Pin) 0011: LFR_CLKIN = WCLK2 (Device Pin) 0100: LFR_CLKIN = BCLK2 (Device Pin) 0101: LFR_CLKIN = GPI1 (Device Pin) 0110: LFR_CLKIN = DIN2 (Device Pin) 0111: LFR_CLKIN = MCLK2 (Device Pin) 1000: LFR_CLKIN = GPIO2 (Device Pin) 1001: LFR_CLKIN = GPI2 (Device Pin) 1010: LFR_CLKIN = WCLK3 (Device Pin) 1011: LFR_CLKIN = BCLK3 (Device Pin) 1100-1111: Reserved. Do not use.
D3-D0	R/W	1111	0000: HF_CLKIN (High frequency clock) = MCLK1 (Device Pin) 0001 - 1110: Reserved. Do not use. 1111: HF_CLKIN = HF_OSC_CLK

5.2.23 Book 0 / Page 0 / Register 25: High Frequency Clock Generation Control 1 - 0x00 / 0x00 / 0x19 (B0_P0_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	1	High Frequency Reference Clock Settling Flag 0: High Frequency Reference Clock is Settled 1: High Frequency Reference Clock is not Settled
D6	R	0	High Frequency Reference Clock Modulator Overflow Flag 0: High Frequency Reference Clock Modulator Overflow has not occurred 1: High Frequency Reference Clock Modulator Overflow has occurred
D5-D4	R/W	00	HF_REF_CLK Lock Ready Threshold 00: 2048 reference clock cycles 01: 512 reference clock cycles 10: 32 reference clock cycles 11: 8 reference clock cycles
D3-D0	R/W	0000	Ratio(27:24): Upper 4-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

5.2.24 Book 0 / Page 0 / Register 26: High Frequency Clock Generation Control 2 - 0x00 / 0x00 / 0x1A (B0_P0_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Ratio(23:16): Next 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

5.2.25 Book 0 / Page 0 / Register 27: High Frequency Clock Generation Control 3 - 0x00 / 0x00

/ 0x1B (B0_P0_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 1000	Ratio(16:8): Next 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

5.2.26 Book 0 / Page 0 / Register 28: High Frequency Clock Generation Control 4 - 0x00 / 0x00 / 0x1C (B0_P0_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0110 1010	Ratio(7:0): Lower 8-bits of 28-bit Multiplication Ratio. Used when a low frequency clock is used to generate the internal reference clock (See B0_P0_R24 for low frequency clock settings). The recommended ratio is "round(12,500,000 / LFR_CLKIN_FREQ)"

5.2.27 Book 0 / Page 0 / Register 29: High Frequency Clock Trim Control 1 - 0x00 / 0x00 / 0x1D (B0_P0_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	High Frequency Oscillator Calibration Flag 0: Calibration is not complete 1: Calibration is complete
D6	R/W	0	High Frequency Oscillator Voltage Source Control 0: AVDD1_18 1: DVDD
D5	R/W	1	High Frequency Oscillator Calibration Enable Control 0: Calibration is disabled 1: Calibration is enabled
D4-D2	R	0 00	Reserved. Write only reset values.
D1-D0	R/W	00	Ratio(25:24): Upper 2 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

5.2.28 Book 0 / Page 0 / Register 30: High Frequency Clock Trim Control 2 - 0x00 / 0x00 / 0x1E (B0_P0_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Ratio(23:16): Next 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

5.2.29 Book 0 / Page 0 / Register 31: High Frequency Clock Trim Control 3 - 0x00 / 0x00 / 0x1F (B0_P0_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0110	Ratio(15:8): Next 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

5.2.30 Book 0 / Page 0 / Register 32: High Frequency Clock Trim Control 4 - 0x00 / 0x00 / 0x20 (B0_P0_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 1010	Ratio(7:0): Lower 8 bits of 26-bit integer ratio between desired high-frequency oscillator frequency and low-frequency reference clock input

5.2.31 Book 0 / Page 0 / Register 33-35: Reserved Registers - 0x00 / 0x00 / 0x21-0x23 (B0_P0_R33-35)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.2.32 Book 0 / Page 0 / Register 36: ADC Flag Register - 0x00 / 0x00 / 0x24 (B0_P0_R36)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status Flag 0: Gain Applied in Left ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Left ADC PGA is equal to Programmed Gain in Control Register
D6	R	0	Left ADC Power Status Flag 0: Left ADC Powered Down 1: Left ADC Powered Up
D5	R	0	Left AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Left AGC is not saturated 1: Gain in Left ADC is equal to maximum allowed gain in Left AGC
D4	R	0	Reserved. Write only reset values.
D3	R	0	Right ADC PGA Status Flag 0: Gain Applied in Right ADC PGA is not equal to Programmed Gain in Control Register 1: Gain Applied in Right ADC PGA is equal to Programmed Gain in Control Register
D2	R	0	Right ADC Power Status Flag 0: Right ADC Powered Down 1: Right ADC Powered Up
D1	R	0	Right AGC Gain Status. This sticky flag will self clear on reading 0: Gain in Right AGC is not saturated 1: Gain in Right ADC is equal to maximum allowed gain in Right AGC
D0	R	0	Reserved. Write only reset values.

5.2.33 Book 0 / Page 0 / Register 37: DAC Flag Register - 0x00 / 0x00 / 0x25 (B0_P0_R37)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: Left DAC Powered Down 1: Left DAC Powered Up
D6	R	0	Reserved. Write only reset values.
D5-D4	R	00	00: Jack is not inserted 01: Jack is inserted without Microphone 10: Reserved. Do not use. 11: Jack is inserted with Microphone
D3	R	0	0: Right DAC Powered Down 1: Right DAC Powered Up
D2	R	0	Reserved. Write only reset values.
D1-D0	R	00	00: Headset is not inserted 01: Jack is inserted with mono-HS (Ground-Centered/Capless Headphone Mode Only) 10: Jack is inserted with stereo-HS (Ground-Centered/Capless Headphone Mode Only) 11: Reserved. Do not use.

5.2.34 Book 0 / Page 0 / Register 38: DAC Flag Register - 0x00 / 0x00 / 0x26 (B0_P0_R38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	1	0: Secondary Left DAC PGA is not muted 1: Secondary Left DAC PGA is muted
D6	R	1	0: Primary Left DAC PGA is not muted 1: Primary Left DAC PGA is muted
D5	R	0	0: Secondary Left DAC PGA , Applied Gain /=Programmed Gain 1: Secondary Left DAC PGA , Applied Gain =Programmed Gain
D4	R	0	0: Primary Left DAC PGA , Applied Gain /=Programmed Gain 1: Primary Left DAC PGA , Applied Gain =Programmed Gain
D3	R	1	0: Secondary Right DAC PGA is not muted 1: Secondary Right DAC PGA is muted
D2	R	1	0: Primary Right DAC PGA is not muted 1: Primary Right DAC PGA is muted
D1	R	0	0: Secondary Right DAC PGA , Applied Gain /=Programmed Gain 1: Secondary Right DAC PGA , Applied Gain =Programmed Gain

Book 0 / Page 0 / Register 38: DAC Flag Register - 0x00 / 0x00 / 0x26 (B0_P0_R38) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	0: Primary Right DAC PGA , Applied Gain /=Programmed Gain 1: Primary Right DAC PGA , Applied Gain =Programmed Gain

5.2.35 Book 0 / Page 0 / Register 39-41: Reserved Registers - 0x00 / 0x00 / 0x27-0x29 (B0_P0_R39-41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only default values.

5.2.36 Book 0 / Page 0 / Register 42: Sticky Flag Register 1 - 0x00 / 0x00 / 0x2A (B0_P0_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left DAC 1: Overflow has happened in Left DAC since last read of this register
D6	R	0	Right DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right DAC 1: Overflow has happened in Right DAC since last read of this register
D5-D4	R	00	Reserved. Do not use.
D3	R	0	Left ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left ADC 1: Overflow has happened in Left ADC since last read of this register
D2	R	0	Right ADC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right ADC 1: Overflow has happened in Right ADC since last read of this register
D1-D0	R	00	Reserved. Do not use.

5.2.37 Book 0 / Page 0 / Register 43: Interrupt Flag Register 1 - 0x00 / 0x00 / 0x2B (B0_P0_R43)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. 0: No overflow in Left DAC 1: Overflow condition is present in Left ADC at the time of reading the register
D6	R	0	Right DAC Overflow Status. 0: No overflow in Right DAC 1: Overflow condition is present in Right DAC at the time of reading the register
D5-D4	R	00	Reserved. Do not use.
D3	R	0	Left ADC Overflow Status. 0: No overflow in Left ADC 1: Overflow condition is present in Left ADC at the time of reading the register
D2	R	0	Right ADC Overflow Status. 0: No overflow in Right ADC 1: Overflow condition is present in Right ADC at the time of reading the register
D1-D0	R	00	Reserved. Write only default values.

5.2.38 Book 0 / Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x00 / 0x2C (B0_P0_R44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No Short Circuit detected at HPL/SPL/RECP driver. 1: Short Circuit is detected at HPL/SPL/RECP driver. (will be cleared when the register is read)
D6	R	0	0: No Short Circuit detected at HPR/SPR/RECM driver. 1: Short Circuit is detected at HPR/SPR/RECM driver. (will be cleared when the register is read)
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected (will be cleared when the register is read)

Book 0 / Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x00 / 0x2C (B0_P0_R44) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R	0	Headset Insertion/Removal Detect Flag 0: Insertion/Removal event not detected 1: Insertion/Removal event detected (will be cleared when the register is read)
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D1-D0	R	00	Reserved. Do not use.

5.2.39 Book 0 / Page 0 / Register 45: Sticky Flag Register 3 - 0x00 / 0x00 / 0x2D (B0_P0_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No over-temperature detected by Speaker driver. 1: Over-temperature detected by Speaker driver. (will be cleared when the register is read)
D6	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D5	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold (will be cleared when the register is read)
D4-D3	R	00	Reserved. Do not use.
D2	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D1	R	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available (will be cleared when the register is read)
D0	R	0	Reserved. Write only reset values.

5.2.40 Book 0 / Page 0 / Register 46: Interrupt Flag Register 2 - 0x00 / 0x00 / 0x2E (B0_P0_R46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No Short Circuit detected at HPL/SPL/RECP driver. 1: Short Circuit is detected at HPL/SPL/RECP driver.
D6	R	0	0: No Short Circuit detected at HPR/SPR/RECM driver. 1: Short Circuit is detected at HPR/SPR/RECM driver.
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected
D4	R	0	Headset Insertion/Removal Detect Flag 0: Headset removal detected 1: Headset insertion detected
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D1-D0	R	00	Reserved. Do not use.

5.2.41 Book 0 / Page 0 / Register 47: Interrupt Flag Register 3 - 0x00 / 0x00 / 0x2F (B0_P0_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No over-temperature detected by Speaker driver. 1: Over-temperature detected by Speaker driver.
D6	R	0	Left AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold
D5	R	0	Right AGC Noise Threshold Flag 0: Signal Power is greater than Noise Threshold 1: Signal Power was lower than Noise Threshold
D4-D3	R	00	Reserved. Do not use.
D2	R	0	Left ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D1	R	0	Right ADC DC Measurement Data Available Flag 0: Data not available 1: Data available
D0	R	0	Reserved. Write only reset values.

5.2.42 Book 0 / Page 0 / Register 48: INT1 Interrupt Control - 0x00 / 0x00 / 0x30 (B0_P0_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT1 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT1 interrupt 1: Headset Insertion even will generate a INT1 interrupt
D6	R/W	0	INT1 Interrupt for Button Press Event 0: Button Press event will not generate a INT1 interrupt 1: Button Press event will generate a INT1 interrupt
D5	R/W	0	INT1 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT1 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT1 interrupt. Read B0_P0_R44 to distinguish between Left or Right Channel
D4	R/W	0	INT1 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT1 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT1 interrupt. Read B0_P0_R45 to distinguish between Left or Right Channel
D3	R/W	0	INT1 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT1 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT1 interrupt. Read B0_P0_R44 to distinguish between HPL and HPR
D2	R/W	0	INT1 Interrupt for overflow event 0: ADC or DAC data overflow does not result in a INT1 interrupt 1: ADC or DAC data overflow will result in a INT1 interrupt. Read Page-0, Register-42 to distinguish between ADC or DAC data overflow
D1	R/W	0	0: SPK over-tempeature detected Interrupt is not used in the generation of INT1 Interrupt 1: SPK over-tempeature detected Interrupt is used in the generation of INT1 Interrupt
D0	R	0	Reserved. Write only reset values.

5.2.43 Book 0 / Page 0 / Register 49: INT2 Interrupt Control - 0x00 / 0x00 / 0x31 (B0_P0_R49)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT2 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT2 interrupt 1: Headset Insertion even will generate a INT2 interrupt
D6	R/W	0	INT2 Interrupt for Button Press Event 0: Button Press event will not generate a INT2 interrupt 1: Button Press event will generate a INT2 interrupt

Book 0 / Page 0 / Register 49: INT2 Interrupt Control - 0x00 / 0x00 / 0x31 (B0_P0_R49) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	INT2 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT2 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT2 interrupt. Read B0_P0_R44 to distinguish between Left or Right Channel
D4	R/W	0	INT2 Interrupt for AGC Noise Interrupt 0: Noise level detected by AGC will not generate a INT2 interrupt 1: Noise level detected by either off Left or Right Channel AGC will generate a INT2 interrupt. Read B0_P0_R45 to distinguish between Left or Right Channel
D3	R/W	0	INT2 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT2 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT2 interrupt. Read B0_P0_R44 to distinguish between HPL and HPR
D2	R/W	0	INT2 Interrupt for overflow event 0: ADC or DAC data overflow will not result in a INT2 interrupt 1: ADC or DAC data overflow will result in a INT2 interrupt. Read B0_P0_R42 to distinguish between ADC or DAC interrupt
D1	R/W	0	0: SPK over-tempeature detected Interrupt is not used in the generation of INT2 Interrupt 1: SPK over-tempeature detected Interrupt is used in the generation of INT2 Interrupt
D0	R	0	Reserved. Write only reset values.

5.2.44 Book 0 / Page 0 / Register 50: SAR Control 1 - 0x00 / 0x00 / 0x32 (B0_P0_R50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: If SAR measurement data out of threshold range, interrupt is not used in the generation of INT1 Interrupt. 1: If SAR measurement data out of threshold range, interrupt is used in the generation of INT1 Interrupt.
D6	R/W	0	0: SAR Data Available Interrupt is not used in the generation of INT1 Interrupt. 1: SAR Data Available Interrupt is used in the generation of INT1 Interrupt.
D5	R/W	0	0: SAR measurement data out of threshold range Interrupt is not used in the generation of INT2 Interrupt. 1: SAR measurement data out of threshold range Interrupt is used in the generation of INT2 Interrupt.
D4	R/W	0	0: SAR Data Available Interrupt is not used in the generation of INT2 Interrupt. 1: SAR Data Available Interrupt is used in the generation of INT2 Interrupt.
D3	R	0	Reserved. Write only default values.
D2	R	0	SAR Data Available Sticky Flag (will be cleared when the register is read) 0: No SAR Data Available for read. 1: SAR Data Available for read.
D1	R	0	SAR Data Threshold Sticky Flag (will be cleared when the register is read) 0: SAR data is within threshold program. 1: SAR data is out of programmed threshold range.
D0	R	0	Reserved. Write only default values.

5.2.45 Book 0 / Page 0 / Register 51: Interrupt Format Control Register - 0x00 / 0x00 / 0x33 (B0_P0_R51)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	INT1 pulse control 00: INT1 is active high interrupt of 1 pulse of minimum 2ms duration 01: INT1 is active high interrupt of multiple pulses, each of minimum duration 2ms and a total period of 4ms. To stop the pulse train, read B0_P0_R42, B0_P0_R44, or B0_P0_R45 10: INT1 is active high, level-based interrupt generated out of sticky bits in Flag registers. To clear this interrupt, read B0_P0_R42, B0_P0_R44, or B0_P0_R45. 11: INT1 is active high, level-based interrupt generated out of instantaneous value of interrupt port.

Book 0 / Page 0 / Register 51: Interrupt Format Control Register - 0x00 / 0x00 / 0x33 (B0_P0_R51) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	INT2 pulse control 00: INT2 is active high interrupt of 1 pulse of approx. 2ms duration 01: INT2 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read B0_P0_R42, B0_P0_R44, or B0_P0_R45 10: INT2 is active high, level-based interrupt generated out of sticky bits in Flag registers. To clear this interrupt, read B0_P0_R42, B0_P0_R44, or B0_P0_R45. 11: INT2 is active high, level-based interrupt generated out of instantaneous value of interrupt port.
D3-D0	R	0000	Reserved. Write only reset values.

5.2.46 Book 0 / Page 0 / Register 52-59: Reserved Registers - 0x00 / 0x00 / 0x34-0x3B (B0_P0_R52-59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.2.47 Book 0 / Page 0 / Register 60: DAC Processing Block Control - 0x00 / 0x00 / 0x3C (B0_P0_R60)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0001	0 0000: Reserved. Do not use. 0 0001: DAC Signal Processing Block PRB_P1 0 0010: DAC Signal Processing Block PRB_P2 0 0011: DAC Signal Processing Block PRB_P3 0 0100: DAC Signal Processing Block PRB_P4 ... 1 1000: DAC Signal Processing Block PRB_P24 1 1001: DAC Signal Processing Block PRB_P25 1 1010: DAC Signal Processing Block PRB_P26 1 1011-1 1111: Reserved. Do not use

5.2.48 Book 0 / Page 0 / Register 61: ADC Processing Block Control - 0x00 / 0x00 / 0x3D (B0_P0_R61)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0001	0 0000: Reserved. Do not use. 0 0001: ADC Singal Processing Block PRB_R1 0 0010: ADC Signal Processing Block PRB_R2 0 0011: ADC Signal Processing Block PRB_R3 0 0100: ADC Signal Processing Block PRB_R4 ... 1 0001: ADC Signal Processing Block PRB_R17 1 0010: ADC Signal Processing Block PRB_R18 1 0010-1 1111: Reserved. Do not use

5.2.49 Book 0 / Page 0 / Register 62: Reserved Register - 0x00 / 0x00 / 0x3E (B0_P0_R62)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.2.50 Book 0 / Page 0 / Register 63: Primary DAC Power and Soft-Stepping Control - 0x00 /

0x00 / 0x3F (B0_P0_R63)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left DAC channel is powered-down 1: Left DAC channel is powered-up
D6	R/W	0	0: Right DAC channel is powered-down 1: Right DAC channel is powered-up
D5-D2	R	00 00	Reserved. Write only reset values.
D1-D0	R/W	00	00: DAC channel volume control soft-stepping is enabled for one-step/Fs 01: DAC channel volume control soft-stepping is enabled for one-step/2Fs 10: DAC channel volume control soft-stepping is disabled 11: Reserved. Do not use.

5.2.51 Book 0 / Page 0 / Register 64: Primary DAC Master Volume Configuration - 0x00 / 0x00 / 0x40 (B0_P0_R64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right Modulator Output Control 0: When Right DAC Channel is powered down, the data is zero. 1: When Right DAC Channel is powered down, the data is inverted version of Left DAC Modulator Output. Can be used when differential mono output is used
D6-D4	R/W	000	DAC Auto Mute Control 000: Auto Mute disabled 001: DAC is auto muted if input data is DC for more than 100 consecutive inputs 010: DAC is auto muted if input data is DC for more than 200 consecutive inputs 011: DAC is auto muted if input data is DC for more than 400 consecutive inputs 100: DAC is auto muted if input data is DC for more than 800 consecutive inputs 101: DAC is auto muted if input data is DC for more than 1600 consecutive inputs 110: DAC is auto muted if input data is DC for more than 3200 consecutive inputs 111: DAC is auto muted if input data is DC for more than 6400 consecutive inputs
D3	R/W	1	Left DAC Channel Mute Control 0: Left DAC Channel not muted 1: Left DAC Channel muted
D2	R/W	1	Right DAC Channel Mute Control 0: Right DAC Channel not muted 1: Right DAC Channel muted
D1-D0	R/W	00	DAC Master Volume Control 00: Left and Right Channel have independent volume control 01: Left Channel Volume is controlled by Right Channel Volume Control setting 10: Right Channel Volume is controlled by Left Channel Volume Control setting 11: Reserved. Do not use

5.2.52 Book 0 / Page 0 / Register 65: Primary DAC Left Volume Control Setting - 0x00 / 0x00 / 0x41 (B0_P0_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Left DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use. 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB ... 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use.

5.2.53 Book 0 / Page 0 / Register 66: Primary DAC Right Volume Control Setting - 0x00 / 0x00 /

0x42 (B0_P0_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Right DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use. 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB ... 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use.

5.2.54 Book 0 / Page 0 / Register 67: Headset Detection - 0x00 / 0x00 / 0x43 (B0_P0_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset Detection Disabled 1: Headset Detection Enabled
D6-D5	R	00	Reserved. Write only reset values.
D4-D2	R/W	0 00	Headset Detection Debounce Programmability 000: Debounce Time = 16ms 001: Debounce Time = 32ms 010: Debounce Time = 64ms 011: Debounce Time = 128ms 100: Debounce Time = 256ms 101: Debounce Time = 512ms 110-111: Reserved. Do not use Note: All times are typical values
D1-D0	R/W	00	Headset Button Press Debounce Programmability 00: Debounce disabled 01: Debounce Time = 8ms 10: Debounce Time = 16ms 11: Debounce Time = 32ms Note: All times are typical values

5.2.55 Book 0 / Page 0 / Register 68: DRC Control Register 1 - 0x00 / 0x00 / 0x44 (B0_P0_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	1	Left DRC Enable Control 0: Left Channel DRC disabled 1: Left Channel DRC enabled
D5	R/W	1	Right DRC Enable Control 0: Right Channel DRC disabled 1: Right Channel DRC enabled
D4-D2	R/W	0 11	DRC Threshold control 000: DRC Threshold = -3dBFS 001: DRC Threshold = -6dBFS 010: DRC Threshold = -9dBFS 011: DRC Threshold = -12dBFS 100: DRC Threshold = -15dBFS 101: DRC Threshold = -18dBFS 110: DRC Threshold = -21dBFS 111: DRC Threshold = -24dBFS
D1-D0	R/W	11	DRC Hysteresis Control 00: DRC Hysteresis = 0dB 01: DRC Hysteresis = 1dB 10: DRC Hysteresis = 2dB 11: DRC Hysteresis = 3dB

5.2.56 Book 0 / Page 0 / Register 69: DRC Control Register 2 - 0x00 / 0x00 / 0x45 (B0_P0_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D3	R/W	011 1	DRC Hold Programmability 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks ... 1110: DRC Hold Time = 4*32768 DAC Word Clocks 1111: DRC Hold Time = 5*32768 DAC Word Clocks
D2-D0	R	000	000: Maximum rate of change of gain = 0.5dB every Fs' frame 001: Maximum rate of change of gain = 0.5dB every 2 Fs' frame 010: Maximum rate of change of gain = 0.5dB every 4 Fs' frame 011: Maximum rate of change of gain = 0.5dB every 8 Fs' frame 100: Maximum rate of change of gain = 0.5dB every 16 Fs' frame 101 - 111: Reserved. Do not use.

5.2.57 Book 0 / Page 0 / Register 70: DRC Control Register 3 - 0x00 / 0x00 / 0x46 (B0_P0_R70)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	DRC Attack Rate control 0000: DRC Attack Rate = 4.0dB per DAC Word Clock 0001: DRC Attack Rate = 2.0dB per DAC Word Clock 0010: DRC Attack Rae = 1.0dB per DAC Word Clock ... 1110: DRC Attack Rate = 2.4414e-4dB per DAC Word Clock 1111: DRC Attack Rate = 1.2207e-4dB per DAC Word Clock
D3-D0	R/W	0000	DRC Decay Rate control 0000: DRC Decay Rate = 1.5625e-2dB per DAC Word Clock 0001: DRC Decay Rate = 7.8125e-3dB per DAC Word Clock 0010: DRC Decay Rae = 3.9062e-3dB per DAC Word Clock ... 1110: DRC Decay Rate = 9.5367e-7dB per DAC Word Clock 1111: DRC Decay Rate = 4.7683e-7dB per DAC Word Clock

5.2.58 Book 0 / Page 0 / Register 71: Beep Generator Register 1 - 0x00 / 0x00 / 0x47 (B0_P0_R71)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep Generator Disabled 1: Beep Generator Enabled. This bit will self clear after the beep has been generated.
D6	R	0	Reserved. Write only reset value.
D5-D0	R/W	00 0000	Left Channel Beep Volume Control 00 0000: Left Channel Beep Volume = 0dB 00 0001: Left Channel Beep Volume = -1dB ... 11 1110: Left Channel Beep Volume = -62dB 11 1111: Left Channel Beep Volume = -63dB

5.2.59 Book 0 / Page 0 / Register 72: Beep Generator Register 2 - 0x00 / 0x00 / 0x48 (B0_P0_R72)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Beep Generator Master Volume Control Setting 00: Left and Right Channels have independent Volume Settings 01: Left Channel Beep Volume is the same as programmed for Right Channel 10: Right Channel Beep Volume is the same as programmed for Left Channel 11: Same as 00

Book 0 / Page 0 / Register 72: Beep Generator Register 2 - 0x00 / 0x00 / 0x48 (B0_P0_R72) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	00 0000	Right Channel Beep Volume Control 00 0000: Right Channel Beep Volume = 0dB 00 0001: Right Channel Beep Volume = -1dB ... 11 1110: Right Channel Beep Volume = -62dB 11 1111: Right Channel Beep Volume = -63dB

5.2.60 Book 0 / Page 0 / Register 73: Beep Generator Register 3 - 0x00 / 0x00 / 0x49 (B0_P0_R73)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	MSB 8-bits of Beep Length - Beep Sample Length(23:16)

5.2.61 Book 0 / Page 0 / Register 74: Beep Generator Register 4 - 0x00 / 0x00 / 0x4A (B0_P0_R74)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Middle 8-bits of Beep Length - Beep Sample Length(15:8)

5.2.62 Book 0 / Page 0 / Register 75: Beep Generator Register 5 - 0x00 / 0x00 / 0x4B (B0_P0_R75)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1110 1110	LSB 8-bits of Beep Length - Beep Sample Length(23:16)

5.2.63 Book 0 / Page 0 / Register 76: Beep Sin(x) MSB - 0x00 / 0x00 / 0x4C (B0_P0_R76)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 0000	Programmed Value is Beep Sin(x)(15:8), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.64 Book 0 / Page 0 / Register 77: Beep Sin(x) LSB - 0x00 / 0x00 / 0x4D (B0_P0_R77)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1101 1000	Programmed Value is Beep Sin(x)(7:0), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.65 Book 0 / Page 0 / Register 78: Beep Cos(x) MSB - 0x00 / 0x00 / 0x4E (B0_P0_R78)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0111 1110	Programmed Value is Beep Cos(x)(15:8), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.66 Book 0 / Page 0 / Register 79: Beep Cos(x) LSB - 0x00 / 0x00 / 0x4F (B0_P0_R79)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1110 0011	Programmed Value is Beep Cos(x)(7:0), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.67 Book 0 / Page 0 / Register 80: Reserved Register - 0x00 / 0x00 / 0x50 (B0_P0_R80)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only reset value.

5.2.68 Book 0 / Page 0 / Register 81: ADC Channel Power Control - 0x00 / 0x00 / 0x51 (B0_P0_R81)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Channel ADC Power Control 0: Left Channel ADC power down 1: Left Channel ADC power up
D6	R/W	0	Right Channel ADC Power Control 0: Right Channel ADC power down 1: Right Channel ADC power up
D5-D4	R/W	00	Left Channel Digital Microphone Power Control 00: Left Channel ADC not configured for Digital Microphone 01: Left Channel ADC configured for Digital Microphone 10: Left Channel DAC Modulator output fed thru ADC CIC Filter (Loopback) 11: Reserved. Do not use.
D3-D2	R/W	00	Right Channel Digital Microphone Power Control 00: Right Channel ADC not configured for Digital Microphone 01: Right Channel ADC configured for Digital Microphone 10: Right Channel DAC Modulator output fed thru ADC CIC Filter (Loopback) 11: Reserved. Do not use.
D1-D0	R/W	00	ADC Volume Control Soft-Stepping Control 00: ADC Volume Control changes by 1 gain step per ADC Word Clock 01: ADC Volume Control changes by 1 gain step per two ADC Word Clocks 10: ADC Volume Control Soft-Stepping disabled 11: Reserved. Do not use

5.2.69 Book 0 / Page 0 / Register 82: ADC Fine Gain Volume Control - 0x00 / 0x00 / 0x52 (B0_P0_R82)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC Channel Mute Control 0: Left ADC Channel Un-Mute 1: Left ADC Channel Mute
D6-D4	R/W	000	Left ADC Channel Fine Gain Adjust 000: Left ADC Channel Fine Gain = 0 dB 111: Left ADC Channel Fine Gain = -0.1 dB 110: Left ADC Channel Fine Gain = -0.2 dB 101: Left ADC Channel Fine Gain = -0.3 dB 100: Left ADC Channel Fine Gain = -0.4 dB 001-011: Reserved. Do not use.
D3	R/W	1	Right ADC Channel Mute Control 0: Right ADC Channel Un-Mute 1: Right ADC Channel Mute
D2-D0	R/W	000	Right ADC Channel Fine Gain Adjust 000: Right ADC Channel Fine Gain = 0 dB 111: Right ADC Channel Fine Gain = -0.1 dB 110: Right ADC Channel Fine Gain = -0.2 dB 101: Right ADC Channel Fine Gain = -0.3 dB 100: Right ADC Channel Fine Gain = -0.4 dB 001-011: Reserved. Do not use.

5.2.70 Book 0 / Page 0 / Register 83: Left ADC Volume Control - 0x00 / 0x00 / 0x53 (B0_P0_R83)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 0 / Register 83: Left ADC Volume Control - 0x00 / 0x00 / 0x53 (B0_P0_R83) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0000	Left ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use. 110 1000: Left ADC Channel Volume = -12.0 dB 110 1001: Left ADC Channel Volume = -11.5 dB 110 1010: Left ADC Channel Volume = -11.0 dB … 111 1111: Left ADC Channel Volume = -0.5 dB 000 0000: Left ADC Channel Volume = 0.0 dB 000 0001: Left ADC Channel Volume = 0.5 dB ... 010 0110: Left ADC Channel Volume = 19.0 dB 010 0111: Left ADC Channel Volume = 19.5 dB 010 1000: Left ADC Channel Volume = 20.0 dB 010 1001-111 1111: Reserved. Do not use.

5.2.71 Book 0 / Page 0 / Register 84: Right ADC Volume Control - 0x00 / 0x00 / 0x54 (B0_P0_R84)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	000 0000	Right ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use. 110 1000: Right ADC Channel Volume = -12.0 dB 110 1001: Right ADC Channel Volume = -11.5 dB 110 1010: Right ADC Channel Volume = -11.0 dB … 111 1111: Right ADC Channel Volume = -0.5 dB 000 0000: Right ADC Channel Volume = 0.0 dB 000 0001: Right ADC Channel Volume = 0.5 dB ... 010 0110: Right ADC Channel Volume = 19.0 dB 010 0111: Right ADC Channel Volume = 19.5 dB 010 1000: Right ADC Channel Volume = 20.0 dB 010 1001-111 1111: Reserved. Do not use.

5.2.72 Book 0 / Page 0 / Register 85: ADC Phase Control - 0x00 / 0x00 / 0x55 (B0_P0_R85)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ADC Phase Compensation Control 1000 0000-1111 1111: Left ADC Channel Data is delayed with respect to Right ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section. 0000 0000: Left and Right ADC Channel data are not delayed with respect to each other 0000 0001-0111 1111: Right ADC Channel Data is delayed with respect to Left ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section.

5.2.73 Book 0 / Page 0 / Register 86: Left AGC Control 1 - 0x00 / 0x00 / 0x56 (B0_P0_R86)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left Channel AGC Disabled 1: Left Channel AGC Enabled

Book 0 / Page 0 / Register 86: Left AGC Control 1 - 0x00 / 0x00 / 0x56 (B0_P0_R86) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D4	R/W	000	Left Channel AGC Target Level Setting 000: Left Channel AGC Target Level = -5.5 dBFS 001: Left Channel AGC Target Level = -8.0 dBFS 010: Left Channel AGC Target Level = -10. 0dBFS 011: Left Channel AGC Target Level = -12.0 dBFS 100: Left Channel AGC Target Level = -14.0 dBFS 101: Left Channel AGC Target Level = -17.0 dBFS 110: Left Channel AGC Target Level = -20.0 dBFS 111: Left Channel AGC Target Level = -24.0 dBFS
D3-D2	R	00	Reserved. Write only reset values.
D1-D0	R/W	00	Left Channel AGC Gain Hysteresis Control 00: Left Channel AGC Gain Hysteresis is disabled 01: Left Channel AGC Gain Hysteresis is +/-0.5 dB 10: Left Channel AGC Gain Hysteresis is +/-1.0 dB 11: Left Channel AGC Gain Hysteresis is +/-1.5 dB

5.2.74 Book 0 / Page 0 / Register 87: Left AGC Control 2 - 0x00 / 0x00 / 0x57 (B0_P0_R87)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Left Channel AGC Hysteresis Setting 00: Left Channel AGC Hysteresis is 1.0 dB 01: Left Channel AGC Hysteresis is 2.0 dB 10: Left Channel AGC Hysteresis is 4.0 dB 11: Left Channel AGC Hysteresis is disabled
D5-D1	R/W	0 0000	Left Channel AGC Noise Threshold 0 0000: Left Channel AGC Noise Gate disabled 0 0001: Left Channel AGC Noise Threshold is -30 dB 0 0010: Left Channel AGC Noise Threshold is -32 dB 0 0011: Left Channel AGC Noise Threshold is -34 dB ... 1 1101: Left Channel AGC Noise Threshold is -86 dB 1 1110: Left Channel AGC Noise Threshold is -88 dB 1 1111: Left Channel AGC Noise Threshold is -90 dB
D0	R	0	Reserved. Write only reset values.

5.2.75 Book 0 / Page 0 / Register 88: Left AGC Control 3 - 0x00 / 0x00 / 0x58 (B0_P0_R88)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	111 1111	Left Channel AGC Maximum Gain Setting 000 0000: Left Channel AGC Maximum Gain = 0.0 dB 000 0001: Left Channel AGC Maximum Gain = 0.5 dB 000 0010: Left Channel AGC Maximum Gain = 1.0 dB ... 111 1110: Left Channel AGC Maximum Gain = 63.0 dB 111 1111: Left Channel AGC Maximum Gain = 63.5 dB

5.2.76 Book 0 / Page 0 / Register 89: Left AGC Attack Time - 0x00 / 0x00 / 0x59 (B0_P0_R89)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Left Channel AGC Attack Time Setting 0 0000: Left Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Left Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Left Channel AGC Attack Time = 5*32 ADC Word Clocks ... 1 1101: Left Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Left Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Left Channel AGC Attack Time = 63*32 ADC Word Clocks

Book 0 / Page 0 / Register 89: Left AGC Attack Time - 0x00 / 0x00 / 0x59 (B0_P0_R89) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	Left Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

5.2.77 Book 0 / Page 0 / Register 90: Left AGC Decay Time - 0x00 / 0x00 / 0x5A (B0_P0_R90)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Left Channel AGC Decay Time Setting 0 0000: Left Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Left Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Left Channel AGC Decay Time = 5*512 ADC Word Clocks ... 1 1101: Left Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Left Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Left Channel AGC Decay Time = 63*512 ADC Word Clocks
D2-D0	R/W	000	Left Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

5.2.78 Book 0 / Page 0 / Register 91: Left AGC Noise Debounce - 0x00 / 0x00 / 0x5B (B0_P0_R91)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D0	R/W	0 0000	Left Channel AGC Noise Debounce Time Setting 0 0001: Left Channel AGC Noise Debounce Time = 0 0 0010: Left Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Left Channel AGC Noise Debounce Time = 8 ADC Word Clocks ... 0 1010: Left Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Left Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Left Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Left Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Left Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Left Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Left Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

5.2.79 Book 0 / Page 0 / Register 92: Left AGC Signal Debounce - 0x00 / 0x00 / 0x5C (B0_P0_R92)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.

Book 0 / Page 0 / Register 92: Left AGC Signal Debounce - 0x00 / 0x00 / 0x5C (B0_P0_R92) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	Left Channel AGC Signal Debounce Time Setting 0001: Left Channel AGC Signal Debounce Time = 0 0010: Left Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Left Channel AGC Signal Debounce Time = 8 ADC Word Clocks ... 1001: Left Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Left Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Left Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Left Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Left Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Left Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Left Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

5.2.80 Book 0 / Page 0 / Register 93: Left AGC Gain - 0x00 / 0x00 / 0x5D (B0_P0_R93)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Left Channel AGC Gain 1110 1000: Left Channel AGC Gain = -12.0dB 1110 1001: Left Channel AGC Gain = -11.5dB 1110 1010: Left Channel AGC Gain = -11.0dB ... 0000 0000: Left Channel AGC Gain = 0.0dB ... 0111 1101: Left Channel AGC Gain = 62.5dB 0111 1110: Left Channel AGC Gain = 63.0dB 0111 1111: Left Channel AGC Gain = 63.5dB

5.2.81 Book 0 / Page 0 / Register 94: Right AGC Control 1 - 0x00 / 0x00 / 0x5E (B0_P0_R94)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right Channel AGC Disabled 1: Right Channel AGC Enabled
D6-D4	R/W	000	Right Channel AGC Target Level Setting 000: Right Channel AGC Target Level = -5.5 dBFS 001: Right Channel AGC Target Level = -8.0 dBFS 010: Right Channel AGC Target Level = -10.0 dBFS 011: Right Channel AGC Target Level = -12.0 dBFS 100: Right Channel AGC Target Level = -14.0 dBFS 101: Right Channel AGC Target Level = -17.0 dBFS 110: Right Channel AGC Target Level = -20.0 dBFS 111: Right Channel AGC Target Level = -24.0 dBFS
D3-D2	R	00	Reserved. Write only reset values.
D1-D0	R/W	00	Right Channel AGC Gain Hysteresis Control 00: Right Channel AGC Gain Hysteresis is disabled 01: Right Channel AGC Gain Hysteresis is +-0.5 dB 10: Right Channel AGC Gain Hysteresis is +-1.0 dB 11: Right Channel AGC Gain Hysteresis is +-1.5 dB

5.2.82 Book 0 / Page 0 / Register 95: Right AGC Control 2 - 0x00 / 0x00 / 0x5F (B0_P0_R95)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Right Channel AGC Hysteresis Setting 00: Right Channel AGC Hysteresis is 1.0dB 01: Right Channel AGC Hysteresis is 2.0dB 10: Right Channel AGC Hysteresis is 4.0dB 11: Right Channel AGC Hysteresis is disabled

Book 0 / Page 0 / Register 95: Right AGC Control 2 - 0x00 / 0x00 / 0x5F (B0_P0_R95) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D1	R/W	00 000	Right Channel AGC Noise Threshold 0 0000: Right Channel AGC Noise Gate disabled 0 0001: Right Channel AGC Noise Threshold is -30dB 0 0010: Right Channel AGC Noise Threshold is -32dB 0 0011: Right Channel AGC Noise Threshold is -34dB ... 1 1101: Right Channel AGC Noise Threshold is -86dB 1 1110: Right Channel AGC Noise Threshold is -88dB 1 1111: Right Channel AGC Noise Threshold is -90dB
D0	R	0	Reserved. Write only reset values.

5.2.83 Book 0 / Page 0 / Register 96: Right AGC Control 3 - 0x00 / 0x00 / 0x60 (B0_P0_R96)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D0	R/W	111 1111	Right Channel AGC Maximum Gain Setting 000 0000: Right Channel AGC Maximum Gain = 0.0dB 000 0001: Right Channel AGC Maximum Gain = 0.5dB 000 0010: Right Channel AGC Maximum Gain = 1.0dB ... 111 1110: Right Channel AGC Maximum Gain = 63.0dB 111 1111: Right Channel AGC Maximum Gain = 63.5dB

5.2.84 Book 0 / Page 0 / Register 97: Right AGC Attack Time - 0x00 / 0x00 / 0x61 (B0_P0_R97)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0000 0	Right Channel AGC Attack Time Setting 0 0000: Right Channel AGC Attack Time = 1*32 ADC Word Clocks 0 0001: Right Channel AGC Attack Time = 3*32 ADC Word Clocks 0 0010: Right Channel AGC Attack Time = 5*32 ADC Word Clocks ... 1 1101: Right Channel AGC Attack Time = 59*32 ADC Word Clocks 1 1110: Right Channel AGC Attack Time = 61*32 ADC Word Clocks 1 1111: Right Channel AGC Attack Time = 63*32 ADC Word Clocks
D2-D0	R/W	000	Right Channel AGC Attack Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

5.2.85 Book 0 / Page 0 / Register 98: Right AGC Decay Time - 0x00 / 0x00 / 0x62 (B0_P0_R98)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R/W	0 0000	Right Channel AGC Decay Time Setting 0 0000: Right Channel AGC Decay Time = 1*512 ADC Word Clocks 0 0001: Right Channel AGC Decay Time = 3*512 ADC Word Clocks 0 0010: Right Channel AGC Decay Time = 5*512 ADC Word Clocks ... 1 1101: Right Channel AGC Decay Time = 59*512 ADC Word Clocks 1 1110: Right Channel AGC Decay Time = 61*512 ADC Word Clocks 1 1111: Right Channel AGC Decay Time = 63*512 ADC Word Clocks

Book 0 / Page 0 / Register 98: Right AGC Decay Time - 0x00 / 0x00 / 0x62 (B0_P0_R98) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	Right Channel AGC Decay Time Scale Factor Setting 000: Scale Factor = 1 001: Scale Factor = 2 010: Scale Factor = 4 ... 101: Scale Factor = 32 110: Scale Factor = 64 111: Scale Factor = 128

5.2.86 Book 0 / Page 0 / Register 99: Right AGC Noise Debounce - 0x00 / 0x00 / 0x63 (B0_P0_R99)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4-D0	R/W	0 0000	Right Channel AGC Noise Debounce Time Setting 0 0001: Right Channel AGC Noise Debounce Time = 0 0 0010: Right Channel AGC Noise Debounce Time = 4 ADC Word Clocks 0 0011: Right Channel AGC Noise Debounce Time = 8 ADC Word Clocks ... 0 1010: Right Channel AGC Noise Debounce Time = 2048 ADC Word Clocks 0 1011: Right Channel AGC Noise Debounce Time = 4096 ADC Word Clocks 0 1100: Right Channel AGC Noise Debounce Time = 2*4096 ADC Word Clocks 0 1101: Right Channel AGC Noise Debounce Time = 3*4096 ADC Word Clocks ... 1 1101: Right Channel AGC Noise Debounce Time = 19*4096 ADC Word Clocks 1 1110: Right Channel AGC Noise Debounce Time = 20*4096 ADC Word Clocks 1 1111: Right Channel AGC Noise Debounce Time = 21*4096 ADC Word Clocks

5.2.87 Book 0 / Page 0 / Register 100: Right AGC Signal Debounce - 0x00 / 0x00 / 0x64 (B0_P0_R100)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3-D0	R/W	0000	Right Channel AGC Signal Debounce Time Setting 0001: Right Channel AGC Signal Debounce Time = 0 0010: Right Channel AGC Signal Debounce Time = 4 ADC Word Clocks 0011: Right Channel AGC Signal Debounce Time = 8 ADC Word Clocks ... 1001: Right Channel AGC Signal Debounce Time = 1024 ADC Word Clocks 1010: Right Channel AGC Signal Debounce Time = 2048 ADC Word Clocks 1011: Right Channel AGC Signal Debounce Time = 2*2048 ADC Word Clocks 1100: Right Channel AGC Signal Debounce Time = 3*2048 ADC Word Clocks 1101: Right Channel AGC Signal Debounce Time = 4*2048 ADC Word Clocks 1110: Right Channel AGC Signal Debounce Time = 5*2048 ADC Word Clocks 1111: Right Channel AGC Signal Debounce Time = 6*2048 ADC Word Clocks

5.2.88 Book 0 / Page 0 / Register 101: Right AGC Gain - 0x00 / 0x00 / 0x65 (B0_P0_R101)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Right Channel AGC Gain 1110 1000: Left Channel AGC Gain = -12.0dB 1110 1001: Left Channel AGC Gain = -11.5dB 1110 1010: Left Channel AGC Gain = -11.0dB ... 0000 0000: Left Channel AGC Gain = 0.0dB ... 0111 1101: Left Channel AGC Gain = 62.5dB 0111 1110: Left Channel AGC Gain = 63.0dB 0111 1111: Left Channel AGC Gain = 63.5dB

5.2.89 Book 0 / Page 0 / Register 102: ADC DC Measurement Control Register 1 - 0x00 / 0x00 /

0x66 (B0_P0_R102)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DC Measurement Mode disabled for Left ADC Channel 1: DC Measurement Mode enabled for Left ADC Channel
D6	R/W	0	0: DC Measurement Mode disabled for Right ADC Channel 1: DC Measurement Mode enabled for Right ADC Channel
D5	R/W	0	0: DC Measurement is done using 1st order moving average filter with averaging of 2^D 1: DC Measurement is done with 1sr order Low-pass IIR filter with coefficients as a function of D
D4-D0	R/W	0 0000	DC Measurement D setting 0 0000: Reserved. Do not use 0 0001: DC Measurement D parameter = 1 0 0010: DC Measurement D parameter = 2 .. 1 0011: DC Measurement D parameter = 19 1 0100: DC Measurement D parameter = 20 1 0101-1 1111: Reserved. Do not use

5.2.90 Book 0 / Page 0 / Register 103: ADC DC Measurement Control Register 2 - 0x00 / 0x00 / 0x67 (B0_P0_R103)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6	R/W	0	0: Left and Right Channel DC measurement result update enabled 1: Left and Right Channel DC measurement result update disabled i.e. new results will be updated while old results are being read
D5	R/W	0	0: For IIR based DC measurement, measurement value is the instantaneous output of IIR filter 1: For IIR based DC measurement, the measurement value is updated before periodic clearing of IIR filter
D4-D0	R/W	0 0000	IIR based DC Measurement, averaging time setting 0 0000: Infinite average is used 0 0001: Averaging time is 2^1 ADC Modulator clocks 0 0010: Averaging time is 2^2 ADC Modulator clocks ... 1 0011: Averaging time is 2^19 ADC Modulator clocks 1 0100: Averaging time is 2^20 ADC Modulator clocks 1 0101-1 1111: Reserved. Do not use

5.2.91 Book 0 / Page 0 / Register 104: Left Channel DC Measurement Output Register 1 (MSB Byte) - 0x00 / 0x00 / 0x68 (B0_P0_R104)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Left Channel DC Measurement Output (23:16)

5.2.92 Book 0 / Page 0 / Register 105: Left Channel DC Measurement Output Register 2 (Middle Byte) - 0x00 / 0x00 / 0x69 (B0_P0_R105)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Left Channel DC Measurement Output (15:8)

5.2.93 Book 0 / Page 0 / Register 106: Left Channel DC Measurement Output Register 3 (LSB Byte) - 0x00 / 0x00 / 0x6A (B0_P0_R106)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Left Channel DC Measurement Output (7:0)

5.2.94 Book 0 / Page 0 / Register 107: Right Channel DC Measurement Output Register 1 (MSB

Byte) - 0x00 / 0x00 / 0x6B (B0_P0_R107)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Right Channel DC Measurement Output (23:16)

5.2.95 Book 0 / Page 0 / Register 108: Right Channel DC Measurement Output Register 2 (Middle Byte) - 0x00 / 0x00 / 0x6C (B0_P0_R108)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Right Channel DC Measurement Output (15:8)

5.2.96 Book 0 / Page 0 / Register 109: Right Channel DC Measurement Output Register 3 (LSB Byte) - 0x00 / 0x00 / 0x6D (B0_P0_R109)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Right Channel DC Measurement Output (7:0)

5.2.97 Book 0 / Page 0 / Register 110-114: Reserved Registers - 0x00 / 0x00 / 0x6E-0x72 (B0_P0_R110-114)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.2.98 Book 0 / Page 0 / Register 115: I2C Interface Miscellaneous Control - 0x00 / 0x00 / 0x73 (B0_P0_R115)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	I2C General Call Address Configuration 0: I2C General Call Address will be ignored 1: I2C General Call Address accepted
D4-D0	R	0 0000	Reserved. Write only reset values.

5.2.99 Book 0 / Page 0 / Register 116-126: Reserved Registers - 0x00 / 0x00 / 0x74-0x7E (B0_P0_R116-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.2.100 Book 0 / Page 0 / Register 127: Book Selection Register - 0x00 / 0x00 / 0x7F (B0_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

5.3 Book 0 Page 1

5.3.1 Book 0 / Page 1 / Register 0: Page Select Register - 0x00 / 0x01 / 0x00 (B0_P1_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

5.3.2 Book 0 / Page 1 / Register 1: Power Configuration Register - 0x00 / 0x01 / 0x01 (B0_P1_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R/W	1	0: Disable weak connection of AVDD with DVDD 1: AVDD is weakly connected to DVDD. Use when DVDD is powered-up and AVDD is not externally powered-up.
D2	R/W	1	0: All the external analog supplies are available. 1: All the external analog supplies are not available.
D1-D0	R	00	Reserved. Write only reset values.

5.3.3 Book 0 / Page 1 / Register 2: Reserved Register - 0x00 / 0x01 / 0x02 (B0_P1_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.4 Book 0 / Page 1 / Register 3: Left DAC PowerTune Configuration Register - 0x00 / 0x01 / 0x03 (B0_P1_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D2	R/W	0 00	Left DAC PTM Control 000: Left DAC in mode PTM_P3, PTM_P4 001: Left DAC in mode PTM_P2 010: Left DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only reset values.

5.3.5 Book 0 / Page 1 / Register 4: Right DAC PowerTune Configuration Register - 0x00 / 0x01 / 0x04 (B0_P1_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4-D2	R/W	0 00	Right DAC PTM Control 000: Right DAC in mode PTM_P3, PTM_P4 001: Right DAC in mode PTM_P2 010: Right DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only reset values.

5.3.6 Book 0 / Page 1 / Register 5-7: Reserved Registers - 0x00 / 0x01 / 0x05-0x07 (B0_P1_R5-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.7 Book 0 / Page 1 / Register 8: Common Mode Register - 0x00 / 0x01 / 0x08 (B0_P1_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Soft-stepping of all the PGA are enabled for DAC channel. 1: Soft-stepping of all the PGA are disabled for DAC channel.
D6	R/W	0	0: Normal Mode 1: Soft-stepping time for all the PGA of DAC channel is doubled.
D5	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 8: Common Mode Register - 0x00 / 0x01 / 0x08 (B0_P1_R8) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D3	R/W	00	00: Output Common Mode for HP (valid if the cap-coupled mode is enabled) Output Drivers = Input Common Mode 01: Output Common Mode for HP (valid if the cap-coupled mode is enabled) Output Drivers = 1.25V 10: Output Common Mode for HP (valid if the cap-coupled mode is enabled) Output Drivers = 1.5V 11: Output Common Mode for HP (valid if the cap-coupled mode is enabled) Output Drivers = 1.65V
D2	R/W	0	0: Input Common Mode for full-chip (ADC and All Output Drivers except Receiver Output) = 0.9V 1: Input Common Mode for full-chip (ADC and All Output Drivers except Receiver Output) = 0.75V
D1-D0	R/W	00	00: Output Common Mode for REC Output Drivers = Input Common Mode 01: Output Common Mode for REC Output Drivers = 1.25V 10: Output Common Mode for REC Output Drivers = 1.5V 11: Output Common Mode for REC Output Drivers = 1.65V

5.3.8 Book 0 / Page 1 / Register 9: Headphone Output Driver Control - 0x00 / 0x01 / 0x09 (B0_P1_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D5	R/W	00	00: Headphone Driver Output Stage is 100%. 01: Headphone Driver Output Stage is 75%. 10: Headphone Driver Output Stage is 50%. 11: Headphone Driver Output Stage is 25%.
D4	R	1	Reserved. Write only reset values.
D3-D1	R/W	000	Debounce Programming for Glitch Rejection during Short Circuit Detection 000: 0us 001: 8us 010: 16us 011: 32us 100: 64us 101: 128us 110: 256us 111: 512us
D0	R/W	0	HPL and HPR Over Current Response Control 0: If Over Current Detected Limit the current delivered by HPL/HPR 1: If Over Current Detected Power-Down the HPL/HPR driver.

5.3.9 Book 0 / Page 1 / Register 10: Receiver Output Driver Control - 0x00 / 0x01 / 0x0A (B0_P1_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0001	Reserved. Write only reset values.
D3-D1	R/W	000	Debounce Programming for Glitch Rejection during Short Circuit Detection 000: 0us 001: 8us 010: 16us 011: 32us 100: 64us 101: 128us 110: 256us 111: 512us
D0	R/W	0	Receiver RECP and RECM Over-Current Response Control 0: If Over-Current Detected Limit the current. 1: If Over-Current Detected Power-Down the RECP/RECM driver

5.3.10 Book 0 / Page 1 / Register 11: Headphone Output Driver De-pop Control - 0x00 / 0x01 /

0x0B (B0_P1_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Headphone De-Pop Due to Input Offset Control (Note: Headphone depop control should only be used in unipolar configuration. This control should be disabled in Ground-Centered Headphone configuration.) 00: Disable 01: Enable (Duration = 50ms) 10: Enable (Duration = 100ms) 11: Enable (Duration = 200ms)
D5-D2	R/W	00 00	Headphone Output Driver De-Pop Control (Note: Headphone depop control should only be used in unipolar configuration. This control should be disabled in Ground-Centered Headphone configuration.) 0000: Disabled 0001: Enabled (Duration = 0.500*RC) 0010: Enabled (Duration = 0.625*RC) 0011: Enabled (Duration = 0.750*RC} 0100: Enabled (Duration = 0.875*RC) 0101: Enabled (Duration = 1.000*RC) 0110: Enabled (Duration = 2.000*RC) 0111: Enabled (Duration = 3.000*RC) 1000: Enabled (Duration = 4.000*RC) 1001: Enabled (Duration = 5.000*RC) 1010: Enabled (Duration = 6.000*RC) 1011: Enabled (Duration = 7.000*RC) 1100: Enabled (Duration = 8.000*RC) 1101: Enabled (Duration = 16.000*RC - do not use for Rchg=25K) 1110: Enabled (Duration = 24.000*RC - do not use for Rchg=25K) 1111: Enabled (Duration = 32.000*RC - do not use for Rchg=25K)
D1-D0	R/W	00	Headphone De-Pop Scheme Duration Based on RC Delay Control 00: Internal R = 25K typical and C is external cap.assumed to be 47uF 01: Internal R = 6K typical and C is external cap. assumed to be 47uF 10: Internal R = 2K typical and C is external cap. assumed to be 47uF 11: Reserved.

5.3.11 Book 0 / Page 1 / Register 12: Receiver Output Driver De-Pop Control - 0x00 / 0x01 / 0x0C (B0_P1_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Receiver De-Pop Due to Input Offset Control 00: Disable 01: Enable (Duration = 50ms) 10: Enable (Duration = 100ms) 11: Enable (Duration = 200ms)
D5-D2	R/W	00 00	Receiver Output Driver De-Pop Control 0000: Disabled 0001: Enabled (Duration = 0.500*RC) 0010: Enabled (Duration = 0.625*RC) 0011: Enabled (Duration = 0.750*RC} 0100: Enabled (Duration = 0.875*RC) 0101: Enabled (Duration = 1.000*RC) 0110: Enabled (Duration = 2.000*RC) 0111: Enabled (Duration = 3.000*RC) 1000: Enabled (Duration = 4.000*RC) 1001: Enabled (Duration = 5.000*RC) 1010: Enabled (Duration = 6.000*RC) 1011: Enabled (Duration = 7.000*RC) 1100: Enabled (Duration = 8.000*RC) 1101: Enabled (Duration = 16.000*RC - do not use for Rchg=25K) 1110: Enabled (Duration = 24.000*RC - do not use for Rchg=25K) 1111: Enabled (Duration = 32.000*RC - do not use for Rchg=25K)
D1-D0	R/W	00	Receiver De-Pop Scheme Duration Based on RC Delay Control 00: Internal R = 25K typical and C is external cap.assumed to be 47uF 01: Internal R = 6K typical and C is external cap. assumed to be 47uF 10: Internal R = 2K typical and C is external cap. assumed to be 47uF 11: Reserved.

5.3.12 Book 0 / Page 1 / Register 13-16: Reserved Registers - 0x00 / 0x01 / 0x0D-0x10

(B0_P1_R13-16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.13 Book 0 / Page 1 / Register 17: Mixer Amplifier Control - 0x00 / 0x01 / 0x11 (B0_P1_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN1L to Mixer Amplifier Left (MAL) Routing Control 0: IN1L input for high-impedance mode is not routed to MAL 1: IN1L input for high-impedance mode is routed to MAL
D4	R/W	0	IN1R to Mixer Amplifier Right (MAR) Routing Control 0: IN1R input for high-impedance mode is not routed to MAR 1: IN1R input for high-impedance mode is routed to MAR
D3	R/W	0	Mixer Amp Left (MAL) Power Control 0: MAL is powered down 1: MAL is powered up
D2	R/W	0	Mixer Amp Right (MAR) Power Control 0: MAR is powered down 1: MAR is powered up
D1-D0	R	00	Reserved. Write only reset values.

5.3.14 Book 0 / Page 1 / Register 18: Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control - 0x00 / 0x01 / 0x12 (B0_P1_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.

Book 0 / Page 1 / Register 18: Left ADC PGA to Left Mixer Amplifier (MAL) Volume Control - 0x00 / 0x01 / 0x12 (B0_P1_R18) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1111	Left ADC PGA Output Routed to Left Mixer Amplifier (MAL) Volume Control: 00 0000: Volume Control = 0.0 dB 00 0001: Volume Control = -0.4 dB 00 0010: Volume Control = -0.9 dB 00 0011: Volume Control = -1.3 dB 00 0100: Volume Control = -1.8 dB 00 0101: Volume Control = -2.3 dB 00 0110: Volume Control = -2.9 dB 00 0111: Volume Control = -3.3 dB 00 1000: Volume Control = -3.9 dB 00 1001: Volume Control = -4.3 dB 00 1010: Volume Control = -4.8 dB 00 1011: Volume Control = -5.2 dB 00 1100: Volume Control = -5.8 dB 00 1101: Volume Control = -6.3 dB 00 1110: Volume Control = -6.6 dB 00 1111: Volume Control = -7.2 dB 01 0000: Volume Control = -7.8 dB 01 0001: Volume Control = -8.2 dB 01 0010: Volume Control = -8.5 dB 01 0011: Volume Control = -9.3 dB 01 0100: Volume Control = -9.7 dB 01 0101: Volume Control = -10.1 dB 01 0110: Volume Control = -10.6 dB 01 0111: Volume Control = -11.0 dB 01 1000: Volume Control = -11.5 dB 01 1001: Volume Control = -12.0 dB 01 1010: Volume Control = -12.6 dB 01 1011: Volume Control = -13.2 dB 01 1100: Volume Control = -13.8 dB 01 1101: Volume Control = -14.5 dB 01 1110: Volume Control = -15.3 dB 01 1111: Volume Control = -16.1 dB 10 0000: Volume Control = -17.0 dB 10 0001: Volume Control = -18.1 dB 10 0010: Volume Control = -19.2 dB 10 0011: Volume Control = -20.6 dB 10 0100: Volume Control = -22.1 dB 10 0101: Volume Control = -24.1 dB 10 0110: Volume Control = -26.6 dB 10 0111: Volume Control = -30.1 dB 10 1000: Volume Control = -36.1 dB 10 1001 - 11 1110: Reserved 11 1111: Left ADC PGA output is not routed to Left Mixer Amplifier (MAL)

5.3.15 Book 0 / Page 1 / Register 19: Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control - 0x00 / 0x01 / 0x13 (B0_P1_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Use the Right ADC PGA output routing setting to MAR as defined in this Register D5-D0 1: Use the Right ADC PGA output routing setting to MAR same as defined for Left ADC PGA in Page 1 / Register 18, bits D5-D0 (previous register)
D6	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 19: Right ADC PGA to Right Mixer Amplifier (MAR) Volume Control - 0x00 / 0x01 / 0x13 (B0_P1_R19) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1111	Right ADC PGA Output Routed to Right Mixer Amplifier Volume Control: 00 0000: Volume Control = 0.0 dB 00 0001: Volume Control = -0.4 dB 00 0010: Volume Control = -0.9 dB 00 0011: Volume Control = -1.3 dB 00 0100: Volume Control = -1.8 dB 00 0101: Volume Control = -2.3 dB 00 0110: Volume Control = -2.9 dB 00 0111: Volume Control = -3.3 dB 00 1000: Volume Control = -3.9 dB 00 1001: Volume Control = -4.3 dB 00 1010: Volume Control = -4.8 dB 00 1011: Volume Control = -5.2 dB 00 1100: Volume Control = -5.8 dB 00 1101: Volume Control = -6.3 dB 00 1110: Volume Control = -6.6 dB 00 1111: Volume Control = -7.2 dB 01 0000: Volume Control = -7.8 dB 01 0001: Volume Control = -8.2 dB 01 0010: Volume Control = -8.5 dB 01 0011: Volume Control = -9.3 dB 01 0100: Volume Control = -9.7 dB 01 0101: Volume Control = -10.1 dB 01 0110: Volume Control = -10.6 dB 01 0111: Volume Control = -11.0 dB 01 1000: Volume Control = -11.5 dB 01 1001: Volume Control = -12.0 dB 01 1010: Volume Control = -12.6 dB 01 1011: Volume Control = -13.2 dB 01 1100: Volume Control = -13.8 dB 01 1101: Volume Control = -14.5 dB 01 1110: Volume Control = -15.3 dB 01 1111: Volume Control = -16.1 dB 10 0000: Volume Control = -17.0 dB 10 0001: Volume Control = -18.1 dB 10 0010: Volume Control = -19.2 dB 10 0011: Volume Control = -20.6 dB 10 0100: Volume Control = -22.1 dB 10 0101: Volume Control = -24.1dB 10 0110: Volume Control = -26.6dB 10 0111: Volume Control = -30.1dB 10 1000: Volume Control = -36.1dB 10 1001 - 11 1110: Reserved 11 1111: Right ADC PGA output is not routed to Right Mixer Amplifer (MAR)

5.3.16 Book 0 / Page 1 / Register 20-21: Reserved Registers - 0x00 / 0x01 / 0x14-0x15 (B0_P1_R20-21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.17 Book 0 / Page 1 / Register 22: Lineout Amplifier Control 1 - 0x00 / 0x01 / 0x16 (B0_P1_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC to LOL Driver Routing Control: 0: Left DAC is not routed to LOL driver. 1: Left DAC M-terminal is routed to LOL driver.
D6	R/W	0	Right DAC to LOR Driver Routing Control: 0: Right DAC is not routed to LOR driver. 1: Right DAC M-terminal is routed to LOR driver.

Book 0 / Page 1 / Register 22: Lineout Amplifier Control 1 - 0x00 / 0x01 / 0x16 (B0_P1_R22) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	Right DAC to LOL Driver Routing Control: 0: Right DAC is not routed to LOL driver. 1: Right DAC P-terminal is routed to LOL driver.(This is provided to support differential DAC output to LO and should be done only when B0_P1_R22_D6=1 and B0_P1_R27_D4=0)
D4-D3	R	0 0	Reserved. Write only reset values.
D2	R/W	0	LOL to LOR Driver Routing Control: 0: LOL output not routed to LOR driver. 1: LOL output routed to LOR driver.
D1	R/W	0	LOL Output Driver Power Control: 0: LOL output driver power-down 1: LOL output driver power-up
D0	R/W	0	LOR Output Driver Power Control: 0: LOR output driver power-down 1: LOR output driver power-up

5.3.18 Book 0 / Page 1 / Register 23: Lineout Amplifier Control 2 - 0x00 / 0x01 / 0x17 (B0_P1_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier to LOL Driver Routing Control: 0: MAL output is not routed to LOL driver. 1: MAL output is routed to LOL driver.
D6	R/W	0	Right Mixer Amplifier to LOR Driver Routing Control: 0: MAR output is not routed to LOR driver. 1: MAR output is routed to LOR driver.
D5	R	0	Reserved. Write only reset values.
D4-D3	R/W	0 0	IN1L Input to LOL Driver Routing and Gain Control: 00: IN1L input is not routed to LOL driver. 01: IN1L input is routed to LOL driver with gain = 0dB 10: IN1L input is routed to LOL driver with gain = -6dB 11: IN1L input is routed to LOL driver with gain = -12dB
D2	R	0	Reserved. Write only reset values.
D1-D0	R/W	00	IN1R Input to LOR Driver Routing and Gain Control: 00: IN1R input is not routed to LOR driver. 01: IN1R input is routed to LOR driver with gain = 0dB 10: IN1R input is routed to LOR driver with gain = -6dB 11: IN1R input is routed to LOR driver with gain = -12dB

5.3.19 Book 0 / Page 1 / Register 24-26: Reserved - 0x00 / 0x01 / 0x18-0x1A (B0_P1_R24-26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.20 Book 0 / Page 1 / Register 27: Headphone Amplifier Control 1 - 0x00 / 0x01 / 0x1B (B0_P1_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier to HPL Driver Routing Control: 0: MAL output is not routed to HPL driver. 1: MAL output is routed to HPL driver.
D6	R/W	0	Right Mixer Amplifier to HPL Driver Routing Control: 0: MAR output is not routed to HPR driver. 1: MAR output is routed to HPR driver.
D5	R/W	0	Left DAC to HPL Driver Routing Control: 0: Left DAC is not routed to HPL driver. 1: Left DAC is routed to HPL driver.

Book 0 / Page 1 / Register 27: Headphone Amplifier Control 1 - 0x00 / 0x01 / 0x1B (B0_P1_R27) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R/W	0	Right DAC to HPR Driver Routing Control: 0: Right DAC is not routed to HPR driver. 1: Right DAC is routed to HPR driver.
D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Left DAC to HPR Driver Routing Control: 0: Left DAC is not routed to HPR driver. 1: Left DAC M-terminal is routed to HPR driver. (This is provided to support differential DAC output for HP and should be done only when B0_P1_R27_D5=1 and B0_P1_R22_D7=0)
D1	R/W	0	HPL Output Driver Power Control: 0: HPL output driver is powered down 1: HPL output driver is powered up
D0	R/W	0	HPR Output Driver Power Control: 0: HPR output driver is powered down 1: HPR output driver is powered up

5.3.21 Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to HPL Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB

Book 0 / Page 1 / Register 28: Headphone Amplifier Control 2 - 0x00 / 0x01 / 0x1C (B0_P1_R28) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -33.1 dB 100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to HPL Driver (Default)

5.3.22 Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOR Output to HPR Driver Master Volume Control 0: LOL to HPL and LOR to HPR Volume are Independently Controlled 1: LOL to HPL and LOR to HPR Volume are Both Controlled by page 1 / register 28, bits D6-D0

Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to HPR Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB

Book 0 / Page 1 / Register 29: Headphone Amplifier Control 3 - 0x00 / 0x01 / 0x1D (B0_P1_R29) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -33.1 dB 100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to HPR Driver (Default)

5.3.23 Book 0 / Page 1 / Register 30: Reserved Register - 0x00 / 0x01 / 0x1E (B0_P1_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.24 Book 0 / Page 1 / Register 31: HPL Driver Volume Control - 0x00 / 0x01 / 0x1F

(B0_P1_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Headphone Configuration: 0: Headphone driver is configured for unipolar/cap-coupled mode. 1: Headphone driver is configured for ground-centered mode. B0_P1_R8_D[4:3] should be set to "00".
D6	R	0	Reserved. Write only reset values.
D5-D0	R/W	11 1001	HPL Driver Volume Control: 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB 00 0011: Volume Control = 3 dB 00 0100: Volume Control = 4 dB 00 0101: Volume Control = 5 dB 00 0110: Volume Control = 6 dB 00 0111: Volume Control = 7 dB 00 1000: Volume Control = 8 dB 00 1001: Volume Control = 9 dB 00 1010: Volume Control = 10 dB 00 1011: Volume Control = 11 dB 00 1100: Volume Control = 12 dB 00 1101: Volume Control = 13 dB 00 1110: Volume Control = 14 dB 001111 - 111111: Reserved. Do not use.

5.3.25 Book 0 / Page 1 / Register 32: HPR Driver Volume Control - 0x00 / 0x01 / 0x20 (B0_P1_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Headphone Right (HPR) Driver Configuration: 0: Use the HPR driver volume setting as defined in B0_P1_R32_D[5:0]. (Only to be used in unipolar/cap-coupled configuration) 1: Use the HPR driver volume setting as defined as same as the HPL volume of B0_P1_R31_D[5:0].
D6	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 32: HPR Driver Volume Control - 0x00 / 0x01 / 0x20 (B0_P1_R32) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1001	HPR Driver Volume Control (Only used in Unipolar/Cap-Coupled Configuration): 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB 00 0011: Volume Control = 3 dB 00 0100: Volume Control = 4 dB 00 0101: Volume Control = 5 dB 00 0110: Volume Control = 6 dB 00 0111: Volume Control = 7 dB 00 1000: Volume Control = 8 dB 00 1001: Volume Control = 9 dB 00 1010: Volume Control = 10 dB 00 1011: Volume Control = 11 dB 00 1100: Volume Control = 12 dB 00 1101: Volume Control = 13 dB 00 1110: Volume Control = 14 dB 001111 - 111111: Reserved. Do not use.

5.3.26 Book 0 / Page 1 / Register 33: Charge Pump Control 1 - 0x00 / 0x01 / 0x21 (B0_P1_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	001	Reserved. Write only reset values.
D4-D1	R/W	0 100	0000: Charge Pump Clock Divide = 16 0001: Charge Pump Clock Divide = 1 0010: Charge Pump Clock Divide = 2 0011: Charge Pump Clock Divide = 3 0100: Charge Pump Clock Divide = 4 (Default) … 1111: Charge Pump Clock Divide = 15
D0	R/W	0	Reserved. Write only reset values.

5.3.27 Book 0 / Page 1 / Register 34: Charge Pump Control 2 - 0x00 / 0x01 / 0x22 (B0_P1_R34)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: AVSS_SENSE is buffered when used to set the output common-mode 01: AVSS_SENSE is not buffered when used to set the output common-mode 10: Internal ground is used to set the output common-mode 11: Reserved.
D5	R/W	1	Reserved. Write only reset values.
D4-D2	R/W	1 11	Charge Pump Power Configuration 000: Charge Pump Configuration is for 1/8 Peak Load Current 001: Charge Pump Configuration is for 2/8 x Peak Load Current .. 110: Charge Pump Configuration is for 7/8 x Peak Load Current 111: Charge Pump Configuration is for 1x Peak Load Current
D1-D0	R/W	10	DC Offset Correction Configuration for Ground Centered Mode of Headphone Driver 00: DC Offset Correction is disabled 01: Reserved 10: DC Offset Correction is enabled for all signal routings which are enabled for HPL and HPR 11: DC Offset Correction for all possible signal routings for HPL and HPR

5.3.28 Book 0 / Page 1 / Register 35: Charge Pump Control 3 - 0x00 / 0x01 / 0x23 (B0_P1_R35)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	Dynamic Offset Calibration 0: Dynamic offset calibration is not enabled for ground-centered headphone. 1: Dynamic offset calibration is enabled for ground-centered headphone. This mode should be enabled before the ground-centered headphone is powered up for the first time.
D4-D2	R	1 00	Reserved. Write only reset values.
D1-D0	R/W	00	Charge-pump Power Control 00: Charge-Pump auto-power-up when ground-centered headphone is powered-up 01: Charge-Pump forced power-up 10: Charge-Pump forced power-down 11: Reserved. Do not use.

5.3.29 Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to RECP Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 36: Receiver Amplifier Control 1 - 0x00 / 0x01 / 0x24 (B0_P1_R36) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to RECP Driver (Default)

5.3.30 Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOR Output to RECM Driver Master Volume Control 0: LOL to RECP and LOR to RECM Volume are Independently Controlled 1: LOL to RECP and LOR to RECM Volume are Both Controlled by B0_P1_R36_D[6:0]. Should only be used when load of receiver amplifier is differential.

Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to RECM Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 37: Receiver Amplifier Control 2 - 0x00 / 0x01 / 0x25 (B0_P1_R37) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to RECM Driver (Default)

5.3.31 Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	IN1L Input Routed to RECP Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 38: Receiver Amplifier Control 3 - 0x00 / 0x01 / 0x26 (B0_P1_R38) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: IN1L Input Not Routed to RECP Driver (Default)

5.3.32 Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Input to RECP and IN1R Input to RECM Driver Master Volume Control 0: IN1L to RECP and IN1R to RECM Volume are Independently Controlled 1: IN1L to RECP and INI1R to RECM Volume are Both Controlled by B0_P1_R38_D[6:0]. Should only be used when load of receiver amplifier is differential.

Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	IN1R Input Routed to RECM Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 39: Receiver Amplifier Control 4 - 0x00 / 0x01 / 0x27 (B0_P1_R39) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: IN1R Input Not Routed to RECM Driver (Default)

5.3.33 Book 0 / Page 1 / Register 40: Receiver Amplifier Control 5 - 0x00 / 0x01 / 0x28 (B0_P1_R40)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	RECP Output Driver Power Control 0: RECP Output Driver Power-Down 1: RECP Output Driver Power-Up
D6	R/W	0	RECM Output Driver Power Control 0: RECM Output Driver Power-Down 1: RECM Output Driver Power-Up

Book 0 / Page 1 / Register 40: Receiver Amplifier Control 5 - 0x00 / 0x01 / 0x28 (B0_P1_R40) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	11 1001	RECP Driver Volume Control: 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB ... 01 1100: Volume Control = 28 dB 01 1101: Volume Control = 29 dB

5.3.34 Book 0 / Page 1 / Register 41: Receiver Amplifier Control 6 - 0x00 / 0x01 / 0x29 (B0_P1_R41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Receiver Master Volume Control 0: RECP and RECM Volume are Independently Controlled 1: RECP and RECM Volume are Both Controlled by B0_P1_R40_D[5:0]. Should only be used when load of receiver amplifier is differential.
D6	R	0	Reserved. Write only reset values.
D5-D0	R/W	11 1001	RECM Driver Volume Control: 10 0000 - 11 1000: Reserved. Do not use. 11 1001: Volume Control is Muted (Default) 11 1010: Volume Control = -6 dB 11 1011: Volume Control = -5 dB 11 1100: Volume Control = -4 dB 11 1101: Volume Control = -3 dB 11 1110: Volume Control = -2 dB 11 1111: Volume Control = -1 dB 00 0000: Volume Control = 0 dB 00 0001: Volume Control = 1 dB 00 0010: Volume Control = 2 dB ... 01 1100: Volume Control = 28 dB 01 1101: Volume Control = 29 dB

5.3.35 Book 0 / Page 1 / Register 42: Receiver Amplifier Control 7 - 0x00 / 0x01 / 0x2A (B0_P1_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Receiver Amplifier Offset Calibration Flag 0: Offset Calibration is Not Done 1: Offset Calibration is Done
D6-D5	R	00	Reserved. Write only reset values.
D4-D3	R/W	0 1	Receiver Amplifier Offset Calibration Control 00: Offset calibration is disabled 01: Force calibrate for offset at receiver amp power-up for routings selected (Default) 10: Calibrate for offset at receiver amp power-up for selected routings only for the first-power-up of receiver amp. 11: Reserved

Book 0 / Page 1 / Register 42: Receiver Amplifier Control 7 - 0x00 / 0x01 / 0x2A (B0_P1_R42) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2-D0	R/W	000	Receiver Offset Time Control (Ensure that B0_P1_R8_D6='0' for initial offset calibration): 000: Receiver Offset calibration time = 182*197 oscillator clock cycles 001: Receiver Offset calibration time = 38*197 oscillator clock cycles 010: Receiver Offset calibration time = 74*197 oscillator clock cycles 011: Receiver Offset calibration time = 110*197 oscillator clock cycles 100: Receiver Offset calibration time = 146*197 oscillator clock cycles 101: Receiver Offset calibration time = 182*197 oscillator clock cycles 110: Receiver Offset calibration time = 218*197 oscillator clock cycles 111: Receiver Offset calibration time = 253*197 oscillator clock cycles

5.3.36 Book 0 / Page 1 / Register 43-44: Reserved Registers - 0x00 / 0x01 / 0x2B-0x2C (B0_P1_R43-44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.37 Book 0 / Page 1 / Register 45: Speaker Amplifier Control 1 - 0x00 / 0x01 / 0x2D (B0_P1_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left Mixer Amplifier (MAL) to Left Speaker Driver (SPKL) Routing Control: 0: MAL output is not routed to SPKL driver. 1: MAL output is routed to SPKL driver.
D6	R/W	0	Right Mixer Amplifier (MAR) to Right Speaker Driver (SPKR) Routing Control: 0: MAR output is not routed to SPKR driver. 1: MAR output is routed to SPKR driver.
D5-D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Stereo and Mono Speaker Mode Control: 0: Stereo Speaker mode. 1: To support mono speaker mode, whatever routing enabled for SPKR is routed to SPKL also and SPKR can be powered-down.
D1	R/W	0	Left Speaker Driver Power Control: 0: SPKL Driver Power-Down 1: SPKL Driver Power-Up
D0	R/W	0	Right Speaker Driver Power Control: 0: SPKR Driver Power-Down 1: SPKR Driver Power-Up

5.3.38 Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOL Output Routed to SPKL Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 46: Speaker Amplifier Control 2 - 0x00 / 0x01 / 0x2E (B0_P1_R46) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOL Output Not Routed to SPKL Driver (Default)

5.3.39 Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	LOL Output to SPKL and LOR Output to SPKR Master Volume Control 0: LOL Output to SPKL and LOR Output to SPKR Volume are Independently Controlled 1: LOL Output to SPKL and LOR Output to SPKR Volume are Both Controlled by B0_P1_R46_D[6:0]

Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	111 1111	LOR Output Routed to SPKR Driver Volume Control: 000 0000: Volume Control = 0.00 dB 000 0001: Volume Control = -0.5 dB 000 0010: Volume Control = -1.0 dB 000 0011: Volume Control = -1.5 dB 000 0100: Volume Control = -2.0 dB 000 0101: Volume Control = -2.5 dB 000 0110: Volume Control = -3.0 dB 000 0111: Volume Control = -3.5 dB 000 1000: Volume Control = -4.0 dB 000 1001: Volume Control = -4.5 dB 000 1010: Volume Control = -5.0 dB 000 1011: Volume Control = -5.5 dB 000 1100: Volume Control = -6.0 dB 000 1101: Volume Control = -6.5 dB 000 1110: Volume Control = -7.0 dB 000 1111: Volume Control = -7.5 dB 001 0000: Volume Control = -8.0 dB 001 0001: Volume Control = -8.5 dB 001 0010: Volume Control = -9.0 dB 001 0011: Volume Control = -9.5 dB 001 0100: Volume Control = -10.0 dB 001 0101: Volume Control = -10.5 dB 001 0110: Volume Control = -11.0 dB 001 0111: Volume Control = -11.5 dB 001 1000: Volume Control = -12.0 dB 001 1001: Volume Control = -12.5 dB 001 1010: Volume Control = -13.0 dB 001 1011: Volume Control = -13.5 dB 001 1100: Volume Control = -14.1 dB 001 1101: Volume Control = -14.6 dB 001 1110: Volume Control = -15.1 dB 001 1111: Volume Control = -15.6 dB 010 0000: Volume Control = -16.0 dB 010 0001: Volume Control = -16.5 dB 010 0010: Volume Control = -17.1 dB 010 0011: Volume Control = -17.5 dB 010 0100: Volume Control = -18.1 dB 010 0101: Volume Control = -18.6 dB 010 0110: Volume Control = -19.1 dB 010 0111: Volume Control = -19.6 dB 010 1000: Volume Control = -20.1 dB 010 1001: Volume Control = -20.6 dB 010 1010: Volume Control = -21.1 dB 010 1011: Volume Control = -21.6 dB 010 1100: Volume Control = -22.1 dB 010 1101: Volume Control = -22.6 dB 010 1110: Volume Control = -23.1 dB 010 1111: Volume Control = -23.6 dB 011 0000: Volume Control = -24.1 dB 011 0001: Volume Control = -24.6 dB 011 0010: Volume Control = -25.1 dB 011 0011: Volume Control = -25.6 dB 011 0100: Volume Control = -26.1 dB 011 0101: Volume Control = -26.6 dB 011 0110: Volume Control = -27.1 dB 011 0111: Volume Control = -27.6 dB 011 1000: Volume Control = -28.1 dB 011 1001: Volume Control = -28.6 dB 011 1010: Volume Control = -29.1 dB 011 1011: Volume Control = -29.6 dB 011 1100: Volume Control = -30.1 dB 011 1101: Volume Control = -30.6 dB 011 1110: Volume Control = -31.1 dB 011 1111: Volume Control = -31.6 dB 100 0000: Volume Control = -32.1 dB 100 0001: Volume Control = -32.7 dB 100 0010: Volume Control = -33.1 dB

Book 0 / Page 1 / Register 47: Speaker Amplifier Control 3 - 0x00 / 0x01 / 0x2F (B0_P1_R47) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0011: Volume Control = -33.6 dB 100 0100: Volume Control = -34.1 dB 100 0101: Volume Control = -34.6 dB 100 0110: Volume Control = -35.2 dB 100 0111: Volume Control = -35.7 dB 100 1000: Volume Control = -36.1 dB 100 1001: Volume Control = -36.7 dB 100 1010: Volume Control = -37.1 dB 100 1011: Volume Control = -37.7 dB 100 1100: Volume Control = -38.2 dB 100 1101: Volume Control = -38.7 dB 100 1110: Volume Control = -39.2 dB 100 1111: Volume Control = -39.7 dB 101 0000: Volume Control = -40.2 dB 101 0001: Volume Control = -40.7 dB 101 0010: Volume Control = -41.2 dB 101 0011: Volume Control = -41.8 dB 101 0100: Volume Control = -42.1 dB 101 0101: Volume Control = -42.7 dB 101 0110: Volume Control = -43.2 dB 101 0111: Volume Control = -43.8 dB 101 1000: Volume Control = -44.3 dB 101 1001: Volume Control = -44.8 dB 101 1010: Volume Control = -45.2 dB 101 1011: Volume Control = -45.8 dB 101 1100: Volume Control = -46.2 dB 101 1101: Volume Control = -46.7 dB 101 1110: Volume Control = -47.4 dB 101 1111: Volume Control = -47.9 dB 110 0000: Volume Control = -48.2 dB 110 0001: Volume Control = -48.7 dB 110 0010: Volume Control = -49.3 dB 110 0011: Volume Control = -50.0 dB 110 0100: Volume Control = -50.3 dB 110 0101: Volume Control = -51.0 dB 110 0110: Volume Control = -51.4 dB 110 0111: Volume Control = -51.8 dB 110 1000: Volume Control = -52.3 dB 110 1001: Volume Control = -52.7 dB 110 1010: Volume Control = -53.7 dB 110 1011: Volume Control = -54.2 dB 110 1100: Volume Control = -55.4 dB 110 1101: Volume Control = -56.7 dB 110 1110: Volume Control = -58.3 dB 110 1111: Volume Control = -60.2 dB 111 0000: Volume Control = -62.7 dB 111 0001: Volume Control = -64.3 dB 111 0010: Volume Control = -66.2 dB 111 0011: Volume Control = -68.7 dB 111 0100: Volume Control = -72.3 dB 111 0101: Volume Control = -78.3 dB 111 0110 - 1111110: Reserved. Do not use. 111 1111: LOR Output Not Routed to SPKR Driver (Default)

5.3.40 Book 0 / Page 1 / Register 48: Speaker Amplifier Volume Controls - 0x00 / 0x01 / 0x30 (B0_P1_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.

Book 0 / Page 1 / Register 48: Speaker Amplifier Volume Controls - 0x00 / 0x01 / 0x30 (B0_P1_R48) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D4	R/W	000	Left Speaker Amplifier (SPKL) Volume Control: 000: SPKL Driver is Muted (Default) 001: SPKL Driver Volume = 6 dB 010: SPKL Driver Volume = 12 dB 011: SPKL Driver Volume = 18 dB 100: SPKL Driver Volume = 24 dB 101: SPKL Driver Volume = 30 dB 110 - 111: Reserved. Do not use.
D3	R	0	Reserved. Write only reset values.
D2-D0	R/W	000	Right Speaker Amplifier (SPKR) Volume Control: 000: SPKR Driver is Muted (Default) 001: SPKR Driver Volume = 6 dB 010: SPKR Driver Volume = 12 dB 011: SPKR Driver Volume = 18 dB 100: SPKR Driver Volume = 24 dB 101: SPKR Driver Volume = 30 dB 110 - 111: Reserved. Do not use.

5.3.41 Book 0 / Page 1 / Register 49-50: Reserved Registers - 0x00 / 0x01 / 0x31-0x32 (B0_P1_R49-50)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.42 Book 0 / Page 1 / Register 51: Microphone Bias Control - 0x00 / 0x01 / 0x33 (B0_P1_R51)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	External Mic Bias Power/Insertion Control 0: MICBIAS_EXT Powered Down if Jack is not inserted. 1: MICBIAS_EXT Powered On and Off based only on P1_R51_D6, even if Jack is not inserted.
D6	R/W	0	External Mic Bias Power Control 0: MICBIAS_EXT Power Down 1: MICBIAS_EXT Power Up
D5-D4	R/W	00	External Mic Bias Voltage Control 00: MICBIAS_EXT = 1.35 V (if Input Common Mode = 0.75 V) or 1.62 V (if Input Common Mode = 0.9 V). 01: MICBIAS_EXT = 2.0 V (if Input Common Mode = 0.75 V) or 2.4 V (if Input Common Mode = 0.9 V). 10: MICBIAS_EXT = 2.5 V (if Input Common Mode = 0.75 V) or 3.0 V (if Input Common Mode = 0.9 V). 11: MICBIAS_EXT = 3.3 V
D3	R/W	0	0: MICBIAS_EXT is not powered up upon insertion if microphone is not detected on inserted jack 1: MICBIAS_EXT is powered up upon jack detect irrespective of whether microphone is detected or not
D2	R/W	0	Mic Bias Power Control 0: MICBIAS Power Down 1: MICBIAS Power Up
D1-D0	R/W	00	Mic Bias Voltage Control 00: MICBIAS = 1.35 V (if Input Common Mode = 0.75 V) or 1.62 V (if Input Common Mode = 0.9 V). 01: MICBIAS = 2.0 V (if Input Common Mode = 0.75 V) or 2.4 V (if Input Common Mode = 0.9 V). 10: MICBIAS = 2.5 V (if Input Common Mode = 0.75 V) or 3.0 V (if Input Common Mode = 0.9 V). 11: MICBIAS = 3.3 V

5.3.43 Book 0 / Page 1 / Register 52: Input Select 1 for Left Microphone PGA P-Terminal - 0x00

/ 0x01 / 0x34 (B0_P1_R52)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	IN1L to Left Mic PGA (P-Terminal) Selection Control 00: IN1L Not Selected 01: IN1L Selected (RIN = 10K) 10: IN1L Selected (RIN = 20K) 11: IN1L Selected (RIN = 40K)
D5-D4	R/W	00	IN2L to Left Mic PGA (P-Terminal) Selection Control 00: IN2L Not Selected 01: IN2L Selected (RIN = 10K) 10: IN2L Selected (RIN = 20K) 11: IN2L Selected (RIN = 40K)
D3-D2	R/W	00	IN3L to Left Mic PGA (P-Terminal) Selection Control 00: IN3L Not Selected 01: IN3L Selected (RIN = 10K) 10: IN3L Selected (RIN = 20K) 11: IN3L Selected (RIN = 40K)
D1-D0	R/W	00	IN1R to Left Mic PGA (P-Terminal) Selection Control 00: IN1R Not Selected 01: IN1R Selected (RIN = 10K) 10: IN1R Selected (RIN = 20K) 11: IN1R Selected (RIN = 40K) NOTE (For All Inputs to PGA): PGA Value = 0 dB for Singled Ended Input with RIN = 10K PGA Value = +6 dB for Differential Input with RIN = 10K PGA Value = -6 dB for Singled Ended Input with RIN = 20K PGA Value = 0 dB for Differential Input with RIN = 20K PGA Value = -12 dB for Singled Ended Input with RIN = 40K PGA Value = -6 dB for Differential Input with RIN = 40K

5.3.44 Book 0 / Page 1 / Register 53: Input Select 2 for Left Microphone PGA P-Terminal - 0x00 / 0x01 / 0x35 (B0_P1_R53)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN4L to Left Mic PGA (P-Terminal) Selection Control 00: IN4L Not Selected 01: IN4L Selected (RIN = 20K)
D4	R/W	0	IN4R to Left Mic PGA (M-Terminal) Selection Control 00: IN4R Not Selected 01: IN4R Selected (RIN = 20K)
D3-D0	R	0000	Reserved. Write only reset values.

5.3.45 Book 0 / Page 1 / Register 54: Input Select for Left Microphone PGA M-Terminal - 0x00 / 0x01 / 0x36 (B0_P1_R54)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Internal Common Mode (CM1) to Left Mic PGA (M-Terminal) Selection Control 00: CM1 Not Selected 01: CM1 Selected (RIN = 10K) 10: CM1 Selected (RIN = 20K) 11: CM1 Selected (RIN = 40K)
D5-D4	R/W	00	IN2R to Left Mic PGA (M-Terminal) Selection Control 00: IN2R Not Selected 01: IN2R Selected (RIN = 10K) 10: IN2R Selected (RIN = 20K) 11: IN2R Selected (RIN = 40K)
D3-D2	R/W	00	IN3R to Left Mic PGA (M-Terminal) Selection Control 00: IN3R Not Selected 01: IN3R Selected (RIN = 10K) 10: IN3R Selected (RIN = 20K) 11: IN3R Selected (RIN = 40K)

Book 0 / Page 1 / Register 54: Input Select for Left Microphone PGA M-Terminal - 0x00 / 0x01 / 0x36 (B0_P1_R54) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1-D0	R/W	00	Internal Common Mode (CM2) to Left Mic PGA (M-Terminal) Selection Control 00: CM2 Not Selected 01: CM2 Selected (RIN = 10K) 10: CM2 Selected (RIN = 20K) 11: CM2 Selected (RIN = 40K)

5.3.46 Book 0 / Page 1 / Register 55: Input Select 1 for Right Microphone PGA P-Terminal - 0x00 / 0x01 / 0x37 (B0_P1_R55)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	IN1R to Right Mic PGA (P-Terminal) Selection Control 00: IN1R Not Selected 01: IN1R Selected (RIN = 10K) 10: IN1R Selected (RIN = 20K) 11: IN1R Selected (RIN = 40K)
D5-D4	R/W	00	IN2R to Right Mic PGA (P-Terminal) Selection Control 00: IN2R Not Selected 01: IN2R Selected (RIN = 10K) 10: IN2R Selected (RIN = 20K) 11: IN2R Selected (RIN = 40K)
D3-D2	R/W	00	IN3R to Right Mic PGA (P-Terminal) Selection Control 00: IN3R Not Selected 01: IN3R Selected (RIN = 10K) 10: IN3R Selected (RIN = 20K) 11: IN3R Selected (RIN = 40K)
D1-D0	R/W	00	IN2L to Right Mic PGA (P-Terminal) Selection Control 00: IN2L Not Selected 01: IN2L Selected (RIN = 10K) 10: IN2L Selected (RIN = 20K) 11: IN2L Selected (RIN = 40K)

5.3.47 Book 0 / Page 1 / Register 56: Input Select 2 for Right Microphone PGA P-Terminal - 0x00 / 0x01 / 0x38 (B0_P1_R56)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	0	IN4R to Right Mic PGA (P-Terminal) Selection Control 00: IN4R Not Selected 01: IN4R Selected (RIN = 20K)
D4	R/W	0	IN4L to Right Mic PGA (M-Terminal) Selection Control 00: IN4L Not Selected 01: IN4L Selected (RIN = 20K)
D3-D0	R	0000	Reserved. Write only reset values.

5.3.48 Book 0 / Page 1 / Register 57: Input Select for Right Microphone PGA M-Terminal - 0x00 / 0x01 / 0x39 (B0_P1_R57)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Internal Common Mode (CM1) to Right Mic PGA (M-Terminal) Selection Control 00: CM1 Not Selected 01: CM1 Selected (RIN = 10K) 10: CM1 Selected (RIN = 20K) 11: CM1 Selected (RIN = 40K)

Book 0 / Page 1 / Register 57: Input Select for Right Microphone PGA M-Terminal - 0x00 / 0x01 / 0x39 (B0_P1_R57) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	IN1L to Right Mic PGA (M-Terminal) Selection Control 00: IN1L Not Selected 01: IN1L Selected (RIN = 10K) 10: IN1L Selected (RIN = 20K) 11: IN1L Selected (RIN = 40K)
D3-D2	R/W	00	IN3L to Right Mic PGA (M-Terminal) Selection Control 00: IN3L Not Selected 01: IN3L Selected (RIN = 10K) 10: IN3L Selected (RIN = 20K) 11: IN3L Selected (RIN = 40K)
D1-D0	R/W	00	Internal Common Mode (CM2) to Right Mic PGA (M-Terminal) Selection Control 00: CM2 Not Selected 01: CM2 Selected (RIN = 10K) 10: CM2 Selected (RIN = 20K) 11: CM2 Selected (RIN = 40K)

5.3.49 Book 0 / Page 1 / Register 58: Input Common Mode Control - 0x00 / 0x01 / 0x3A (B0_P1_R58)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D6	R/W	0	IN1R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D5	R/W	0	IN2L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D4	R/W	0	IN2R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D3	R/W	0	IN3L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D2	R/W	0	IN3R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D1	R/W	0	IN4L Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode
D0	R/W	0	IN4R Common-Mode Control When Not Connected to PGAs 0: Floating 1: Connected to Internal Common Mode

5.3.50 Book 0 / Page 1 / Register 59: Left Microphone PGA Control - 0x00 / 0x01 / 0x3B (B0_P1_R59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Left MICPGA Gain is enabled 1: Left MICPGA Gain is set to 0dB

Book 0 / Page 1 / Register 59: Left Microphone PGA Control - 0x00 / 0x01 / 0x3B (B0_P1_R59) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0000	Left MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB ... 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use.

5.3.51 Book 0 / Page 1 / Register 60: Right Microphone PGA Control - 0x00 / 0x01 / 0x3C (B0_P1_R60)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Right MICPGA Gain is enabled 1: Right MICPGA Gain is set to 0dB
D6-D0	R/W	000 0000	Right MICPGA Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = 0.5dB 000 0010: Volume Control = 1.0dB ... 101 1101: Volume Control = 46.5dB 101 1110: Volume Control = 47.0dB 101 1111: Volume Control = 47.5dB 110 0000-111 1111: Reserved. Do not use.

5.3.52 Book 0 / Page 1 / Register 61: ADC PowerTune Configuration Register - 0x00 / 0x01 / 0x3D (B0_P1_R61)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: PTM_R4 (Default) 01: PTM_R3 10: PTM_R2 11: PTM_R1
D5-D4	R	00	Reserved. Write only reset values.
D3	R/W	0	0: Left ADC Modulator is gets input from Left ADCPGA 1: Left ADC Modulator gets input directly from pin (IN2L routes to positive terminal of Left ADC Modulator, IN3L routes to negative terminal of Left ADC Modulator)
D2	R/W	0	0: Right ADC Modulator is gets input from Right ADCPGA 1: Right ADC Modulator gets input directly from pin (IN2R routes to positive terminal of Right ADC Modulator, IN3R routes to negative terminal of Right ADC Modulator)
D1-D0	R	00	Reserved. Write only reset values.

5.3.53 Book 0 / Page 1 / Register 62: ADC Analog PGA Gain Flag Register - 0x00 / 0x01 / 0x3E (B0_P1_R62)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only reset values.
D1	R	0	Left Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D0	R	0	Right Channel Analog Volume Control Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume

5.3.54 Book 0 / Page 1 / Register 63: DAC Analog Gain Flags Register 1 - 0x00 / 0x01 / 0x3F

(B0_P1_R63)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	HPR Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	RECP Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	RECM Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3-D0	R	0000	Reserved. Write only reset values.

5.3.55 Book 0 / Page 1 / Register 64: DAC Analog Gain Flags Register 2 - 0x00 / 0x01 / 0x40 (B0_P1_R64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	LOL to HPL Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	LOR to HPR Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	LOL to RECP Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	LOR to RECM Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3	R	0	LOL to SPK-L Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D2	R	0	LOR to SPK-R Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D1	R	0	Reserved. Write only reset values.
D0	R	0	0: Charge Pump is not Powered-Up 1: Charge Pump is Powered-Up

5.3.56 Book 0 / Page 1 / Register 65: Analog Bypass Gain Flags Register - 0x00 / 0x01 / 0x41 (B0_P1_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	IN1L to Receiver Left (RECP) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	IN1R to RECM Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5	R	0	Left ADC PGA to Mixer Amp Left (MAL) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D4	R	0	Right ADC PGA to Mixer Amp Right (MAR) Driver Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D3-D0	R	0000	Reserved. Write only reset values.

5.3.57 Book 0 / Page 1 / Register 66: Driver Power-Up Flags Register - 0x00 / 0x01 / 0x42 (B0_P1_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Line Out Left Driver (LOL) Power-Up Flag 0: LOL Driver Powered Down 1: LOL Driver Powered Up
D6	R	0	Line Out Right Driver (LOR) Power-Up Flag 0: LOR Driver Powered Down 1: LOR Driver Powered Up
D5	R	0	Headphone Left Driver (HPL) Power-Up Flag 0: HPL Driver Powered Down 1: HPL Driver Powered Up
D4	R	0	Headphone Right Driver (HPR) Power-Up Flag 0: HPR Driver Powered Down 1: HPR Driver Powered Up
D3	R	0	Receiver Left Driver (RECP) Power-Up Flag 0: RECP Driver Powered Down 1: RECP Driver Powered Up
D2	R	0	Receiver Right Driver (RECM) Power-Up Flag 0: RECM Driver Powered Down 1: RECM Driver Powered Up
D1	R	0	Speaker Left Driver (SPKL) Power-Up Flag 0: SPKL Driver Powered Down 1: SPKL Driver Powered Up
D0	R	0	Speaker Right Driver (SPKR) Power-Up Flag 0: SPKR Driver Powered Down 1: SPKR Driver Powered Up

5.3.58 Book 0 / Page 1 / Register 67-118: Reserved Registers - 0x00 / 0x01 / 0x43-0x76 (B0_P1_R67-118)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.3.59 Book 0 / Page 1 / Register 119: Headset Detection Tuning Register 1 - 0x00 / 0x01 / 0x77 (B0_P1_R119)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	10	Headset Detection Pulse 0: Detector pulse mode is disabled 1: Detector pulse mode period is enabled with period of 144 cycles of LF_OSC_CLK 2: Detector pulse mode period is enabled with period of 288 cycles of LF_OSC_CLK (default) 3: Detector pulse mode period is enabled with period of 4608 cycles of LF_OSC_CLK
D5-D2	R/W	01 01	Headset Detection Pulse High Duration 0000: Reserved. 0001: Detector pulse high duration is 1*Detector Pulse High Width Scale Factor*LF_OSC_CLK. See bit D1 for Detector Pulse High Width Scale Factor. 0010: Detector pulse high duration is 2*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0011: Detector pulse high duration is 3*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0100: Detector pulse high duration is 4*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 0101: Detector pulse high duration is 5*Detector Pulse High Width Scale Factor*LF_OSC_CLK. (default) ... 1110: Detector pulse high duration is 14*Detector Pulse High Width Scale Factor*LF_OSC_CLK. 1111: Detector pulse high duration is 15*Detector Pulse High Width Scale Factor*LF_OSC_CLK.
D1	R/W	0	Detector Pulse High Width Scale Factor 0: Detector Pulse High Width Scale Factor =1 1: Detector Pulse High Width Scale Factor =8

Book 0 / Page 1 / Register 119: Headset Detection Tuning Register 1 - 0x00 / 0x01 / 0x77 (B0_P1_R119) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	Auto configuration setup 0: Upon microphone insertion detection, the auto configuration of detection is enabled. This enables the detector pulse mode with period of 4608 cycles of the LF_OSC_CLK, and sets Detector Pulse High Width Scale Factor to 8. (default) 1: Upon microphone insertion detection, the auto configuration of detection is enabled. Therefor, detector pulse mode period and Detector Pulse High Width Scale Factor does not change upon insertion.

5.3.60 Book 0 / Page 1 / Register 120: Headset Detection Tuning Register 2 - 0x00 / 0x01 / 0x78 (B0_P1_R120)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0100	Headphone Detection Pulse Width 0000: Headphone Detection Pulse Width is 1*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK, where Detector_Pulse_Period is set by B0_P1_R119_D[7:6]. 0001: Headphone Detection Pulse Width is 1.5*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0010: Headphone Detection Pulse Width is 2*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0011: Headphone Detection Pulse Width is 2.5*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 0100: Headphone Detection Pulse Width is 3*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. (default) ... 1110: Headphone Detection Pulse Width is 8*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK. 1111: Headphone Detection Pulse Width is 8.5*(Detector_Pulse_Period*0.5+1) cycles of LF_OSC_CLK.
D3	R	0	Reserved. Write only reset values.
D2	R/W	0	Headphone Detection Range 0: Headphone detection supported in the range of 16-Ohms to 300-Ohms. 1: Headphone detection supported in the range of 16-Ohms to 64-Ohms.
D1-D0	R/W	10	Microphone Detection for Inputs to IN4L/IN4R: 00: Reserved. Do not use. 01: IN4L/IN4R enabled for microphone detection inputs. 10: IN4L/IN4R disabled for microphone detection inputs. 11: Reserved. Do not use.

5.3.61 Book 0 / Page 1 / Register 121: Microphone PGA Power-Up Control Register - 0x00 / 0x01 / 0x79 (B0_P1_R121)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0011 00	Reserved. Write only reset values.
D1-D0	R/W	11	Left and Right Mic Quick-Charge Duration Control 00: Quick-Charge Duration = 0 ms (Left and Right) 01: Quick-Charge Duration = 2.2 ms (Left) and 0.9 ms (Right) 10: Quick-Charge Duration = 5.5 ms (Left) and 0.9 ms (Right) 11: Quick-Charge Duration = 1.1 ms (Left) and 0.5 ms (Right)

5.3.62 Book 0 / Page 1 / Register 122: Reference Powerup Delay Register - 0x00 / 0x01 / 0x7A (B0_P1_R122)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only reset values.
D3	R/W	0	0: At the fine charge time, VREF is considered as settled and therefore all other necessary blocks are powered-up 1: At the coarse charge time, VREF is considered as settled and therefore all other necessary blocks are powered-up

Book 0 / Page 1 / Register 122: Reference Powerup Delay Register - 0x00 / 0x01 / 0x7A (B0_P1_R122) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	0	0: Chip-Reference powered-up and powered-down internally based on other on-chip block requirements 1: Chip-Reference will be force-fully powered-up
D1-D0	R/W	01	00: VREF Fast Charge Disabled 01: VREF Fast Charge : Coarse Charge Time = 10ms, Fine Charge Time = 30ms (Recommended Setting) 10: VREF Fast Charge : Coarse Charge Time = 20ms, Fine Charge Time = 60ms 11: VREF Fast Charge : Coarse Charge Time = 30ms, Fine Charge Time = 90ms

5.3.63 Book 0 / Page 1 / Register 123-127: Reserved Registers - 0x00 / 0x01 / 0x7B-0x7F (B0_P1_R123-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4 Book 0 Page 3

5.4.1 Book 0 / Page 3 / Register 0: Page Select Register - 0x00 / 0x03 / 0x00 (B0_P3_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

5.4.2 Book 0 / Page 3 / Register 1: Reserved Register - 0x00 / 0x03 / 0x01 (B0_P3_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.3 Book 0 / Page 3 / Register 2: Primary SAR ADC Control - 0x00 / 0x03 / 0x02 (B0_P3_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Normal Mode 1: Stop Conversion and power down SAR ADC
D6-D5	R/W	00	00: SAR ADC resolution = 12-bit 01: SAR ADC resolution = 8-bit 10: SAR ADC resolution = 10-bit 11: SAR ADC resolution = 12-bit
D4-D3	R/W	1 1	00: SAR ADC clock divider = 1 (Use for 8-bit resolution case only) 01: SAR ADC clock divider = 2 (Use for 8-bit/10-bit resolution case only) 10: SAR ADC clock divider = 4 (For better performance in 8-bit/10-bit resolution mode, this setting is recommended) 11: SAR ADC clock divider = 8 (For better performance in 12-bit resolution mode, this setting is recommended)
D2	R/W	0	0: Mean filter is used for on-chip data averaging (if enabled) 1: Median filter is used for on-chip data averaging (if enabled)
D1-D0	R/W	00	00: On-chip data averaging is disabled. 01: 4-data averaging in case mean filter / 5-data averaging in case of median filter. 10: 8-data averaging in case mean filter / 9-data averaging in case of median filter. 11: 16-data averaging in case mean filter / 15-data averaging in case of median filter.

5.4.4 Book 0 / Page 3 / Register 3: Primary SAR ADC Conversion Mode - 0x00 / 0x03 / 0x03

(B0_P3_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D2	R/W	00 00	Conversion Mode 0000: No Scan 0001 - 0101: Reserved. Do not use. 0110: VBAT Measurement 0111: IN1R Measurement 1000: IN1L Measurment 1001: Auto Scan. Sequence used is IN1L, IN1R, VBAT, TEMP1(or TEMP2). Each of these input can be enabled or disabled independently using register-19 and with that sequence will get modified accordingly. Scan continues until stop bit(D7 of reg-2) is sent or D5-D2 of this register is changed. 1010: TEMP1 Measurement 1011: PortScan : IN1L, IN1R, VBAT 1100: TEMP2 Measurement 1101 - 1111: Reserved. Do not use.
D1-D0	R/W	00	00: Interrupt Disabled 01: Interrupt = Data-Available (active LOW) 10-11: Reserved. Do not use.

5.4.5 Book 0 / Page 3 / Register 4-5: Reserved Registers - 0x00 / 0x03 / 0x04-0x05 (B0_P3_R4-5)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	x000 0000	Reserved. Write only reset values.

5.4.6 Book 0 / Page 3 / Register 6: SAR Reference Control - 0x00 / 0x03 / 0x06 (B0_P3_R6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	SAR Reference Selection 0: Use External Reference for SAR Measurement 1: Use Internal Reference (1.25V) for SAR Measurement
D6	R	0	Reserved. Write only reset values.
D5	R/W	1	SAR Internal Reference Power Options 0: Internal Reference Powered Forever for Conversions 1: Internal Reference Powered up/down automatically based on whether conversions are going on or not.
D4	R	0	Reserved. Write only reset values.
D3-D2	R/W	10	SAR Reference Stabilization Time Before Conversion 00: 0 ms 01: 1 ms 10: 4 ms 11: 8 ms
D1-D0	R	00	Reserved. Write only reset values.

5.4.7 Book 0 / Page 3 / Register 7-8: Reserved Registers - 0x00 / 0x03 / 0x07-0x08 (B0_P3_R7-8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.8 Book 0 / Page 3 / Register 9: SAR ADC Flags Register 1 - 0x00 / 0x03 / 0x09 (B0_P3_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R	1	SAR Busy Flag 0: SAR ADC is Busy 1: SAR ADC is not Busy

Book 0 / Page 3 / Register 9: SAR ADC Flags Register 1 - 0x00 / 0x03 / 0x09 (B0_P3_R9) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R	0	SAR Data Available Flag 0: No New Data Available 1: New Data is Available
D4-D0	R	0 0000	Reserved. Write only reset values.

5.4.9 Book 0 / Page 3 / Register 10: SAR ADC Flags Register 2 - 0x00 / 0x03 / 0x0A (B0_P3_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	IN1L Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D6	R	0	IN1R Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D5	R	0	VBAT Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D4-D2	R	000	Reserved. Write only reset values.
D1	R	0	TEMP1 Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)
D0	R	0	TEMP2 Data Available Flag 0: No New Data Available 1: New Data is Available (This bit cleared only after the converted data has been read. Not valid for the buffer mode.)

5.4.10 Book 0 / Page 3 / Register 11-12: Reserved Registers - 0x00 / 0x03 / 0x0B-0x0C (B0_P3_R11-12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.11 Book 0 / Page 3 / Register 13: SAR ADC Buffer Mode Control - 0x00 / 0x03 / 0x0D (B0_P3_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Buffer Mode Enable Select 0: Buffer mode is disabled and RDPTR, WRPTR & TGPTR are set to their default value. 1: Buffer mode is enabled.
D6	R/W	0	Buffer Conversion Mode Select 0: Buffer mode is enabled as continuous conversion mode. 1: Buffer mode is enabled as single shot mode.
D5-D3	R/W	00 0	Buffer Mode Conversion Trigger Level Select 000: Trigger Level for conversion = 8 converted data values 001: Trigger Level for conversion = 16 converted data values 010: Trigger Level for conversion = 24 converted data values 011: Trigger Level for conversion = 32 converted data values 100: Trigger Level for conversion = 40 converted data values 101: Trigger Level for conversion = 48 converted data values 110: Trigger Level for conversion = 56 converted data values 111: Trigger Level for conversion = 64 converted data values
D2	R	0	Reserved. Write only reset values.

Book 0 / Page 3 / Register 13: SAR ADC Buffer Mode Control - 0x00 / 0x03 / 0x0D (B0_P3_R13) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R	0	Buffer Full Flag 0: Buffer is not full 1: Buffer is full (buffer contains 64 unread converted data).
D0	R	1	Buffer Empty Flag 0: Buffer is not empty 1: Buffer is empty (there is no unread converted data in the buffer).

5.4.12 Book 0 / Page 3 / Register 14: Reserved Register - 0x00 / 0x03 / 0x0E (B0_P3_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.13 Book 0 / Page 3 / Register 15: Scan Mode Timer Control - 0x00 / 0x03 / 0x0F (B0_P3_R15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0100	Reserved. Write only reset values.
D3	R/W	0	SAR Auto-Measurement Enable 0: Disabled 1: Enabled
D2-D0	R/W	000	Programmable Interval Timer Delay Setting: 000: Delay = 1.12 min. 001: Delay = 3.36 min. 010: Delay = 5.59 min. 011: Delay = 7.83 min. 100: Delay = 10.01 min. 101: Delay = 12.30 min. 110: Delay = 14.54 min. 111: Delay = 16.78 min. (Note: Based on an 8 MHz Internal Oscillator or MCLK/DIV(Page-0, Reg-23) = 1MHz)

5.4.14 Book 0 / Page 3 / Register 16: Reserved Register - 0x00 / 0x03 / 0x10 (B0_P3_R16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.15 Book 0 / Page 3 / Register 17: SAR ADC Clock Control - 0x00 / 0x03 / 0x11 (B0_P3_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	SAR ADC Clock Selection 0: Internal Oscillator 1: External MCLK1
D6-D0	R/W	000 0001	MCLK1 to SAR ADC Clock Divider Selection 000 0000: MCLK Divider = 128 000 0001: MCLK Divider = 1 000 0010: MCLK Divider = 2 … 111 1110: MCLK Divider = 126 111 1111: MCLK Divider = 127

5.4.16 Book 0 / Page 3 / Register 18: SAR ADC Buffer Mode Data Read Control - 0x00 / 0x03 /

0x12 (B0_P3_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: SPI Interface is used for the SAR/Buffer data reading. 1: I2C Interface is used for the SAR/Buffer data reading.
D6	R/W	0	0: SAR data update is automatically halted (to avoid simultaneous buffer read and write operations) based on internal detection logic. Valid only for SPI interface. 1: SAR data update is held using software control (P3_R18_D5).
D5	R/W	0	0: SAR data update is enabled all the time (valid only if P3_R18_D6 = 1) 1: SAR data update is stopped so that user can read the last updated data without any data corruption (valid only if P3_R18_D6 = 1).
D4-D0	R	0 0000	Reserved. Write only reset values.

5.4.17 Book 0 / Page 3 / Register 19: SAR ADC Measurement Control - 0x00 / 0x03 / 0x13 (B0_P3_R19)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Automatic IN1L Measurement Enable 0: Disable 1: Enable
D6	R/W	0	Automatic IN1R Measurement Enable 0: Disable 1: Enable
D5	R/W	0	Automatic VBAT Measurement Enable 0: Disable 1: Enable
D4	R/W	0	Automatic TEMP Measurement Enable 0: Disable 1: Enable
D3	R/W	0	Automatic TEMP Measurement Sensor Selection 0: TEMP1 1: TEMP2
D2	R/W	0	IN1L Measurement Type Selection 0: Voltage Measurement 1: Resistance Measurement
D1	R/W	0	IN1R Measurement Type Selection 0: Voltage Measurement 1: Resistance Measurement
D0	R/W	0	Resistance Measurement Mode Selection 0: Internal Bias Resistance Measurment Mode 1: External Bias Resistance Measurment Mode

5.4.18 Book 0 / Page 3 / Register 20: Reserved Register - 0x00 / 0x03 / 0x14 (B0_P3_R20)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.19 Book 0 / Page 3 / Register 21: SAR ADC Measurement Threshold Flags - 0x00 / 0x03 / 0x15 (B0_P3_R21)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R	0	IN1L Measurement Max Threshold Flag 0: IN1L Measurement < Programmed Max Threshold Setting 1: IN1L Measurement >= Programmed Max Threshold Setting
D4	R	0	IN1L Measurement Min Threshold Flag 0: IN1L Measurement > Programmed Min Threshold Setting 1: IN1L Measurement <= Programmed Min Threshold Setting

Book 0 / Page 3 / Register 21: SAR ADC Measurement Threshold Flags - 0x00 / 0x03 / 0x15 (B0_P3_R21) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	IN1R Measurement Max Threshold Flag 0: IN1R Measurement < Programmed Max Threshold Setting 1: IN1R Measurement >= Programmed Max Threshold Setting
D2	R	0	IN1R Measurement Min Threshold Flag 0: IN1R Measurement > Programmed Min Threshold Setting 1: IN1R Measurement <= Programmed Min Threshold Setting
D1	R	0	TEMP (TEMP1 / TEMP2) Measurement Max Threshold Flag 0: TEMP Measurement < Programmed Max Threshold Setting 1: TEMP Measurement >= Programmed Max Threshold Setting
D0	R	0	TEMP (TEMP1 / TEMP2) Measurement Min Threshold Flag 0: TEMP Measurement > Programmed Min Threshold Setting 1: TEMP Measurement <= Programmed Min Threshold Setting

5.4.20 Book 0 / Page 3 / Register 22: IN1L Max Threshold Check Control 1 - 0x00 / 0x03 / 0x16 (B0_P3_R22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1L Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1L Max Threshold 12-bit Code (MSB 4-bits)

5.4.21 Book 0 / Page 3 / Register 23: IN1L Max Threshold Check Control 2 - 0x00 / 0x03 / 0x17 (B0_P3_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1L Max Threshold 12-bit Code (LSB 8-bits)

5.4.22 Book 0 / Page 3 / Register 24: IN1L Min Threshold Check Control 1 - 0x00 / 0x03 / 0x18 (B0_P3_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1L Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1L Min Threshold 12-bit Code (MSB 4-bits)

5.4.23 Book 0 / Page 3 / Register 25: IN1L Min Threshold Check Control 2 - 0x00 / 0x03 / 0x19 (B0_P3_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1L Min Threshold 12-bit Code (LSB 8-bits)

5.4.24 Book 0 / Page 3 / Register 26: IN1R Max Threshold Check Control 1 - 0x00 / 0x03 / 0x1A (B0_P3_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1R Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)

Book 0 / Page 3 / Register 26: IN1R Max Threshold Check Control 1 - 0x00 / 0x03 / 0x1A (B0_P3_R26) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	IN1R Max Threshold 12-bit Code (MSB 4-bits)

5.4.25 Book 0 / Page 3 / Register 27: IN1R Max Threshold Check Control 2 - 0x00 / 0x03 / 0x1B (B0_P3_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1R Max Threshold 12-bit Code (LSB 8-bits)

5.4.26 Book 0 / Page 3 / Register 28: IN1R Min Threshold Check Control 1 - 0x00 / 0x03 / 0x1C (B0_P3_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	IN1R Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1R Min Threshold 12-bit Code (MSB 4-bits)

5.4.27 Book 0 / Page 3 / Register 29: IN1R Min Threshold Check Control 2 - 0x00 / 0x03 / 0x1D (B0_P3_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	IN1R Min Threshold 12-bit Code (LSB 8-bits)

5.4.28 Book 0 / Page 3 / Register 30: TEMP Max Threshold Check Control 1 - 0x00 / 0x03 / 0x1E (B0_P3_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	TEMP (TEMP1 / TEMP2) Max Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	IN1R Max Threshold 12-bit Code (MSB 4-bits)

5.4.29 Book 0 / Page 3 / Register 31: TEMP Max Threshold Check Control 2 - 0x00 / 0x03 / 0x1F (B0_P3_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	TEMP (TEMP1 / TEMP2) Max Threshold 12-bit Code (LSB 8-bits)

5.4.30 Book 0 / Page 3 / Register 32: TEMP Min Threshold Check Control 1 - 0x00 / 0x03 / 0x20 (B0_P3_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.
D4	R/W	0	TEMP (TEMP1 / TEMP2) Min Threshold Check Enable Control 0: Disable (Valid For Both Auto and non-Auto Scan Measurement) 1: Enable (Valid For Both Auto and non-Auto Scan Measurement)
D3-D0	R/W	0000	TEMP Min Threshold 12-bit Code (MSB 4-bits)

5.4.31 Book 0 / Page 3 / Register 33: TEMP Min Threshold Check Control 2 - 0x00 / 0x03 / 0x21

(B0_P3_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	TEMP (TEMP1 / TEMP2) Min Threshold 12-bit Code (LSB 8-bits)

5.4.32 Book 0 / Page 3 / Register 34-53: Reserved Registers - 0x00 / 0x03 / 0x22-0x35 (B0_P3_R34-53)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.33 Book 0 / Page 3 / Register 54: IN1L Measurement Data (MSB) - 0x00 / 0x03 / 0x36 (B0_P3_R54)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of IN1L Measurement 16-bit Data

5.4.34 Book 0 / Page 3 / Register 55: IN1L Measurement Data (LSB) - 0x00 / 0x03 / 0x37 (B0_P3_R55)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of IN1L Measurement 16-bit Data

5.4.35 Book 0 / Page 3 / Register 56: IN1R Measurement Data (MSB) - 0x00 / 0x03 / 0x38 (B0_P3_R56)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of IN1R Measurement 16-bit Data

5.4.36 Book 0 / Page 3 / Register 57: IN1R Measurement Data (LSB) - 0x00 / 0x03 / 0x39 (B0_P3_R57)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of IN1R Measurement 16-bit Data

5.4.37 Book 0 / Page 3 / Register 58: VBAT Measurement Data (MSB) - 0x00 / 0x03 / 0x3A (B0_P3_R58)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of VBAT Measurement 16-bit Data

5.4.38 Book 0 / Page 3 / Register 59: VBAT Measurement Data (LSB) - 0x00 / 0x03 / 0x3B (B0_P3_R59)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of VBAT Measurement 16-bit Data

5.4.39 Book 0 / Page 3 / Register 60-65: Reserved Registers - 0x00 / 0x03 / 0x3C-0x41 (B0_P3_R60-65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.4.40 Book 0 / Page 3 / Register 66: TEMP1 Measurement Data (MSB) - 0x00 / 0x03 / 0x42

(B0_P3_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of TEMP1 Measurement 16-bit Data

5.4.41 Book 0 / Page 3 / Register 67: TEMP1 Measurement Data (LSB) - 0x00 / 0x03 / 0x43 (B0_P3_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of TEMP1 Measurement 16-bit Data

5.4.42 Book 0 / Page 3 / Register 68: TEMP2 Measurement Data (MSB) - 0x00 / 0x03 / 0x44 (B0_P3_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	MSB 8-bits of TEMP1 Measurement 16-bit Data

5.4.43 Book 0 / Page 3 / Register 69: TEMP2 Measurement Data (LSB) - 0x00 / 0x03 / 0x45 (B0_P3_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	LSB 8-bits of TEMP1 Measurement 16-bit Data

5.4.44 Book 0 / Page 3 / Register 70-127: Reserved Registers - 0x00 / 0x03 / 0x46-0x7F (B0_P3_R70-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.5 Book 0 Page 4

5.5.1 Book 0 / Page 4 / Register 0: Page Select Register - 0x00 / 0x04 / 0x00 (B0_P4_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table ""Summary of Memory Map" for details.

5.5.2 Book 0 / Page 4 / Register 1: Audio Serial Interface 1, Audio Bus Format Control Register - 0x00 / 0x04 / 0x01 (B0_P4_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Primary Audio Serial Interface Selection 000: ASI1 Audio Interface = I2S 001: ASI1 Audio Interface = DSP 010: ASI1 Audio Interface = RJF 011: ASI1 Audio Interface = LJF 100: ASI1 Audio Interface = Mono PCM 101-111: Reserved. Do not use.
D4-D3	R/W	0 0	Primary Audio Serial Interface Data Word Length Selection 00: ASI1 Data Word length = 16 bits 01: ASI1 Data Word length = 20 bits 10: ASI1 Data Word length = 24 bits 11: ASI1 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	DOUT1 High Impendance Output Control 0: DOUT1 will not be high impedance while ASI1 is active 1: DOUT1 will be high impedance after data has been transferred

5.5.3 Book 0 / Page 4 / Register 2: Audio Serial Interface 1, Left Ch_Offset_1 Control Register - 0x00 / 0x04 / 0x02 (B0_P4_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI1 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

5.5.4 Book 0 / Page 4 / Register 3: Audio Serial Interface 1, Right Ch_Offset_2 Control Register - 0x00 / 0x04 / 0x03 (B0_P4_R3)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI1 Data Offset Value (Ch_Offset_2) relative to last bit of left channel (applicable only if slot mode enabled) 0000 0000: Data Offset 2 = 0 BCLK's 0000 0001: Data Offset 2= 1 BCLK's ... 1111 1110: Data Offset 2 = 254 BCLK's 1111 1111: Data Offset 2 = 255 BCLK's

5.5.5 Book 0 / Page 4 / Register 4: Audio Serial Interface 1, Channel Setup Register - 0x00 / 0x04 / 0x04 (B0_P4_R4)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only default values.
D3-D2	R/W	00	00: For DAC all the left and right channels are enabled 01: For DAC all the left channels are disabled 10: For DAC all the right channels are disabled. 11: For DAC all the left and right channel are disabled.
D1-D0	R/W	00	00: For ADC all the left and right channels are enabled 01: For ADC all the left channels are disabled 10: For ADC all the right channels are disabled. 11: For ADC all the left and right channel are disabled.

5.5.6 Book 0 / Page 4 / Register 5-6: Reserved Registers - 0x00 / 0x04 / 0x05-0x06 (B0_P4_R5-6)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.5.7 Book 0 / Page 4 / Register 7: Audio Serial Interface 1, ADC Input Control - 0x00 / 0x04 / 0x07 (B0_P4_R7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	001	Audio Serial Interface 1 ADC Input Control 000: ASI1 digital audio output data source disabled (No serial data output on external ASI1 bus. ASI1 digital output is tri-stated.) 001: ASI1 digital audio output data is sourced from ADC Data Output (ADC signal fed to ASI1.) 010: ASI1 digital audio output data is sourced from ASI1 digital input data (ASI1-to-ASI1 loopback) 011: ASI1 digital audio output data is sourced from ASI2 digital input data (ASI2-to-ASI1 loopback) 100: ASI1 digital audio output data is sourced from ASI3 digital input data (ASI3-to-ASI1 loopback)

5.5.8 Book 0 / Page 4 / Register 8: Audio Serial Interface 1, DAC Output Control - 0x00 / 0x04

/ 0x08 (B0_P4_R8)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	01	ASI1 Left DAC Datapath 00: ASI1 Left DAC Datapath = Off 01: ASI1 Left DAC Datapath = Left Data 10: ASI1 Left DAC Datapath = Right Data 11: ASI1 Left DAC Datapath = Mono Mix of Left and Right
D5-D4	R/W	01	ASI1 Right DAC Datapath 00: ASI1 Right DAC Datapath = Off 01: ASI1 Right DAC Datapath = Right Data 10: ASI1 Right DAC Datapath = Left Data 11: ASI1 Right DAC Datapath = Mono Mix of Left and Right
D3-D2	R	00	Reserved. Write only default values.
D1	R/W	0	0: Left and right channel slot-swapping is disabled for ADC datapath. 1: Left and right channel slot-swapping is enabled for ADC datapath.
D0	R/W	0	0: Time slot mode is disabled which means the position for left and right channels will be controlled by WCLK and offset1 programming controlled by B0_P4_R2. 1: Time slot mode is enabled which means the position for the left channels are controlled by WCLK and offset1 programming controlled by B0_P4_R2 and for right channel the relative offset with respect to last bit of left channel will be contolled by B0_P4_R3.

5.5.9 Book 0 / Page 4 / Register 9: Audio Serial Interface 1, Control Register 9, ADC Slot Tristate Control - 0x00 / 0x04 / 0x09 (B0_P4_R9)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values.
D4	R/W	0	0: ADC left channel slot is not tri-stated 1: ADC left channel slot is tri-stated
D3-D1	R	000	Reserved. Write only default values.
D0	R/W	0	0: ADC right channel slot is not tri-stated 1: ADC right channel slot is tri-stated

5.5.10 Book 0 / Page 4 / Register 10: Audio Serial Interface 1, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x0A (B0_P4_R10)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Audio Serial Interface 1 Word Clock Direction Control 000: WCLK1 pin is input to Audio Serial Interface 1 001: WCLK1 pin is output from Audio Serial Interface 1 010: GPIO1 pin is input to Audio Serial Interface 1 011: GPIO1 pin is output from Audio Serial Interface 1 100: DOUT3 pin is output from Audio Serial Interface 1 101-111: Reserved. Do not use.
D4-D2	R/W	0 00	Audio Serial Interface 1 Bit Clock Direction Control 000: BCLK1 pin is input to Audio Serial Interface 1 001: BCLK1 pin is output from Audio Serial Interface 1 010: GPIO2 pin is input to Audio Serial Interface 1 011: GPIO2 pin is output from Audio Serial Interface 1 100-111: Reserved. Do not use.
D1	R/W	0	Primary Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	Primary BCLK and Primary WCLK Power control 0: Primary BCLK and Primary WCLK buffers are powered down when the codec is powered down or Audio Serial Interface 1 is inactive 1: Primary BCLK and Primary WCLK buffers are powered up when they are used in clock generation even when the codec is powered down

5.5.11 Book 0 / Page 4 / Register 11: Audio Serial Interface 1, Bit Clock N Divider Input Control

- 0x00 / 0x04 / 0x0B (B0_P4_R11)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI1 BDIV_CLKIN Multiplexer Control 00: ASI1_BDIV_CLKIN = DAC_CLK 01: ASI1_BDIV_CLKIN = DAC_MOD_CLK 10: ASI1_BDIV_CLKIN = ADC_CLK 11: ASI1_BDIV_CLKIN = ADC_MOD_CLK

5.5.12 Book 0 / Page 4 / Register 12: Audio Serial Interface 1, Bit Clock N Divider - 0x00 / 0x04 / 0x0C (B0_P4_R12)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1 BCLK N Divider Power Control 0: BCLK N divider powered down 1: BCLK N divider powered up
D6-D0	R/W	000 0001	ASI1 BCLK N Divider value 0000 0000: BCLK N divider = 128 0000 0001: BCLK N divider = 1 ... 1111 1110: BCLK N divider = 126 1111 1111: BCLK N divider = 127

5.5.13 Book 0 / Page 4 / Register 13: Audio Serial Interface 1, Word Clock N Divider - 0x00 / 0x04 / 0x0D (B0_P4_R13)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI1 WCLK Divider Power Control 0: Primary WCLK N divider is powered down 1: Primary WCLK N divider is powered up
D6-D0	R/W	010 0000	ASI1 WCLK N Divider value 000 0000: Primary WCLK divider N = 128 010 0000: Primary WCLK divider N = 32 010 0001: Primary WCLK divider N = 33 … 111 1110: Primary WCLK divider N = 126 111 1111: Primary WCLK divider N = 127

5.5.14 Book 0 / Page 4 / Register 14: Audio Serial Interface 1, BCLK and WCLK Output - 0x00 / 0x04 / 0x0E (B0_P4_R14)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	ASI1 Bit Clock Output Mux 000: Bit Clock Output = ASI1 Bit Clock Divider Output 001: Reserved. Do not use. 010: Bit Clock Output = ASI2 Bit Clock Divider Output 011: Bit Clock Output = ASI2 Bit Clock Input 100: Bit Clock Output = ASI3 Bit Clock Divider Output 101: Bit Clock Output = ASI3 Bit Clock Input 110-111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	ASI1 Word Clock Output Mux 000: Word Clock Output = Generated DAC_FS 001: Word Clock Output = Generated ADC_FS 010: Word Clock Output = ASI1 Word Clock Divider Output 011: Reserved. Do not use. 100: Word Clock Output = ASI2 Word Clock Divider Output 101: Word Clock Output = ASI2 Word Clock Input 110: Word Clock Output = ASI3 Word Clock Divider Output 111: Word Clock Output = ASI3 Word Clock Input

5.5.15 Book 0 / Page 4 / Register 15: Audio Serial Interface 1, Data Output - 0x00 / 0x04 / 0x0F (B0_P4_R15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI1 Data Output Control 00: DOUT1 from Codec Audio Serial Interface 1 Output 01: DOUT1 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT1 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT1 from ASI3 Data Input (Pin-to-Pin Loopback)

5.5.16 Book 0 / Page 4 / Register 16: Audio Serial Interface 1, ADC WCLK and BCLK Control - 0x00 / 0x04 / 0x10 (B0_P4_R16)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	Audio Serial Interface 1 ADC Word Clock Control for Six-Wire Interface 000: ADC WCLK is same as DAC WCLK (Default 4-wire Interface) 001: ADC WCLK is input/output on GPIO1 010: ADC WCLK is input/output on GPIO2 011: ADC WCLK is input on GPI1 100: ADC WCLK is input on GPI2 101: ADC WCLK is input on GPI3 110: ADC WCLK is input on GPI4 111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	Audio Serial Interface 1 ADC Bit Clock Control for Six-Wire Interface 000: ADC BCLK is same as DAC BCLK (Default 4-wire Interface) 001: ADC BCLK is input/output on GPIO1 010: ADC BCLK is input/output on GPIO2 011: ADC BCLK is input on GPI1 100: ADC BCLK is input on GPI2 101: ADC BCLK is input on GPI3 110: ADC BCLK is input on GPI4 111: Reserved. Do not use.

5.5.17 Book 0 / Page 4 / Register 17: Audio Serial Interface 2, Audio Bus Format Control Register - 0x00 / 0x04 / 0x11 (B0_P4_R17)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Secondary Audio Serial Interface Selection 000: ASI2 Audio Interface = I2S 001: ASI2 Audio Interface = DSP 010: ASI2 Audio Interface = RJF 011: ASI2 Audio Interface = LJF 100: ASI2 Audio Interface = Mono PCM 101: Reserved. Do not use.
D4-D3	R/W	0 0	Secondary Audio Serial Interface Data Word Length Selection 00: ASI2 Data Word length = 16 bits 01: ASI2 Data Word length = 20 bits 10: ASI2 Data Word length = 24 bits 11: ASI2 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	ASI2 Data Output High Impendance Output Control 0: DOUT2 will not be high impedance while ASI2 is active 1: DOUT2 will be high impedance after data has been transferred

5.5.18 Book 0 / Page 4 / Register 18: Audio Serial Interface 2, Data Offset Control Register -

0x00 / 0x04 / 0x12 (B0_P4_R18)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI2 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

5.5.19 Book 0 / Page 4 / Register 19-22: Reserved Registers - 0x00 / 0x04 / 0x13-0x16 (B0_P4_R19-22)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.20 Book 0 / Page 4 / Register 23: Audio Serial Interface 2, ADC Input Control - 0x00 / 0x04 / 0x17 (B0_P4_R23)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	Audio Serial Interface 2 ADC Input Control 000: ASI2 digital audio output data source disabled (No serial data output on external ASI2 bus. ASI2 digital output is tri-stated.) 001: ASI2 digital audio output data is sourced from ADC Digital Output 010: ASI2 digital audio output data is sourced from ASI1 digital input data (ASI1-to-ASI2 loopback) 011: ASI2 digital audio output data is sourced from ASI2 digital input data (ASI2-to-ASI1 loopback) 100: ASI2 digital audio output data is sourced from ASI3 digital input data (ASI3-to-ASI1 digital loopback) 101: Reserved. Do not use. 110-111: Reserved. Do not use.

5.5.21 Book 0 / Page 4 / Register 24: Audio Serial Interface 2, DAC Output Control - 0x00 / 0x04 / 0x18 (B0_P4_R24)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	ASI2 Left DAC Datapath 00: ASI2 Left DAC Datapath = Off 01: ASI2 Left DAC Datapath = Left Data 10: ASI2 Left DAC Datapath = Right Data 11: ASI2 Left DAC Datapath = Mono Mix of Left and Right
D5-D4	R/W	00	ASI2 Right DAC Datapath 00: ASI2 Right DAC Datapath = Off 01: ASI2 Right DAC Datapath = Right Data 10: ASI2 Right DAC Datapath = Left Data 11: ASI2 Right DAC Datapath = Mono Mix of Left and Right
D3-D0	R	0000	Reserved. Write only default values.

5.5.22 Book 0 / Page 4 / Register 25: Reserved Register - 0x00 / 0x04 / 0x19 (B0_P4_R25)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.23 Book 0 / Page 4 / Register 26: Audio Serial Interface 2, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x1A (B0_P4_R26)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values.

Book 0 / Page 4 / Register 26: Audio Serial Interface 2, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x1A (B0_P4_R26) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5	R/W	0	Audio Serial Interface 2 Word Clock Direction Control 0: WCLK2 pin is input to Audio Serial Interface 2 1: WCLK2 pin is output from Audio Serial Interface 2
D4-D3	R	0 0	Reserved. Write only default values.
D2	R/W	0	Audio Serial Interface 2 Bit Clock Direction Control 0: BCLK2 pin is input to Audio Serial Interface 2 Bit Clock 1: BCLK2 pin is output from Audio Serial Interface 2 Bit Clock
D1	R/W	0	Audio Serial Interface 2 Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	Audio Serial Interface 2 BCLK and WCLK Power control 0: ASI2 BCLK and Primary WCLK buffers are powered down when the codec is powered down or Audio Serial Interface 2 is inactive 1: ASI2 BCLK and WCLK buffers are powered up when they are used in clock generation even when the codec is powered down

5.5.24 Book 0 / Page 4 / Register 27: Audio Serial Interface 2, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x1B (B0_P4_R27)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI2_BDIV_CLKIN Multiplexer Control 00: ASI2_BDIV_CLKIN = DAC_CLK (Generated On-Chip) 01: ASI2_BDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 10: ASI2_BDIV_CLKIN = ADC_CLK (Generated On-Chip) 11: ASI2_BDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip)

5.5.25 Book 0 / Page 4 / Register 28: Audio Serial Interface 2, Bit Clock N Divider - 0x00 / 0x04 / 0x1C (B0_P4_R28)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI2 BCLK Divider Power Control 0: Secondary BCLK N divider is powered down 1: Secondary BCLK N divider is powered up
D6-D0	R/W	000 0001	ASI2 BCLK N Divider value 000 0000: Secondary BCLK divider N = 128 000 0001: Secondary BCLK divider N = 1 000 0010: Secondary BCLK divider N = 2 … 111 1110: Secondary BCLK divider N = 126 111 1111: Secondary BCLK divider N = 127

5.5.26 Book 0 / Page 4 / Register 29: Audio Serial Interface 2, Word Clock N Divider - 0x00 / 0x04 / 0x1D (B0_P4_R29)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI2 WCLK Divider Power Control 0: Secondary WCLK N divider is powered down 1: Secondary WCLK N divider is powered up
D6-D0	R/W	010 0000	ASI2 WCLK N Divider value 000 0000: Secondary WCLK divider N = 128 010 0000: Secondary WCLK divider N = 32 010 0001: Secondary WCLK divider N = 33 … 111 1110: Secondary WCLK divider N = 126 111 1111: Secondary WCLK divider N = 127

5.5.27 Book 0 / Page 4 / Register 30: Audio Serial Interface 2, BCLK and WCLK Output - 0x00 / 0x04 / 0x1E (B0_P4_R30)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	010	ASI2 Bit Clock Output Mux 000: ASI2_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 001: ASI2_BCLK_OUT = ASI1 Bit Clock Input (ASI1_BCLK) 010: ASI2_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 011: Reserved. Do not use. 100: ASI2_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 101: ASI2_BCLK_OUT = ASI3 Bit Clock Input (ASI3_BCLK) 110-111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	ASI2 Word Clock Output Mux 000: ASI2_WCLK_OUT = Generated DAC_FS 001: ASI2_WCLK_OUT = Generated ADC_FS 010: ASI2_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 011: ASI2_WCLK_OUT = ASI1 Word Clock Input (ASI1_WCLK) 100: ASI2_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 101: Reserved. Do not use. 110: ASI2_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 111: ASI2_WCLK_OUT = ASI3 Word Clock Input (ASI3_WCLK)

5.5.28 Book 0 / Page 4 / Register 31: Audio Serial Interface 2, Data Output - 0x00 / 0x04 / 0x1F (B0_P4_R31)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI2 Data Output Control 00: DOUT2 from Codec Audio Serial Interface 2 Output 01: DOUT2 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT2 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT2 from ASI3 Data Input (Pin-to-Pin Loopback)

5.5.29 Book 0 / Page 4 / Register 32: Audio Serial Interface 2, ADC WCLK and BCLK Control - 0x00 / 0x04 / 0x20 (B0_P4_R32)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	Audio Serial Interface 2 ADC Word Clock Control for Six-Wire Interface 000: ADC WCLK is same as DAC WCLK (Default 4-wire Interface) 001: ADC WCLK is input/output on GPIO1 010: ADC WCLK is input/output on GPIO2 011: ADC WCLK is input on GPI1 100: ADC WCLK is input on GPI2 101: ADC WCLK is input on GPI3 110: ADC WCLK is input on GPI4 111: Reserved
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	Audio Serial Interface 2 ADC Bit Clock Control for Six-Wire Interface 000: ADC BCLK is same as DAC BCLK (Default 4-wire Interface) 001: ADC BCLK is input/output on GPIO1 010: ADC BCLK is input/output on GPIO2 011: ADC BCLK is input on GPI1 100: ADC BCLK is input on GPI2 101: ADC BCLK is input on GPI3 110: ADC BCLK is input on GPI4 111: Reserved

5.5.30 Book 0 / Page 4 / Register 33: Audio Serial Interface 3, Audio Bus Format Control

Register - 0x00 / 0x04 / 0x21 (B0_P4_R33)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R/W	000	Tertiary Audio Serial Interface Selection 000: ASI3 Audio Interface = I2S 001: ASI3 Audio Interface = DSP 010: ASI3 Audio Interface = RJF 011: ASI3 Audio Interface = LJF 100: ASI3 Audio Interface = Mono PCM 101-111: Reserved. Do not use.
D4-D3	R/W	0 0	Tertiary Audio Serial Interface Data Word Length Selection 00: ASI3 Data Word length = 16 bits 01: ASI3 Data Word length = 20 bits 10: ASI3 Data Word length = 24 bits 11: ASI3 Data Word length = 32 bits
D2-D1	R	00	Reserved. Write only default values.
D0	R/W	0	DOUT3 High Impendance Output Control 0: DOUT3 will not be high impedance while ASI1 is active 1: DOUT3 will be high impedance after data has been transferred

5.5.31 Book 0 / Page 4 / Register 34: Audio Serial Interface 3, Data Offset Control Register - 0x00 / 0x04 / 0x22 (B0_P4_R34)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ASI3 Data Offset Value (Ch_Offset_1) relative to rising edge of Word Clock (Offset measured from Rising Edge of Word Clock in DSP mode) 0000 0000: Data Offset 1 = 0 BCLK's 0000 0001: Data Offset 1= 1 BCLK's ... 1111 1110: Data Offset 1 = 254 BCLK's 1111 1111: Data Offset 1 = 255 BCLK's

5.5.32 Book 0 / Page 4 / Register 35-38: Reserved Registers - 0x00 / 0x04 / 0x23-0x26 (B0_P4_R35-38)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.33 Book 0 / Page 4 / Register 39: Audio Serial Interface 3, ADC Input Control - 0x00 / 0x04 / 0x27 (B0_P4_R39)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values.
D2-D0	R/W	000	Audio Serial Interface 3 ADC Input Control 000: ASI3 digital audio output data source disabled (No serial data output on external ASI3 bus. ASI3 digital output is tri-stated.) 001: ASI3 digital audio output data is sourced from ADC Digital Output. 010: ASI3 digital audio output data is sourced from ASI1 digital input data (ASI1-to-ASI3 loopback) 011: ASI3 digital audio output data is sourced from ASI2 digital input data (ASI2-to-ASI3 loopback) 100: ASI3 digital audio output data is sourced from ASI3 digital input data (ASI3-to-ASI3 loopback) 101-111: Reserved. Do not use.

5.5.34 Book 0 / Page 4 / Register 40: Audio Serial Interface 3, DAC Output Control - 0x00 / 0x04 / 0x28 (B0_P4_R40)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	ASI3 Left DAC Datapath 00: ASI3 Left DAC Datapath = Off 01: ASI3 Left DAC Datapath = Left Data 10: ASI3 Left DAC Datapath = Right Data 11: ASI3 Left DAC Datapath = Mono Mix of Left and Right

Book 0 / Page 4 / Register 40: Audio Serial Interface 3, DAC Output Control - 0x00 / 0x04 / 0x28 (B0_P4_R40) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	ASI3 Right DAC Datapath 00: ASI3 Right DAC Datapath = Off 01: ASI3 Right DAC Datapath = Right Data 10: ASI3 Right DAC Datapath = Left Data 11: ASI3 Right DAC Datapath = Mono Mix of Left and Right
D3-D0	R	0000	Reserved. Write only default values.

5.5.35 Book 0 / Page 4 / Register 41: Reserved Register - 0x00 / 0x04 / 0x29 (B0_P4_R41)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.36 Book 0 / Page 4 / Register 42: Audio Serial Interface 3, WCLK and BCLK Control Register - 0x00 / 0x04 / 0x2A (B0_P4_R42)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values.
D5	R/W	0	Audio Serial Interface 3 Word Clock Direction Control 0: WCLK3 pin is input to Audio Serial Interface 3 1: WCLK3 pin is output from Audio Serial Interface 3
D4-D3	R	0 0	Reserved. Write only default values.
D2	R/W	0	Audio Serial Interface 3 Bit Clock Direction Control 0: BCLK3 pin is input to Audio Serial Interface 3 Bit Clock 1: BCLK3 pin is output from Audio Serial Interface 3 Bit Clock
D1	R/W	0	Audio Serial Interface 3 Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D0	R/W	0	Audio Serial Interface 3 BCLK and WCLK Power control 0: ASI3 BCLK and Primary WCLK buffers are powered down when the codec is powered down or Audio Serial Interface 3 is inactive 1: ASI3 BCLK and WCLK buffers are powered up when they are used in clock generation even when the codec is powered down

5.5.37 Book 0 / Page 4 / Register 43: Audio Serial Interface 3, Bit Clock N Divider Input Control - 0x00 / 0x04 / 0x2B (B0_P4_R43)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI3_BDIV_CLKIN Multiplexer Control 00: ASI3_BDIV_CLKIN = DAC_CLK (Generated On-Chip) 01: ASI3_BDIV_CLKIN = DAC_MOD_CLK (Generated On-Chip) 10: ASI3_BDIV_CLKIN = ADC_CLK (Generated On-Chip) 11: ASI3_BDIV_CLKIN = ADC_MOD_CLK (Generated On-Chip)

5.5.38 Book 0 / Page 4 / Register 44: Audio Serial Interface 3, Bit Clock N Divider - 0x00 / 0x04 / 0x2C (B0_P4_R44)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI3 BCLK Divider Power Control 0: Tertiary BCLK N divider is powered down 1: Tertiary BCLK N divider is powered up

Book 0 / Page 4 / Register 44: Audio Serial Interface 3, Bit Clock N Divider - 0x00 / 0x04 / 0x2C (B0_P4_R44) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0001	ASI3 BCLK N Divider value 000 0000: Tertiary BCLK divider N = 128 000 0001: Tertiary BCLK divider N = 1 000 0010: Tertiary BCLK divider N = 2 … 111 1110: Tertiary BCLK divider N = 126 111 1111: Tertiary BCLK divider N = 127

5.5.39 Book 0 / Page 4 / Register 45: Audio Serial Interface 3, Word Clock N Divider - 0x00 / 0x04 / 0x2D (B0_P4_R45)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	ASI3 WCLK Divider Power Control 0: Tertiary WCLK N divider is powered down 1: Tertiary WCLK N divider is powered up
D6-D0	R/W	010 0000	ASI3 WCLK N Divider value 000 0000: Tertiary WCLK divider N = 128 010 0000: Tertiary WCLK divider N = 32 010 0001: Tertiary WCLK divider N = 33 … 111 1110: Tertiary WCLK divider N = 126 111 1111: Tertiary WCLK divider N = 127

5.5.40 Book 0 / Page 4 / Register 46: Audio Serial Interface 3, BCLK and WCLK Output - 0x00 / 0x04 / 0x2E (B0_P4_R46)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	100	ASI3 Bit Clock Output Mux 000: ASI3_BCLK_OUT = ASI1 Bit Clock Divider Output (ASI1_BDIV_OUT) 001: ASI3_BCLK_OUT = ASI1 Bit Clock Input (ASI1_BCLK) 010: ASI3_BCLK_OUT = ASI2 Bit Clock Divider Output (ASI2_BDIV_OUT) 011: ASI3_BCLK_OUT = ASI2 Bit Clock Input (ASI2_BCLK) 100: ASI3_BCLK_OUT = ASI3 Bit Clock Divider Output (ASI3_BDIV_OUT) 101-111: Reserved. Do not use.
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	ASI3 Word Clock Output Mux 000: ASI3_WCLK_OUT = Generated DAC_FS 001: ASI3_WCLK_OUT = Generated ADC_FS 010: ASI3_WCLK_OUT = ASI1 Word Clock Divider Output (ASI1_WDIV_OUT) 011: ASI3_WCLK_OUT = ASI1 Word Clock Input (ASI1_WCLK) 100: ASI3_WCLK_OUT = ASI2 Word Clock Divider Output (ASI2_WDIV_OUT) 101: ASI3_WCLK_OUT = ASI2 Word Clock Input (ASI2_WCLK) 110: ASI2_WCLK_OUT = ASI3 Word Clock Divider Output (ASI3_WDIV_OUT) 111: Reserved. Do not use.

5.5.41 Book 0 / Page 4 / Register 47: Audio Serial Interface 3, Data Output - 0x00 / 0x04 / 0x2F (B0_P4_R47)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values.
D1-D0	R/W	00	ASI3 Data Output Control 00: DOUT3 from Codec Audio Serial Interface 3 Output 01: DOUT3 from ASI1 Data Input (Pin-to-Pin Loopback) 10: DOUT3 from ASI2 Data Input (Pin-to-Pin Loopback) 11: DOUT3 from ASI3 Data Input (Pin-to-Pin Loopback)

5.5.42 Book 0 / Page 4 / Register 48: Audio Serial Interface 3, ADC WCLK and BCLK Control -

0x00 / 0x04 / 0x30 (B0_P4_R48)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values.
D6-D4	R/W	000	Audio Serial Interface 3 ADC Word Clock Control for Six-Wire Interface 000: ADC WCLK is same as DAC WCLK (Default 4-wire Interface) 001: ADC WCLK is input/output on GPIO1 010: ADC WCLK is input/output on GPIO2 011: ADC WCLK is input on GPI1 100: ADC WCLK is input on GPI2 101: ADC WCLK is input on GPI3 110: ADC WCLK is input on GPI4 111: Reserved
D3	R	0	Reserved. Write only default values.
D2-D0	R/W	000	Audio Serial Interface 3 ADC Bit Clock Control for Six-Wire Interface 000: ADC BCLK is same as DAC BCLK (Default 4-wire Interface) 001: ADC BCLK is input/output on GPIO1 010: ADC BCLK is input/output on GPIO2 011: ADC BCLK is input on GPI1 100: ADC BCLK is input on GPI2 101: ADC BCLK is input on GPI3 110: ADC BCLK is input on GPI4 111: Reserved

5.5.43 Book 0 / Page 4 / Register 49-64: Reserved Registers - 0x00 / 0x04 / 0x31-0x40 (B0_P4_R49-64)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.44 Book 0 / Page 4 / Register 65: WCLK1 (Input/Output) Pin Control - 0x00 / 0x04 / 0x41 (B0_P4_R65)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values.
D5-D2	R/W	00 01	WCLK1 Pin Control 0000: Reserved. Do not use. 0001: WCLK1 is ASI1 Word Clock Input/Output. (Note: B0_P4_R10 defines ASI1 Word Clock routing.) 0010-0011: Reserved. Do not use. 0100: WCLK1 pin is CLKOUT output.
D1-D0	R	00	Reserved. Write only default values.

5.5.45 Book 0 / Page 4 / Register 66: Reserved Register - 0x00 / 0x04 / 0x42 (B0_P4_R66)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values.

5.5.46 Book 0 / Page 4 / Register 67: DOUT1 (Output) Pin Control - 0x00 / 0x04 / 0x43 (B0_P4_R67)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	1	DOUT1 Bus Keeper Control 0: DOUT1 Bus Keeper Enabled 1: DOUT1 Bus Keeper Disabled

Book 0 / Page 4 / Register 67: DOUT1 (Output) Pin Control - 0x00 / 0x04 / 0x43 (B0_P4_R67) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D1	R/W	0 001	DOUT1 Pin Control 0000: DOUT1 disabled 0001: DOUT1 is ASI1 Data Output 0010: DOUT1 is General Purpose Output 0011: DOUT1 is CLKOUT 0100: DOUT1 is INT1 0101: DOUT1 is INT2 0110: DOUT1 is SAR ADC interrupt as defined in B0_P3 0111-1111: Reserved.
D0	R/W	0	DOUT1 as General Purpose Output 0: DOUT1 General Purpose Output is '0' 1: DOUT1 General Purpose Output is '1'

5.5.47 Book 0 / Page 4 / Register 68: DIN1 (Input) Pin Control - 0x00 / 0x04 / 0x44 (B0_P4_R68)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6-D5	R/W	01	DIN1 Pin Control 00: DIN1 pin is disabled 01: DIN1 is enabled for Primary Data Input or Digital Microphone Input, General Purpose Clock input or as General Purpose Input 10-11: Reserved. Do not use
D4	R	X	DIN1 Input Pin State, used along with DIN1 as general purpose input
D3-D0	R	0000	Reserved. Write only reset values.

5.5.48 Book 0 / Page 4 / Register 69: WCLK2 (Input/Output) Pin Control - 0x00 / 0x04 / 0x45 (B0_P4_R69)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D2	R/W	00 01	WCLK2 Pin Control 0000: WCLK2 pin Disabled (Input and Output buffers powered down) 0001: WCLK2 pin acts as ASI Secondary WCLK as defined in B0_P4_R26_D5 0010: WCLK2 pin is used as General Purpose Input (GPI) or chip input for any other purpose. 0011: WCLK2 pin Output = General Purpose Output 0100: WCLK2 pin Output = CLKOUT Output 0101: WCLK2 pin Output = INT1 Interrupt Output 0110: WCLK2 pin Output = INT2 Interrupt Output 0111-1001: Reserved. Do not use. 1010: WCLK2 pin Output = ADC_MOD_CLK Output for digital microphone 1011: Reserved. Do not use. 1100: WCLK2 pin Output = SAR ADC interrupt as defined in B0_P3 1101-1111: Reserved. Do not use.
D1	R	X	WCLK2 Input Pin State, used along with WCLK2 as general purpose input
D0	R/W	0	WCLK2 as General Purpose Output 0: WCLK2 General Purpose Output is '0' 1: WCLK2 General Purpose Output is '1'

5.5.49 Book 0 / Page 4 / Register 70: BCLK2 (Input/Output) Pin Control - 0x00 / 0x04 / 0x46 (B0_P4_R70)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values

Book 0 / Page 4 / Register 70: BCLK2 (Input/Output) Pin Control - 0x00 / 0x04 / 0x46 (B0_P4_R70) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D2	R/W	00 01	BCLK2 Pin Control 0000: BCLK2 pin Disabled (Input and Output buffers powered down) 0001: BCLK2 pin acts as ASI Secondary BCLK as defined in B0_P4_R26_D2 0010: BCLK2 pin is used as General Purpose Input (GPI) or chip input for any other purpose. 0011: BCLK2 pin Output = General Purpose Output 0100: BCLK2 pin Output = CLKOUT Output 0101: BCLK2 pin Output = INT1 Interrupt Output 0110: BCLK2 pin Output = INT2 Interrupt Output 0111-1001: Reserved. Do not use. 1010: BCLK2 pin Output = ADC_MOD_CLK Output for the digital microphone 1011: Reserved. Do not use. 1100: BCLK2 pin Output = SAR ADC interrupt as defined in B0_P3 1101-1111: Reserved. Do not use.
D1	R	X	BCLK2 Input Pin State, used along with BCLK2 as general purpose input
D0	R/W	0	BCLK2 as General Purpose Output 0: BCLK2 General Purpose Output is '0' 1: BCLK2 General Purpose Output is '1'

5.5.50 Book 0 / Page 4 / Register 71: DOUT2 (Output) Pin Control - 0x00 / 0x04 / 0x47 (B0_P4_R71)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	1	DOUT2 Bus Keeper Control 0: DOUT2 Bus Keeper Enabled 1: DOUT2 Bus Keeper Disabled
D4-D1	R/W	0 001	DOUT2 Pin Control 0000: DOUT2 pin disabled 0001: DOUT2 pin Output = ASI2 Data Output 0010: DOUT2 pin Output = General Purpose Output 0011: Reserved. Do not use. 0100: DOUT2 pin Output = INT1 Interrupt 0101: DOUT2 pin Output = INT2 Interrupt 0110: DOUT2 pin is SAR ADC interrupt as defined in B0_P3 0111-1001: Reserved. Do not use. 1010: DOUT2 pin Output = ADC_MOD_CLK Output for digital microphone 1011-1111: Reserved. Do not use.
D0	R/W	0	DOUT2 as General Purpose Output 0: DOUT2 General Purpose Output is '0' 1: DOUT2 General Purpose Output is '1'

5.5.51 Book 0 / Page 4 / Register 72: DIN2 (Input) Pin Control - 0x00 / 0x04 / 0x48 (B0_P4_R72)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D5	R/W	01	DIN2 Pin Control 00: DIN2 Disabled (Input buffer powered down) 01: DIN2 Enabled (can be used as Data Input of ASI2, Dig_Mic_In, ADC_WCLK, ClockGen Block, or General Purpose Input. Program other registers to choose) 10-11: Reserved. Do not use.
D4	R	X	DIN2 Input Pin State, used along with DIN2 as general purpose input
D3-D0	R	0000	Reserved. Write only reset values.

5.5.52 Book 0 / Page 4 / Register 73: WCLK3 (Input/Output) Pin Control - 0x00 / 0x04 / 0x49

(B0_P4_R73)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values
D5-D2	R/W	00 01	WCLK3 Pin Control 0000: WCLK3 pin Disabled 0001: WCLK3 pin acts as ASI3 WCLK as defined in B0_P4_R42_D5 0010: WCLK3 pin is used as General Purpose Input (GPI) or General Purpose Clock Input for LFR_CLKIN or HF_CLKIN 0011: WCLK3 pin Output = General Purpose Output 0100-1111: Reserved. Do not use.
D1	R	X	WCLK3 Input Pin State, used along with WCLK3 as general purpose input
D0	R/W	0	WCLK3 as General Purpose Output 0: WCLK3 General Purpose Output is '0' 1: WCLK3 General Purpose Output is '1'

5.5.53 Book 0 / Page 4 / Register 74: BCLK3 (Input/Output) Pin Control - 0x00 / 0x04 / 0x4A (B0_P4_R74)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	xx	Reserved. Write only reset values
D5-D2	R/W	00 01	BCLK3 Pin Control 0000: BCLK3 pin Disabled 0001: BCLK3 pin acts as ASI3 BCLK as defined in B0_P4_R42_D2 0010: BCLK3 pin is used as General Purpose Input (GPI) or General Purpose Clock Input for LFR_CLKIN or HF_CLKIN 0011: BCLK3 pin Output = General Purpose Output 0100-1111: Reserved. Do not use.
D1	R	X	BCLK3 Input Pin State, used along with BCLK3 as general purpose input
D0	R/W	0	BCLK3 as General Purpose Output 0: BCLK3 General Purpose Output is '0' 1: BCLK3 General Purpose Output is '1'

5.5.54 Book 0 / Page 4 / Register 75: DOUT3 (Output) Pin Control - 0x00 / 0x04 / 0x4B (B0_P4_R75)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5	R/W	1	DOUT3 Bus Keeper Control 0: DOUT3 Bus Keeper Enabled 1: DOUT3 Bus Keeper Disabled
D4-D1	R/W	0 001	DOUT3 Pin Control 0000: DOUT3 pin disabled 0001: DOUT3 pin Output = ASI3 Data Output 0010: DOUT3 pin Output = General Purpose Output 0011-1101: Reserved. Do not use. 1110: DOUT3 pin Output = ASI1 Word Clock Output 1111: Reserved. Do not use.
D0	R/W	0	DOUT3 as General Purpose Output 0: DOUT3 General Purpose Output is '0' 1: DOUT3 General Purpose Output is '1'

5.5.55 Book 0 / Page 4 / Register 76: DIN3 (Input) Pin Control - 0x00 / 0x04 / 0x4C (B0_P4_R76)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D5	R/W	01	DIN3 Pin Control 00: DIN3 Disabled 01: DIN3 Enabled (can be used as Data Input of ASI3) 10-11: Reserved. Do not use.
D4	R	X	DIN3 Input Pin State, used along with DIN3 as general purpose input

Book 0 / Page 4 / Register 76: DIN3 (Input) Pin Control - 0x00 / 0x04 / 0x4C (B0_P4_R76) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R	0000	Reserved. Write only reset values.

5.5.56 Book 0 / Page 4 / Register 77-81: Reserved Registers - 0x00 / 0x04 / 0x4D-0x51 (B0_P4_R77-81)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

5.5.57 Book 0 / Page 4 / Register 82: MCLK2 (Input) Pin Control - 0x00 / 0x04 / 0x52 (B0_P4_R82)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D4	R/W	00	MCLK2 Pin Control 00: MCLK2 Disabled 01: MCLK2 Enabled (can be used as Dig_Mic_In, or ClockGen Block) 10-11: Reserved.
D3-D2	R	00	Reserved. Write only reset values.
D1	R/W	X	MCLK2 Input Pin State, used along with MCLK2 as general purpose input
D0	R	0	Reserved. Write only reset values.

5.5.58 Book 0 / Page 4 / Register 83-85: Reserved Registers - 0x00 / 0x04 / 0x53-0x55 (B0_P4_R83-85)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

5.5.59 Book 0 / Page 4 / Register 86: GPIO1 (Input/Output) Pin Control - 0x00 / 0x04 / 0x56 (B0_P4_R86)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D2	R/W	000 00	GPIO1 Pin Control 00000: GPIO1 pin input/output disabled. 00001: GPIO1 pin = Input Mode, which can be used for Data Input for ASI1, digital microphone input, clock input, or general purpose input 00010: Reserved. Do not use. 00011: GPIO1 pin = General Purpose Output 00100: GPIO1 pin = CLKOUT Output or WCLK1 Output (as defined in B0_P4_R10_D[7:5]) 00101: GPIO1 pin = INT1 Interrupt Output 00110: GPIO1 pin = INT2 Interrupt Output 00111-1001: Reserved. Do not use. 01010: GPIO1 pin = ADC_MOD_CLK Output for digital microphone 01011: Reserved. Do not use. 01100: GPIO1 pin = SAR ADC interrupt as defined in B0_P3 01101-01111: Reserved. Do not use. 10000: GPIO1 pin = Audio Serial Interface 1 ADC WCLK Output 10001: GPIO1 pin = Audio Serial Interface 1 ADC BCLK Output 10010: GPIO1 pin = Audio Serial Interface 2 ADC WCLK Output 10011: GPIO1 pin = Audio Serial Interface 2 ADC BCLK Output 10100: GPIO1 pin = Audio Serial Interface 3 ADC WCLK Output 10101: GPIO1 pin = Audio Serial Interface 3 ADC BCLK Output 10110-11111: Reserved. Do not use.
D1	R	X	GPIO1 Input Pin state, used along with GPIO1 as general purpose input
D0	R/W	0	GPIO1 as General Purpose Output 0: GPIO1 pin is driven to '0' in general purpose output mode 1: GPIO1 pin is driven to '1' in general purpose output mode

5.5.60 Book 0 / Page 4 / Register 87: GPIO2 (Input/Output) Pin Control - 0x00 / 0x04 / 0x57 (B0_P4_R87)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values
D6-D2	R/W	000 00	GPIO2 Pin Control 00000: GPIO2 pin input/output disabled. 00001: GPIO2 pin = Input Mode, which can be used for Data Input for ASI1, digital microphone input, or general purpose input. 00010: Reserved. Do not use. 00011: GPIO2 pin = General Purpose Output 00100: GPIO2 pin = CLKOUT Output or BCLK1 Output (as defined in B0_P4_R10_D[4:2]) 00101: GPIO2 pin = INT1 Interrupt Output 00110: GPIO2 pin = INT2 Interrupt Output 00111-01001: Reserved. Do not use. 01010: GPIO2 pin = ADC_MOD_CLK Output for digital microphone 01011: Reserved. Do not use. 01100: GPIO2 pin = SAR ADC interrupt as defined in B0_P3 01101-01111: Reserved. Do not use. 10000: GPIO2 pin = Audio Serial Interface 1 ADC WCLK Output 10001: GPIO2 pin = Audio Serial Interface 1 ADC BCLK Output 10010: GPIO2 pin = Audio Serial Interface 2 ADC WCLK Output 10011: GPIO2 pin = Audio Serial Interface 2 ADC BCLK Output 10100: GPIO2 pin = Audio Serial Interface 3 ADC WCLK Output 10101: GPIO2 pin = Audio Serial Interface 3 ADC BCLK Output 10110-11111: Reserved. Do not use.
D1	R	X	GPIO2 Input Pin state, used along with GPIO2 as general purpose input
D0	R/W	0	GPIO2 as General Purpose Output 0: GPIO2 pin is driven to '0' in general purpose output mode 1: GPIO2 pin is driven to '1' in general purpose output mode

5.5.61 Book 0 / Page 4 / Register 88-90: Reserved Registers - 0x00 / 0x04 / 0x58-0x5A (B0_P4_R88-90)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

5.5.62 Book 0 / Page 4 / Register 91: GPI1 (Input) Pin Control - 0x00 / 0x04 / 0x5B (B0_P4_R91)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only reset values.
D2-D1	R/W	01	GPI1 Pin Control 00: GPI1 pin Disabled 01: GPI1 pin Enabled (If device is in SPI mode then this pin is used as SCLK, in I2C mode this pin can be used as Digital Microphone input, ClockGen block input, or General Purpose Input) 10-11: Reserved. Do not use.
D0	R	0	GPI1 Input Pin state, used along with GPI1 as general purpose input

5.5.63 Book 0 / Page 4 / Register 92: GPI2 (Input) Pin Control - 0x00 / 0x04 / 0x5C (B0_P4_R92)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only reset values.
D5-D4	R/W	00	00: GPI2 pin Disabled (Input buffer powered down) 01: GPI2 pin Enabled (used as Dig_Mic_In, Data for ASI1, in ClockGen block, General Purpose Input) 10-11: Reserved. Do not use.
D3-D1	R	000	Reserved. Write only reset values.
D0	R	0	GPI2 Input Pin state, used along with GPI2 as general purpose input

5.5.64 Book 0 / Page 4 / Register 93-95: Reserved Registers - 0x00 / 0x04 / 0x5D-0x5F

(B0_P4_R93-95)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values

5.5.65 Book 0 / Page 4 / Register 96: GPO1 (Output) Pin Control - 0x00 / 0x04 / 0x60 (B0_P4_R96)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values
D4-D1	R/W	0 001	GPO1 Pin Control 0000: GPO1 pin output disabled 0001: GPO1 pin is used for data output in SPI interface (MISO), is disabled for I2C interface 0010: GPO1 pin is General Purpose Output 0011: GPO1 pin is CLKOUT Output 0100: GPO1 pin is INT1 Interrupt Output 0101: GPO1 pin is INT2 Interrupt Output 0110: Reserved. Do not use. 0111: GPO1 pin is ADC_MOD_CLK Output for Digital Microphone 1000-1011: Reserved. Do not use. 1100: GPO1 pin is SAR ADC interrupt as defined in B0_P3 1101-1110: Reserved. Do not use 1111: GPO1 pin is Data Output for ASI1
D0	R/W	0	GPO1 as General Purpose Output 0: GPO1 General Purpose Output Value = 0 1: GPO1 General Purpose Output Value = 1

5.5.66 Book 0 / Page 4 / Register 97-100: Reserved Registers - 0x00 / 0x04 / 0x61-0x64 (B0_P4_R97-100)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.5.67 Book 0 / Page 4 / Register 101: Digital Microphone Input Pin Control - 0x00 / 0x04 / 0x65 (B0_P4_R101)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only reset values.

Book 0 / Page 4 / Register 101: Digital Microphone Input Pin Control - 0x00 / 0x04 / 0x65 (B0_P4_R101) (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D0	R/W	0 0110	Digital Microphone Data Input Control 00000: Left Channel on GPI1 Rising Clock Edge, Right Channel on GPI1 Falling Clock Edge 00001: Left Channel on GPI2 Rising Clock Edge, Right Channel on GPI2 Falling Clock Edge 00010: Left Channel on DIN1 Rising Clock Edge, Right Channel on DIN1 Falling Clock Edge 00011: Left Channel on DIN2 Rising Clock Edge, Right Channel on DIN2 Falling Clock Edge 00100: Left Channel on GPIO1 Rising Clock Edge, Right Channel on GPIO1 Falling Clock Edge 00101: Left Channel on GPIO2 Rising Clock Edge, Right Channel on GPIO2 Falling Clock Edge 00110: Left Channel on MCLK2 Rising Clock Edge, Right Channel on MCLK2 Falling Clock Edge 00111: Left Channel on GPI1 Rising Clock Edge, Right Channel on GPI2 Rising Clock Edge 01000: Left Channel on GPI1 Rising Clock Edge, Right Channel on DIN1 Rising Clock Edge 01001: Left Channel on GPI1 Rising Clock Edge, Right Channel on DIN2 Rising Clock Edge 01010: Left Channel on GPI1 Rising Clock Edge, Right Channel on GPIO1 Rising Clock Edge 01011: Left Channel on GPI1 Rising Clock Edge, Right Channel on GPIO2 Rising Clock Edge 01100: Left Channel on GPI1 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 01101: Left Channel on GPI2 Rising Clock Edge, Right Channel on DIN1 Rising Clock Edge 01110: Left Channel on GPI2 Rising Clock Edge, Right Channel on DIN2 Rising Clock Edge 01111: Left Channel on GPI2 Rising Clock Edge, Right Channel on GPIO1 Rising Clock Edge 10000: Left Channel on GPI2 Rising Clock Edge, Right Channel on GPIO2 Rising Clock Edge 10001: Left Channel on GPI2 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 10010: Left Channel on DIN1 Rising Clock Edge, Right Channel on DIN2 Rising Clock Edge 10011: Left Channel on DIN1 Rising Clock Edge, Right Channel on GPIO1 Rising Clock Edge 10100: Left Channel on DIN1 Rising Clock Edge, Right Channel on GPIO2 Rising Clock Edge 10101: Left Channel on DIN1 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 10110: Left Channel on DIN2 Rising Clock Edge, Right Channel on GPIO1 Rising Clock Edge 10111: Left Channel on DIN2 Rising Clock Edge, Right Channel on GPIO2 Rising Clock Edge 11000: Left Channel on DIN2 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 11001: Left Channel on GPIO1 Rising Clock Edge, Right Channel on GPIO2 Rising Clock Edge 11010: Left Channel on GPIO1 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 11011: Left Channel on GPIO2 Rising Clock Edge, Right Channel on MCLK2 Rising Clock Edge 11100-11111: Reserved. Do not use.

5.5.68 Book 0 / Page 4 / Register 102-117: Reserved Registers - 0x00 / 0x04 / 0x66-0x75 (B0_P4_R102-117)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.5.69 Book 0 / Page 4 / Register 118: ADC/DAC Data Port Control - 0x00 / 0x04 / 0x76 (B0_P4_R118)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only reset values.
D6	R/W	0	ADC Data Output Configuration 0: Independent Left and Right Channels for ADC digital output 1: Left Channel of ADC digital output copied to Right Channel digital output
D5-D4	R/W	00	DAC Data Input Configuration 00: DAC receives data from ASI1 output 01: DAC receives data from ASI2 output 10: DAC receives data from ASI3 output 11: DAC receives data from ADC digital output (ADC-to-DAC Loopback)
D3-D0	R/W	0110	Reserved. Do not use.

5.5.70 Book 0 / Page 4 / Register 119: Digital Audio Engine Synchronization Control - 0x00 /

0x04 / 0x77 (B0_P4_R119)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	11	DAC Engine Synchronization: 00: Enable DAC engine syncing using Audio Serial Interface 1 01: Enable DAC engine syncing using Audio Serial Interface 2 10: Enable DAC engine syncing using Audio Serial Interface 3 11: Disable DAC engine syncing with data input frame from Audio Serial Interface mux at power up
D5-D4	R/W	11	ADC Engine Synchronization: 00: Enable ADC engine syncing using Audio Serial Interface 1 01: Enable ADC engine syncing using Audio Serial Interface 2 10: Enable ADC engine syncing using Audio Serial Interface 3 11: Disable ADC engine syncing with data output frame from Audio Serial Interface mux at power up
D3-D0	R	0000	Reserved. Write only reset values.

5.5.71 Book 0 / Page 4 / Register 120-127: Reserved Registers - 0x00 / 0x04 / 0x78-0x7F (B0_P4_R120-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	Reserved. Write only reset values.

5.6 Book 0 Page 252

5.6.1 Book 0 / Page 252 / Register 0: Page Select Register - 0x00 / 0xFC / 0x00 (B0_P252_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command.

5.6.2 Book 0 / Page 252 / Register 1: SAR Buffer Mode Data (MSB) and Buffer Flags - 0x00 / 0xFC / 0x01 (B0_P252_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Buffer-Full Flag 0: 64-sample Buffer is not filled 1: 64-sample Buffer has been filled
D6	R	1	Buffer-Empty Flag 0: Buffer still contains un-read data 1: Buffer is empty (contains no un-read data)
D5	R	X	Reserved. Write only reset values.
D4	R	X	Data Identification: 0: VBAT or IN1R/AUX2 data found in SAR Buffer Data (i.e. B0_P252_R1_D[3:0] and B0_P252_R2_D[7:0]. 1: IN1L/AUX1 or TEMP data found in SAR Buffer Data (i.e. B0_P252_R1_D[3:0] and B0_P252_R2_D[7:0].
D3-D0	R	XXXX	SAR ADC Buffer Mode Data (11:8) - Reading this register will return MSB 4 bits of SAR Buffer Mode data (based on Read Pointer).

5.6.3 Book 0 / Page 252 / Register 2: SAR Buffer Mode Data (LSB) - 0x00 / 0xFC / 0x02 (B0_P252_R2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	SAR ADC Buffer Mode Data (7:0) - Reading this register will return LSB 8 bits of SAR Buffer Mode data (based on Read Pointer).

5.6.4 Book 0 / Page 252 / Register 3-127: Reserved Registers - 0x00 / 0xFC / 0x03-0x7F

(B0_P252_R3-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.7 Book 40 Page 0

5.7.1 Book 40 / Page 0 / Register 0: Page Select Register - 0x28 / 0x00 / 0x00 (B40_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.7.2 Book 40 / Page 0 / Register 1: ADC Adaptive CRAM Configuration Register - 0x28 / 0x00 / 0x01 (B40_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only reset values.
D2	R/W	0	ADC Adaptive Filtering Control 0: Adaptive Filtering disabled for ADC 1: Adaptive Filtering enabled for ADC
D1	R	0	ADC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-A, and control interface accesses ADC Coefficient Buffer-B 1: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-B, and control interface accesses ADC Coefficient Buffer-A
D0	R/W	0	ADC Adaptive Filter Buffer Switch control 0: ADC Coefficient Buffers will not be switched at next frame boundary 1: ADC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

5.7.3 Book 40 / Page 0 / Register 2-126: Reserved Registers - 0x28 / 0x00 / 0x02-0x7E (B40_P0_R2-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.7.4 Book 40 / Page 0 / Register 127: Book Selection Register - 0x28 / 0x00 / 0x7F (B40_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

5.8 Book 40 Page 1-17

5.8.1 Book 40 / Page 1-17 / Register 0: Page Select Register - 0x28 / 0x01-0x11 / 0x00 (B40_P1-17_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.8.2 Book 40 / Page 1-17 / Register 1-7: Reserved Registers - 0x28 / 0x01-0x11 / 0x01-0x07 (B40_P1-17_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.8.3 Book 40 / Page 1-17 / Register 8-127: ADC Adaptive Coefficients C(0:509) - 0x28 / 0x01-0x11 / 0x08-0x7F (B40_P1-17_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficients. Refer to Tables "ADC Adaptive Coefficient Buffer-A Map" and "ADC Adaptive Coefficient Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, ADC Coefficients are one contiguous block.

5.9 Book 40 Page 18

5.9.1 Book 40 / Page 18 / Register 0: Page Select Register - 0x28 / 0x12 / 0x00 (B40_P18_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.9.2 Book 40 / Page 18 / Register 1-7: Reserved Registers - 0x28 / 0x12 / 0x01-0x07 (B40_P18_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.9.3 Book 40 / Page 18 / Register 8-15: ADC Adaptive Coefficients C(510:511) - 0x28 / 0x12 / 0x08-0x0F (B40_P18_R8-15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficients. Refer to Tables "ADC Adaptive Coefficient Buffer-A Map" and "ADC Adaptive Coefficient Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, ADC Coefficients are one contiguous block.

5.9.4 Book 40 / Page 18 / Register 16-127: Reserved Registers - 0x28 / 0x12 / 0x10-0x7F (B40_P18_R16-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	Reserved. Write only reset values.

5.10 Book 80 Page 0

5.10.1 Book 80 / Page 0 / Register 0: Page Select Register - 0x50 / 0x00 / 0x00 (B80_P0_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.10.2 Book 80 / Page 0 / Register 1: DAC Adaptive Coefficient Bank Configuration Register -

0x50 / 0x00 / 0x01 (B80_P0_R1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only reset values.
D2	R/W	0	DAC Adaptive Filtering Control 0: Adaptive Filtering disabled for DAC Adaptive Coefficient Bank 1: Adaptive Filtering enabled for DAC Adaptive Coefficient Bank
D1	R	0	DAC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC accesses DAC Coefficient Bank Buffer-A, and control interface accesses DAC Coefficient Bank Buffer-B 1: In adaptive filter mode, DAC accesses DAC Coefficient Bank Buffer-B, and control interface accesses DAC Coefficient Bank Buffer-A
D0	R/W	0	DAC Bank Adaptive Filter Buffer Switch control 0: DAC Coefficient Bank Buffers will not be switched at next frame boundary 1: DAC Coefficient Bank Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

5.10.3 Book 80 / Page 0 / Register 2-126: Reserved Registers - 0x50 / 0x00 / 0x02-0x7E (B80_P0_R2-126)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.10.4 Book 80 / Page 0 / Register 127: Book Selection Register - 0x50 / 0x00 / 0x7F (B80_P0_R127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	0000 0000: Book 0 selected 0000 0001: Book 1 selected ... 1111 1110: Book 254 selected 1111 1111: Book 255 selected

5.11 Book 80 Page 1-17

5.11.1 Book 80 / Page 1-17 / Register 0: Page Select Register - 0x50 / 0x01-0x11 / 0x00 (B80_P1-17_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.11.2 Book 80 / Page 1-17 / Register 1-7: Reserved Registers - 0x50 / 0x01-0x11 / 0x01-0x07 (B80_P1-17_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

5.11.3 Book 80 / Page 1-17 / Register 8-127: DAC Adaptive Coefficient Bank C(0:509) - 0x50 / 0x01-0x11 / 0x08-0x7F (B80_P1-17_R8-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank. Refer to Tables "DAC Adaptive Coefficient Bank Buffer-A Map" and "DAC Adaptive Coefficient Bank Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

5.12 Book 80 Page 18

5.12.1 Book 80 / Page 18 / Register 0: Page Select Register - 0x50 / 0x12 / 0x00 (B80_P18_R0)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.12.2 Book 80 / Page 18 / Register 1-7: Reserved Registers - 0x50 / 0x12 / 0x01-0x07 (B80_P18_R1-7)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only reset values.

5.12.3 Book 80 / Page 18 / Register 8-15: DAC Adaptive Coefficient Bank C(510:511) - 0x50 / 0x12 / 0x08-0x0F (B80_P18_R8-15)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Adaptive Coefficient Bank. Refer to Tables "DAC Adaptive Coefficient Bank Buffer-A Map" and "DAC Adaptive Coefficient Bank Buffer-B Map" for details in adaptive mode. If these coefficients are set to fixed mode, these DAC Coefficients are one contiguous block.

5.12.4 Book 80 / Page 18 / Register 16-127: Reserved Registers - 0x50 / 0x12 / 0x10-0x7F (B80_P18_R16-127)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	Reserved. Write only reset values.

5.13 ADC Coefficients

Table 5-2. ADC Fixed Coefficient Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	20	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	20	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	20	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	20	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	20	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	20	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	20	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	20	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	20	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	20	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	20	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	20	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	20	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-2. ADC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C180	20	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	20	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	20	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	20	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	20	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C269	20	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C270	20	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C299	20	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C300	20	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C329	20	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C330	20	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C359	20	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C360	20	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C389	20	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C390	20	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C419	20	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C420	20	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C449	20	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C450	20	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C479	20	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C480	20	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C509	20	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C510	20	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C539	20	18	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C540	20	19	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C569	20	19	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C570	20	20	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C599	20	20	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C600	20	21	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C629	20	21	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C630	20	22	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..

Table 5-2. ADC Fixed Coefficient Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C659	20	22	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C660	20	23	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C689	20	23	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C690	20	24	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C719	20	24	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C720	20	25	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C749	20	25	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C750	20	26	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C767	20	26	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-3. ADC Adaptive Coefficient Buffer-A Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	40	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	40	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	40	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	40	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	40	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	40	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	40	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	40	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	40	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	40	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	40	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	40	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	40	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	40	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	40	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	40	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	40	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	40	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C255	40	9	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-4. ADC Adaptive Coefficient Buffer-B Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	40	9	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	40	9	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C13	40	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C14	40	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C43	40	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C44	40	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C73	40	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C74	40	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C103	40	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C104	40	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C133	40	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C134	40	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C163	40	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C164	40	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C193	40	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C194	40	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C223	40	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C224	40	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C253	40	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C254	40	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C255	40	18	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

5.14 ADC Defaults

Table 5-5. Default values of ADC Coefficients in Buffers A and B

ADC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	01170000H
C2	01170000H
C3	7DD30000H
C4	7FFFFF00H
C5,C6	00000000H
C7	7FFFFF00H
C8,..,C11	00000000H
C12	7FFFFF00H

Table 5-5. Default values of ADC Coefficients in Buffers A and B (continued)

ADC Buffer-A,B Coefficients	Default Value at reset
C13,..,C16	00000000H
C17	7FFFFF00H
C18,..,C21	00000000H
C22	7FFFFF00H
C23,..,C26	00000000H
C27	7FFFFF00H
C28,..,C35	00000000H
C36	7FFFFF00H
C37,C38	00000000H
C39	7FFFFF00H
C40,..,C43	00000000H
C44	7FFFFF00H
C45,..,C48	00000000H
C49	7FFFFF00H
C50,..,C53	00000000H
C54	7FFFFF00H
C55,..,C58	00000000H
C59	7FFFFF00H
C60,..,C255	00000000H

5.15 DAC Coefficients

Table 5-6. DAC Adaptive Coefficient Bank Buffer-A Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	80	1	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	80	1	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C29	80	1	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	80	2	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C59	80	2	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	80	3	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C89	80	3	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	80	4	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C119	80	4	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	80	5	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C149	80	5	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	80	6	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C179	80	6	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-6. DAC Adaptive Coefficient Bank Buffer-A Map (continued)

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C180	80	7	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C209	80	7	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	80	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C239	80	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	80	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C255	80	9	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-7. DAC Adaptive Coefficient Bank Buffer-B Map

Coef No	Book No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	80	9	72	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	80	9	76	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C13	80	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C14	80	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C43	80	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C44	80	11	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C73	80	11	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C74	80	12	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C103	80	12	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C104	80	13	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C133	80	13	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C134	80	14	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C163	80	14	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C164	80	15	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C193	80	15	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C194	80	16	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C223	80	16	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C224	80	17	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
		..	..	..	..	..	..
C253	80	17	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C254	80	18	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C255	80	18	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

5.16 DAC Defaults

Table 5-8. Default values of DAC Coefficient Bank in Buffers A and B

DAC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	7FFFFF00H
C2,..,C5	00000000H
C6	7FFFFF00H
C7,..,C10	00000000H
C11	7FFFFF00H
C12,..,C15	00000000H
C16	7FFFFF00H
C17,..,C20	00000000H
C21	7FFFFF00H
C22,..,C25	00000000H
C26	7FFFFF00H
C27,..,C30	00000000H
C31,C32	00000000H
C33	7FFFFF00H
C34,..,C37	00000000H
C38	7FFFFF00H
C39,..,C42	00000000H
C43	7FFFFF00H
C44,..,C47	00000000H
C48	7FFFFF00H
C49,..,C52	00000000H
C53	7FFFFF00H
C54,..,C57	00000000H
C58	7FFFFF00H
C59,..,C64	00000000H
C65	7FFFFF00H
C66,C67	00000000H
C68	7FFFFF00H
C69,C70	00000000H
C71	7FF70000H
C72	10090000H
C73	7FEF0000H
C74,C75	00110000H
C76	7FDE0000H
C77,..,C255	00000000H

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