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TLV1572EVM Evaluation Module for the TLV1572 10-Bit ADC

User's Guide

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Preface

Read This First

About This Manual

This User's Guide describes the characteristics, operation, and use of the 10-bit TLC1572 Analog-to-Digital Converter (ADC) Evaluation Module.

How to Use This Manual

This document contains the following chapters:

- ❑ Chapter 1 Overview
- ❑ Chapter 2 Physical Description
- ❑ Chapter 3 Circuit Description
- ❑ Chapter 4 Operation

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- TPS7101QD — Literature No. SLVS092
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Application Reports:

- *Interfacing the TLV1572 Analog-to-Digital Converter to the TMS320C203 DSP*, literature number SLAA026.

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Chapter 1

Overview

This chapter gives a general overview of the TLV1572 Evaluation Module (EVM), and describes some of the factors that must be considered in using the module.

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1.1 Purpose

The TLC1572 Evaluation Module (EVM) provides a platform for evaluating the TLV1572 10-Bit Analog-to-Digital Converter (ADC) under various signal, reference, and supply conditions.

1.2 EVM Basic Function

The EVM allows for observation and evaluation of an on board buffered potentiometer dc input, an operational amplifier buffered input, and an unbuffered direct input. The ADC digital I/O is buffered through a SN74AHC244 bus transceiver for driving an interconnect cable, and these I/O lines have in-line terminations on board to minimize overshoot. There are four integrated circuits on the board:

- U1 TLV1572 10-bit analog to digital converter with serial I/O
- U2 SN74AHC244 I/O digital buffer for the ADC
- U3 TPS7101 Low drop-out adjustable regulator
- U4 TLV2432 Single supply. 5/3 volta dual operational amplifier

Recommended power supply voltage for the EVM is 10 V maximum to 7 V minimum; ground is applied through connector J1.

The TPS7101 regulates for 5 V, or approximately 2.7 V V_{DD} through jumper JP1, such that the ADC evaluation can be done at either V_{DD}. JP1 also changes the SN74HC244 V_{DD} to 3 V.

The ADC has one analog input designated by AIN. Through jumper placement, AIN can receive an input from four sources as follows:

- Input 1. Jumper array JP3 provides a simple zero, half, and full scale input. This input is supplied to the device AIN through JP2, position 1.
- Input 2. One half of the TLV2432 single-supply operational amplifier is connected as a gain-of-two amplifier with a potentiometer on the noninverting input for dc input adjustment throughout the range. This input is selected by JP2, position 3.
- Input 3. The other half of the TLV2432 is connected as a noninverting gain-of-two amplifier. The external EVM input ANA IN BUF is applied to this amplifier through J2. This input is supplied to AIN through JP2, positiion 2.
- Input 4. This unbuffered input provides a direct input to the ADC input terminal, AIN. This input is selected through JP2, position 4.

1.3 TLV1572EVM Setup

The TLV1572EVM requires some signal setup or software. The TLV1572 data sheet provides the timing requirements and the application report SLAA026 supplies an example of software using the TMS320C203 DSP. Once the input requirements are completed, TLV1572 EVM operation is as follows.

- Connect 7 to 10 volts to the V+ terminal of J1 and ground to the ground terminal. JP1 is open for 5-volt V_{CC} and shorted for 2.7-volt V_{CC}. The 2.7-volt operation should be used only with a host interface that provides 3-volt input signals or less to the EVM.

- Use jumper array JP2 to select the analog input to the TLV1572.

JP2 Position	Analog Input
1	Full, half, and zero scale
2	External input through X2 amplifier
3	Potentiometer through X2 amplifier
4	External input unbuffered

  Use the full, half, and zero scale jumper positions of JP3 to assure proper operation.

JP3 Position	Function	
1	Full scale	All 1s
2	Half scale	Nominally a 1 and all 0s or a 0 and all 1s depending on resistor tolerance
3	Zero scale	All zeros

- The initial condition of JP4 is position 1, which selects the AV_{CC} as the reference voltage input. JP4, position 2, selects an externally applied reference voltage.

- Once the zero, half, and full scale readings are complete, the jumper selection can be JP3, position 3. This selection provides a potentiometer variable voltage input to the TLV1572.

- The I/O signals can be monitored at J7.

- The additional analog inputs can be used for application of external signals.

1.4 Power Requirements

The EVM operates properly over an input voltage range of 10 V maximum to 7 V minimum. The power supply and externally applied reference voltage should be supplied to the EVM through a shielded twisted pair for best performance. This type of power cabling minimizes any stray or transient pickup from the higher frequency digital circuitry.

Voltage Limits

Exceeding the 10-V maximum can damage EVM components. The positive supply can be lowered to 7 V and the EVM will maintain the 5-V supply.

1.5 I/O CLK Requirements

The I/O CLK can be 20 MHz for most of the voltage range when fast I/O is possible. The maximum I/O CLK is limited to 10 MHz for a supply voltage of 2.7 V. Table 1–1 lists the maximum I/O CLK frequencies for different supply voltages. The maximum I/O CLK frequency also depends on input source impedance.

Table 1–1. Maximum I/O CLK Frequency

V_{CC}	Maximum Internal Input Resistance (Max)	External Source Impedance	I/O CLK
2.7 V	5 K	100 Ω	10 MHz
4.5 V	1 K	100 Ω	20 MHz

1.6 I/O Interface Connector Provisions

The connector interface allows different connection arrangements depending on the user-selected interface. The 12-position single-inline male connector J4 is hard wired to the input/output signals of the TLV1572 through the SN74AHC244. Dual-row, 26-position header H1 allows any dual-row, 100-mil-center connector with up to 26 pins to be used. A jumper row that separates J4 and H1 allows H1 to be configured for the appropriate external interface. The schematic shows the signal arrangement for H1. Either J5 or H1 can easily be used with the corresponding male ribbon cable plug or connector.

Using jumpers and the two rows of plated-through holes (JPA), the user can connect the TLV1572 EVM I/O signals to a variety of external devices (DSPs EVMs, microprocessor EVM, micro-controller EVMs, etc.).

When using H1, the clock lines should have a ground line on either side in the ribbon cable to minimize cross-talk. If possible every other conductor in the ribbon cable should be grounded.

1.7 Timing and Signal Requirements

The signal timing necessary is shown in Chapter 4, Figures 4–2, 4–5, 4–7, 4–8, 4–9, and 4–10 for the various processor options.

Chapter 2

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.1 PCB Layout

The EVM is constructed on a 4-layer, 3-inch × 5-inch, 0.062-inch thick PCB using FR-4 material. Figures 2–1 through 2–5 show the individual layers.

Figure 2–1. PCB Layout

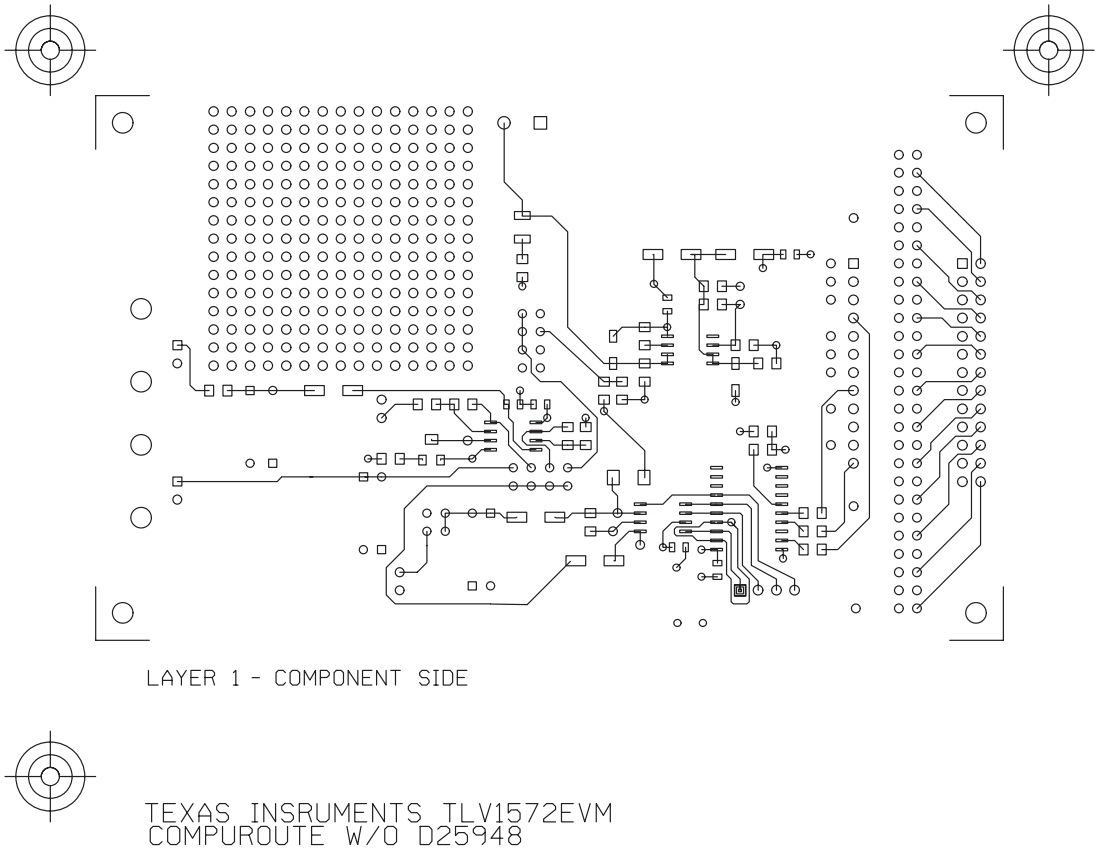


Figure 2–2. PCB Layout

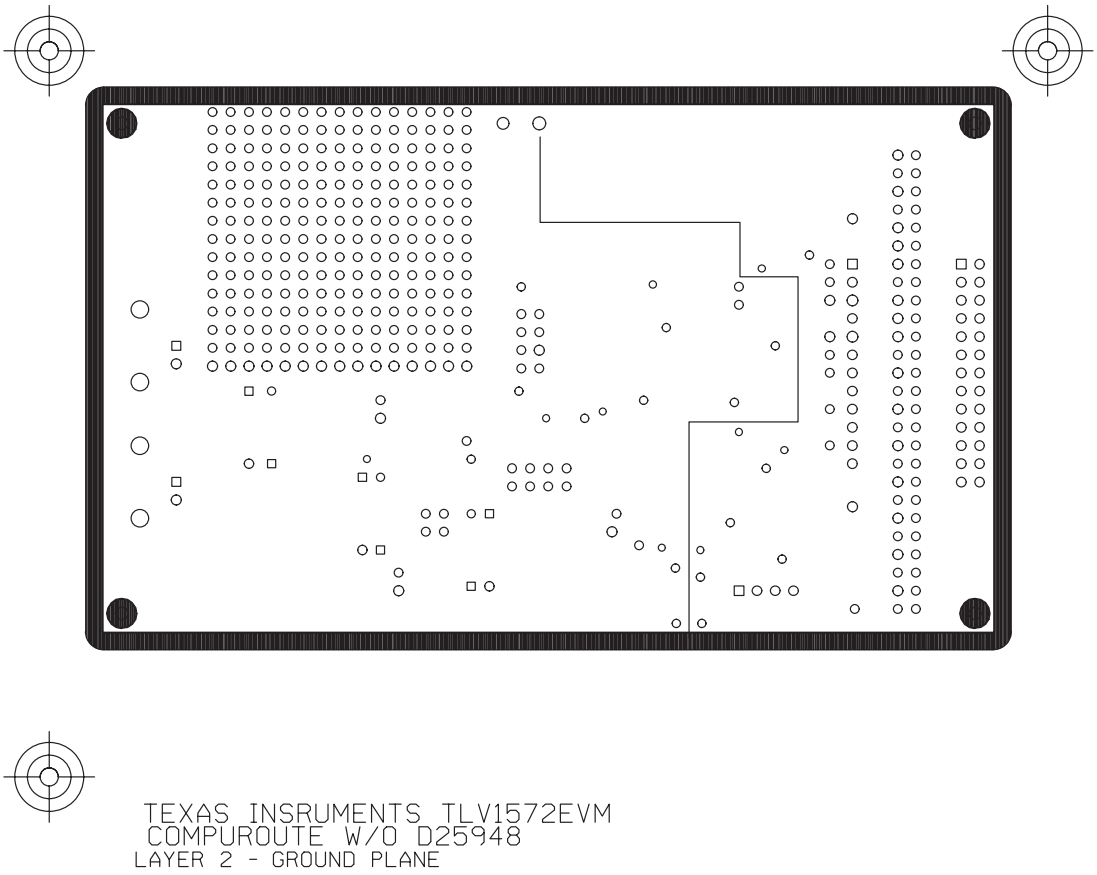


Figure 2–3. PCB Layout

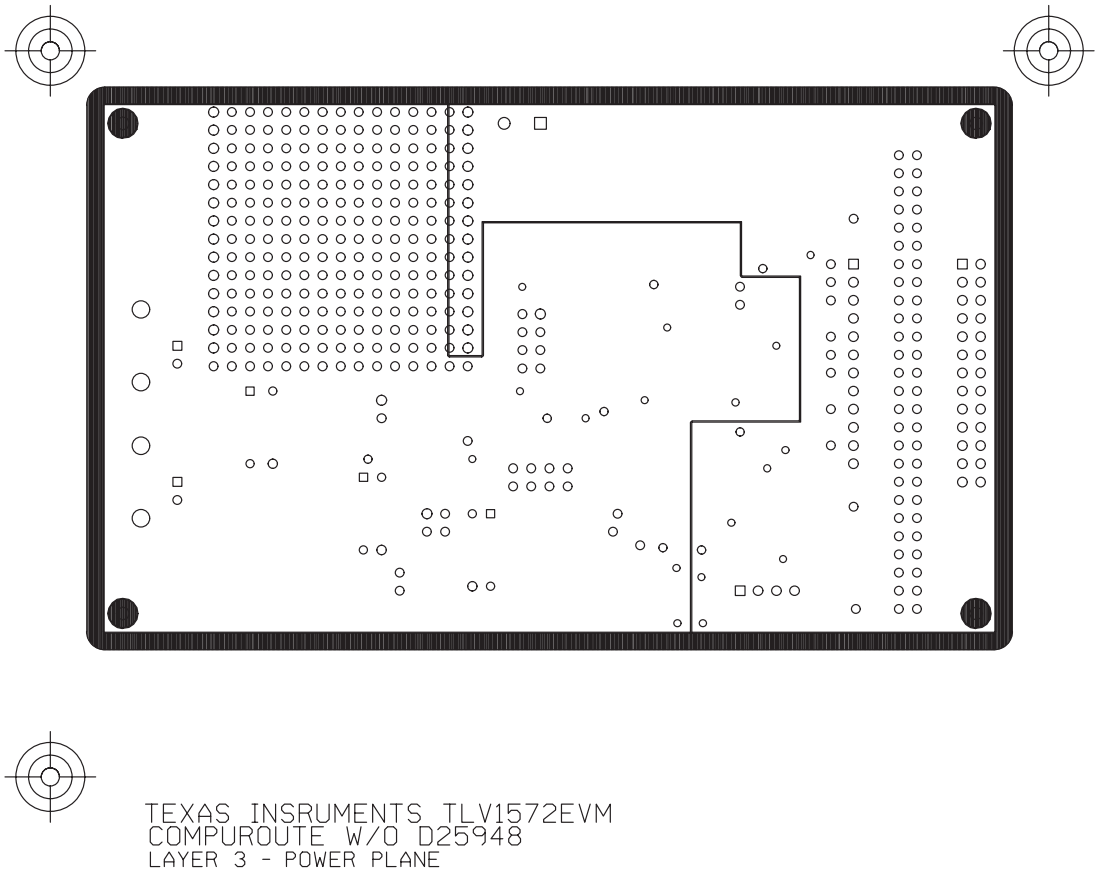


Figure 2–4. PCB Layout

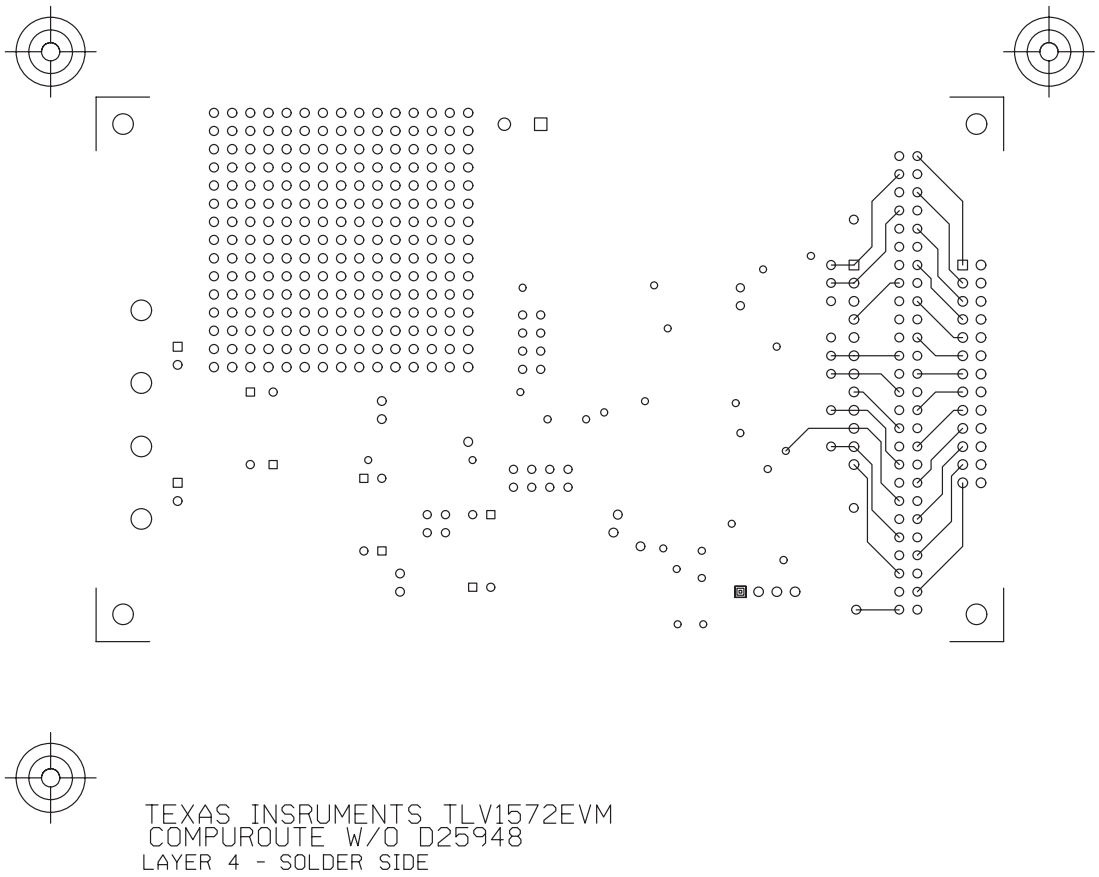
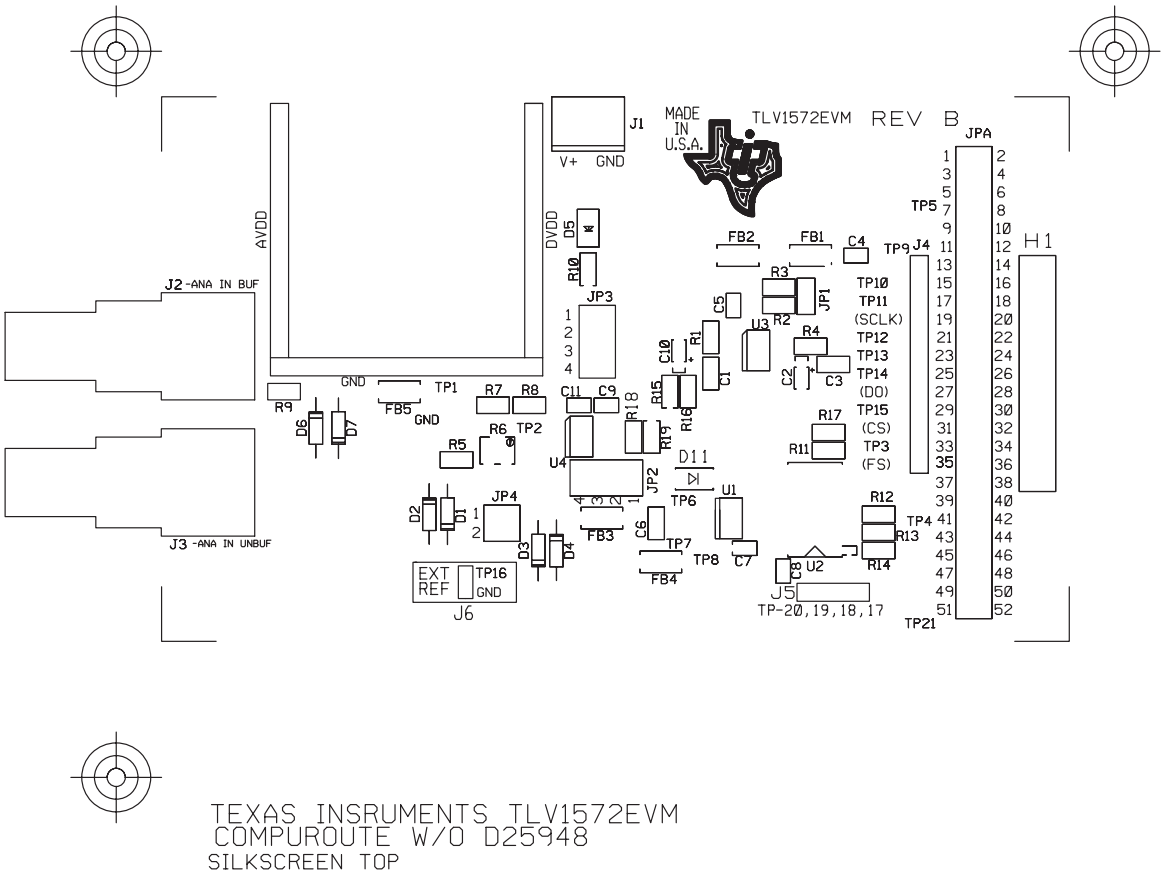


Figure 2–5. PCB Layout



TEXAS INSRUMENTS TLV1572EVM
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2.2 Component List

Table 2–1 lists the components used in constructing the EVM.

Table 2–1. Component List

Reference Designator	Value	Manufacturer	Part Number
R1, R5, R7, R8, R17, R18, R19	10 K, 1%, 1206 SMD	Panasonic	ERJ-8ENF-1002
R2	562 K, 1%, 1206 SMD	Panasonic	ERJ-8ENF-5623
R3	357 K 1%, 1206 SMD	Panasonic	ERJ-8ENF-3573
R4	169 K, 1% 1206 SMD	Panasonic	ERJ-8ENF-1693
R6	10 K potentiometer, multi-turn, SMD	Bourns	3224W-1-103D
R9, R12	100-Ω, 1%, 1206 SMD	Panasonic	ERJ-8ENF-1000
R11, R13, R14	510 Ω, 1%, 1206 SMD	Panasonic	ERJ-8ENF-5100
R10, R15, R16	1 K, 1%, 1206 SMD	Panasonic	ERJ-8ENF-1001
FB1–FB5	Ferrite bead	Fair-Rite	27-44-44447
C1, C3	0.1 μF, 1206 SMD	Panasonic	ECUV1C104KBW
C7, C8, C9	0.1 μF, 0805 SMD	Panasonic	ECUV1C104KBX
C2, C10	4.7 μF, EIA Size A	Panasonic	ECST1CY475R
C4, C5	0.01 μF, 0805 SMD	Panasonic	ECUV1H103KBG
C6	1 μF, 1206 SMD	Panasonic	ECUYC105KBW
C12	22 pF, 1206 SMD	Panasonic	ECUV1H220KCM
D1, D2, D4, D6, D7	Diode IN4148, D0–35	Phillips	1N4148
D3	Schottky	SGS	BAT81
D5	Red LED	AND	AND5RA
U1	IC, 10-bit serial out ADC	Texas Instruments	TLV1544CD
U2	IC, Digital Buffer	Texas Instruments	SN74HC244IDW
U3	IC, Low dropout voltage regulator	Texas Instruments	TPS7101QD
U4	IC, Dual single supply op amp	Texas Instruments	TLV2432AID
TP4, TP5	Standoff, Pin, 0.025'' sq.	Samtec	TWS-101-07-S-S
JP1, J6	Single jumper	Berg	68705-202
JP2	4 position jumper	Berg	68217-204
JP3	3 position jumper, 100 mil CENTER	Berg	68217-203
JP4	2 position jumper	Berg	68217-202
J1	2 terminal connector	Lumberg	KRMZ
J2, J3	BNC, right angle, through hole	AMP	227161-7
J4	12 pin, single row male	Berg	68705-212
J5	4 pin, single row male	Berg	68705-204

Chapter 3

Circuit Description

This chapter contains the EVM schematic diagram and discusses the various functions on the EVM.

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3.1 Schematic Diagram

Figure 3–1 shows the schematic diagram for the EVM. The following paragraphs describe the EVM circuits.

Figure 3–1. EVM Schematic Diagram

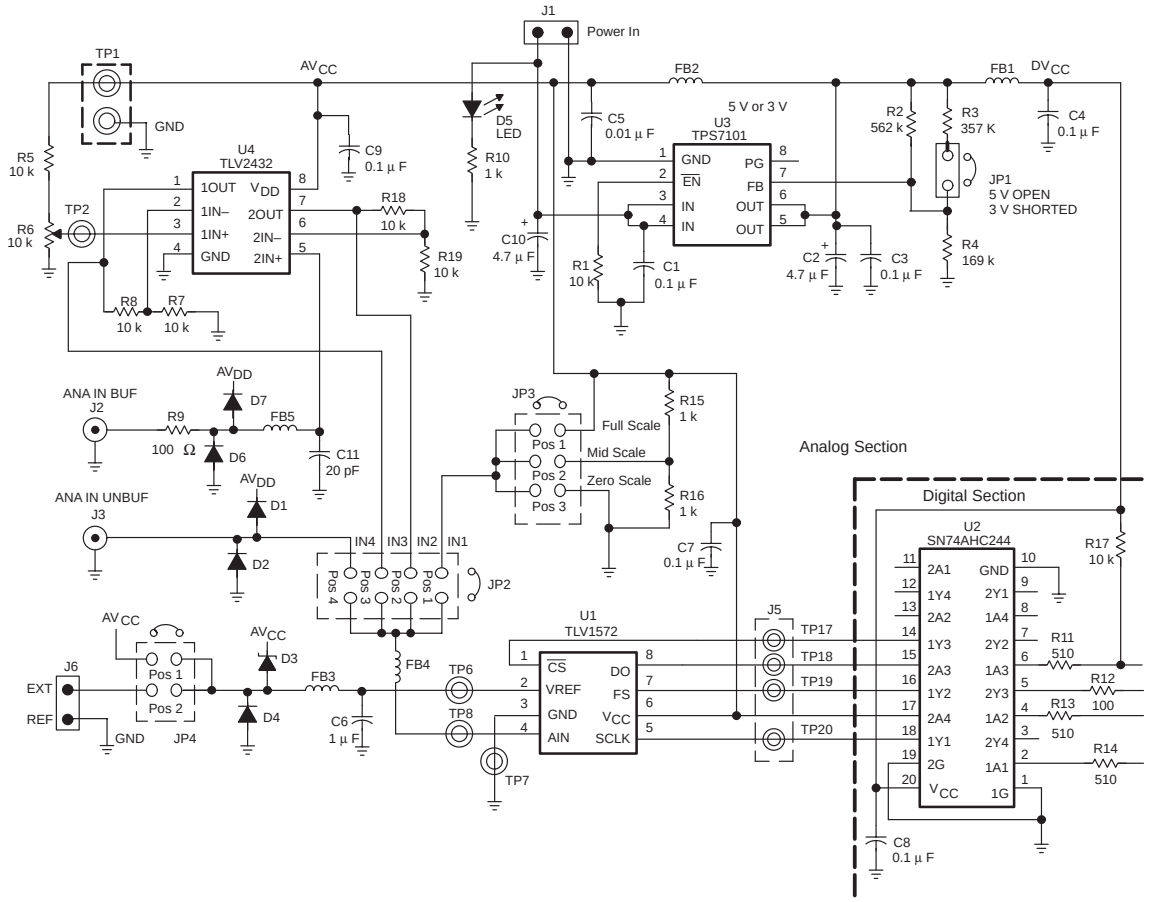
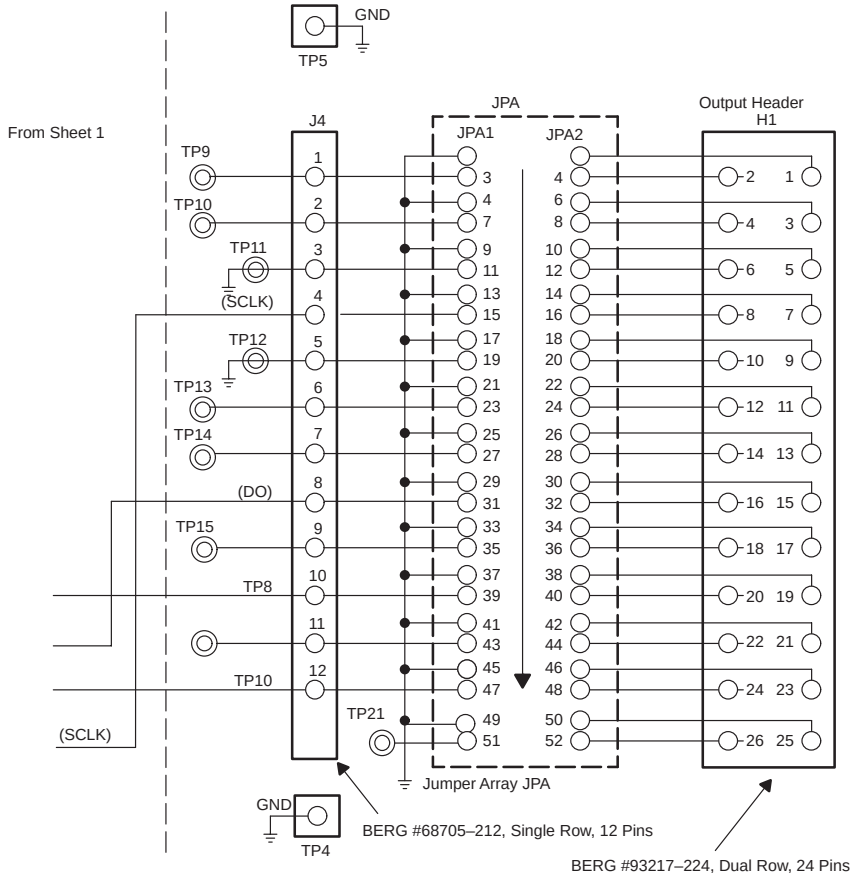


Figure 3–1. EVM Schematic Diagram (Continued)



c) Test connector, jumper array, and output header

3.2 Circuit Function

The following paragraphs describe the function of individual circuits.

3.2.1 Input 1 – Onboard Operational Check

This ADC input allows for a quick check by using the shorting plug of the nominal zero scale, half scale, and full scale. JP3, position 1, supplies the upper reference voltage. JP3, position 2, supplies an approximate midscale voltage, and JP3, position 3, supplies ground. The resistors, R15 and R16, form a low impedance divider to provide half scale voltage.

3.2.2 Input 2 – External Input with X2 Amplifier Buffer

Through JP2, position 2, the analog input to AIN connects through one amplifier of U4 connected in a noninverting gain of 2. J2 provides the external input for this buffer. The ANA IN BUF input lead is protected from voltages above and below the ADC supply by diodes, D6 and D7, and resistor R9

3.2.3 Input 3 – Voltage Variable Analog Input (Potentiometer)

Potentiometer, R6, controls the dc voltage to JP2 position 3. When the jumper is in position 3, the ADC input is the output of one section of U4, the TLV2432. This amplifier is in a noninverting gain of 2 amplifier. R5 and R6 form a voltage divider from AVDD with the R6 wiper to the noninverting input. Adjusting R6, the 10 kΩ potentiometer, through the adjustment range, changes the operational amplifier input voltage from 0 to Vdd/2. Since the amplifier has a gain of 2, the voltage to JP2–3 ranges from 0 to a nominal 5 volts. Measurements made with this analog channel are ratiometric since the input voltage varies with changes in the supply voltage. The full scale output of the TLV2432 will be approximately 10 counts below the nominal full scale digital output of all ones when using V_{CC} as the reference voltage.

3.2.4 Input 4 – Unbuffered Analog Input

J3 provides an unbuffered input to JP2, position 4. Diodes D1 and D2 with FB5 and C12 protect the TLV2432 noninverting input from moderate transient voltages in excess of the supply rails at J2.

When using the unbuffered input, the driving source impedance must be low for proper slew rate of the input signal. The source must provide enough current into 50 pF to arrive at the final voltage value within the device specified sampling time. Also, if the source noise is not below the 10 bit level, this noise could cause jitter in the least significant bit.

3.2.5 Voltage Reference Generation

Jumper JP4 selects the reference voltage source for the ADC. Position 1 selects the AV_{CC} as the reference and positiion 2 allows an external reference to be used. The external reference voltage is supplied to J6 and the corresponding ground point marked EXT REF. Care must be exercised when

using the external reference method to provide a clean, low-noise voltage at the V_{REF} terminal of the ADC. The reference voltage applied to J6 should always be equal to or greater than 2.5 volts for proper operation within the TLV1572 specified data sheet operational limits.

Ratiometric measurements are the measurements made on signals that vary with the supply voltage. If an input signal voltage is used that varies proportionately with the supply voltage, such as the on board potentiometer input, the signal is a ratio of the absolute value of the supply. Therefore, connecting the reference to the supply provides a conversion result independent of supply voltage variations.

3.2.6 Test Connector

Test connector J5 provides a convenient point for measuring the device signal. Table 3–1 lists the device test points.

Table 3–1. Test Connector J5

J5 Pin	TLV1572 pin	Function
TP17	1	$\overline{CS}$
TP18	8	DO
TP19	7	FS
TP20	5	SCLK

3.2.7 Jumper Arrangement

The EVM evaluation can begin with the following jumper condition:

- JP1 – open
- JP2 – position 1
- JP3 – position 1
- JP4 – position 1

Chapter 4

Operation

This chapter describes the basic operation of the EVM with a host DSP or processor.

Topic **Page**

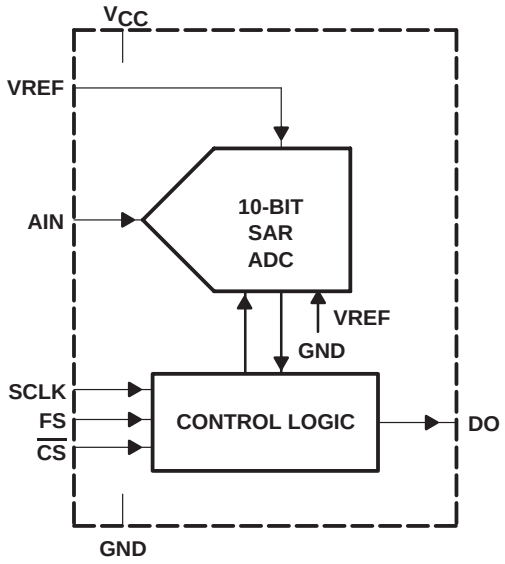
4.1 TLV1572 Description

The following paragraphs describe the TLV1572 10-bit ADC.

The TLV1572 is a 600 ns, 10-bit analog-to-digital converter with throughput to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V respectively. To run at its fastest conversion rate, the clock must be 20 MHz at 5 V or 10 MHz at 3 V. The TLV1572 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. The serial interface is designed to be fully compatible with Serial Peripheral Interface(SPI) and the TMS320 DSP serial ports. The interface requires no hardware between the TLV1572 and the microcontrollers (μCs) with the SPI serial port or the TMS320 DSPs. However, the speed may be limited by the SCLK rate of the μC or the DSP.

The TLV1572 interfaces to the DSPs over four lines: $\overline{CS}$, SCLK, DO, and FS, and interfaces to μCs over three lines: $\overline{CS}$, SCLK, and DO. The FS input should be pulled high in μC mode. The chip is in 3-state and power-down mode when the $\overline{CS}$ is high. After the $\overline{CS}$ falls, the TLV1572 checks the FS input at the $\overline{CS}$ falling edge to determine the operation mode. If the FS is low, the DSP mode is set; otherwise, the μC mode is set.

Figure 4–1. Functional Block Diagram



4.1.1 Timing Diagrams

Figures 4–2 and 4–3 show the system signal timing diagrams. These timing diagrams show the basic signal I/O signal sets required for microprocessor and DSP timing.

Figure 4–2. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = High)

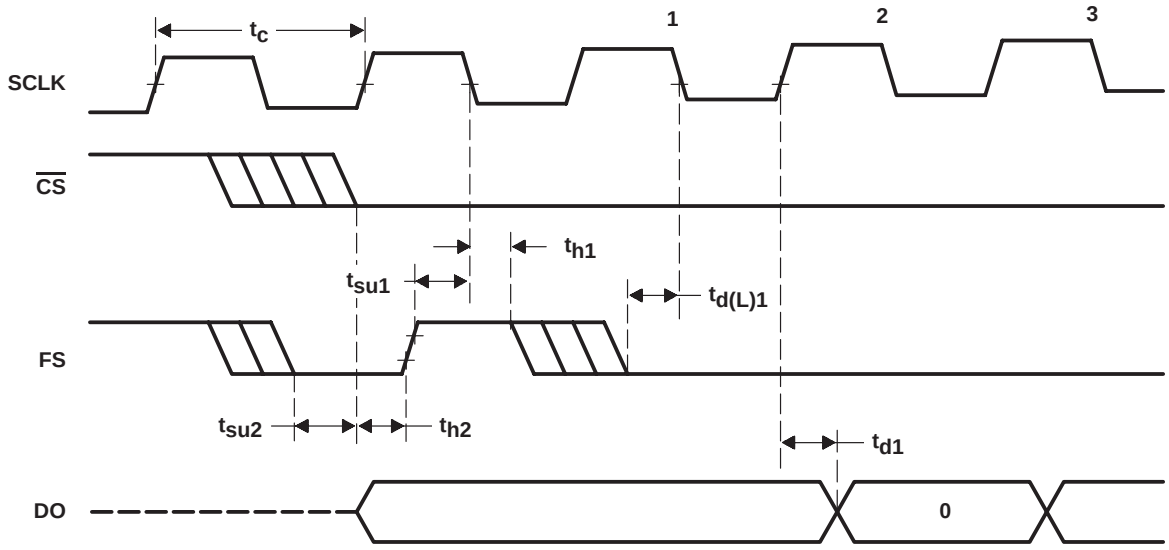
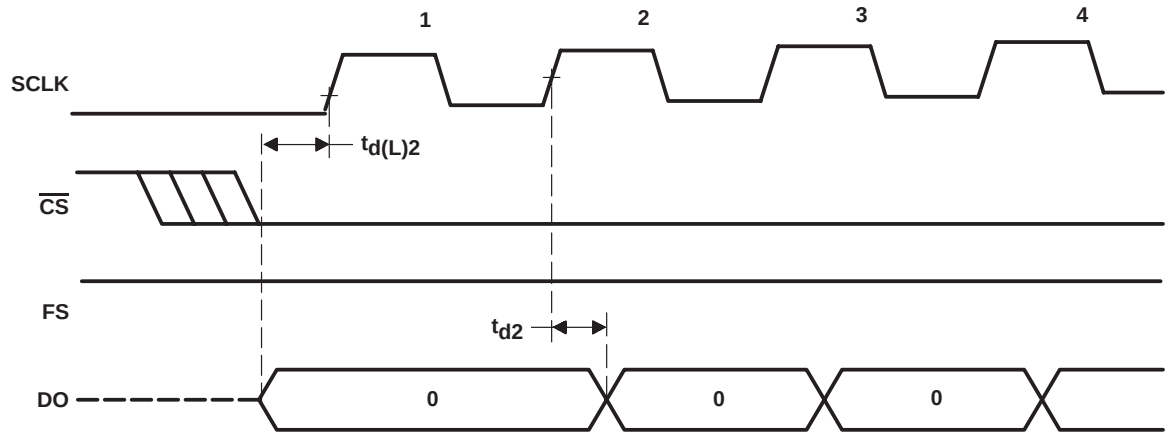


Figure 4–3. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = Low)



4.1.2 TLV1572 Terminal Functions

Table 4–1 explains the terminal functions for the TLV1572.

Table 4–1. Terminal Functions

Terminal Name	NO.	I/O	Description
$\overline{CS}$/Powerdown	1	I	Chip Select. A logic low on this input enables the TLV1572. A logic high disables the device and disconnects the power to the TLV1572.
AIN	2	I	Analog input
V_{REF}	3	I	Reference voltage input. The voltage applied to this pin defines the input span of the TLV1572.
GND	4		Ground
DO	5	O	Serial data output. A/D conversion results are provided at this output pin.
FS	6	I	Frame sync input in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1572. The FS input is tied to V_{CC} when interfacing to a microcontroller.
SCLK	7	I	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
V_{CC}	8		Power supply, recommend connection to analog supply

4.2 Interfacing TLV1572 to TMS320 DSPs

The TLV1572 is compatible with Texas Instruments TMS320 DSP serial ports. Figures 4–4(a) and 4–4(b) show the pin connections to interface the TLV1572 to the TMS320 DSPs.

Figure 4–4. DSP to TLV1570 Interface

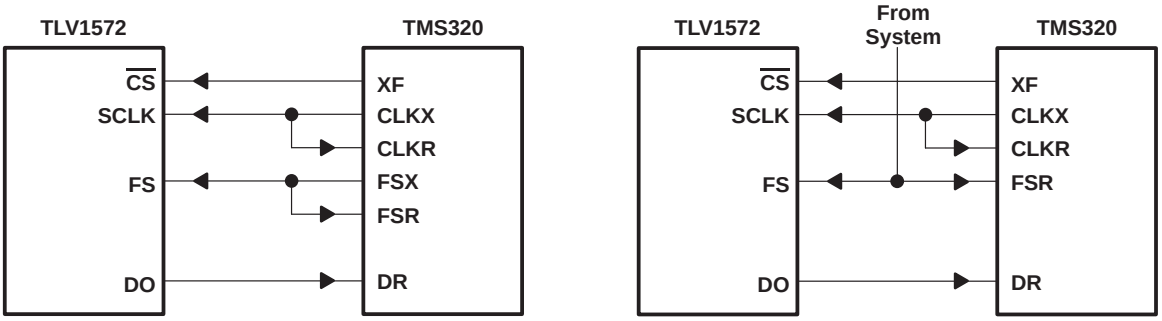
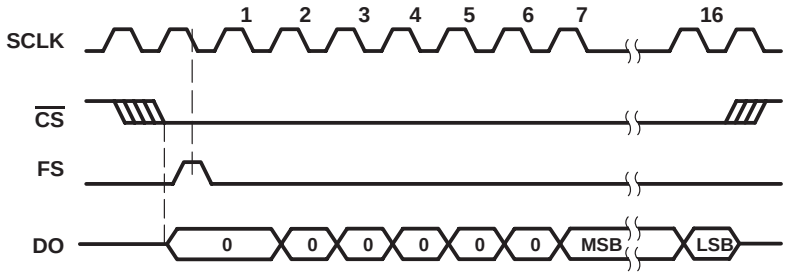


Figure 4–5. Typical Timing Diagram for DSP Application



In the DSP mode, the FS input should be low when the $\overline{CS}$ goes low. A hold time before FS input can go high after the $\overline{CS}$ falling edge ensures proper mode latching. With the $\overline{CS}$ going low, the DO comes out of 3-state but the chip is still in power down until the FS (Frame Sync signal from DSP) comes.

The TLV1572 checks for the FS at the falling edges of SCLK. Once the FS is detected high, the sampling of input is started. As soon as the FS goes low, the chip starts shifting the data out on the DO line. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by DSP on the falling edges. Figure 4–5 shows the DSP mode timing diagram.

The TLV1572 goes into auto-power down after the LSB is shifted out. The next FS pulls it out of auto-power down as shown in Figure 4–6. If the FS comes on the 16th bit, next conversion cycle starts from next rising edge of the SCLK, allowing back to back conversions as shown in Figure 4–7. An FS in the middle of a conversion cycle resets the chip and starts a new conversion cycle. Therefore, variable-bit transfer is supported if the FS appears earlier.

The $\overline{CS}$ can be pulled high asynchronously to put the chip into 3-state and power down. The $\overline{CS}$ can also be pulled low asynchronously to start checking for the state of FS on the falling edges of the clock.

Figure 4–6. DSP Application Timing (Intermittent Conversion)

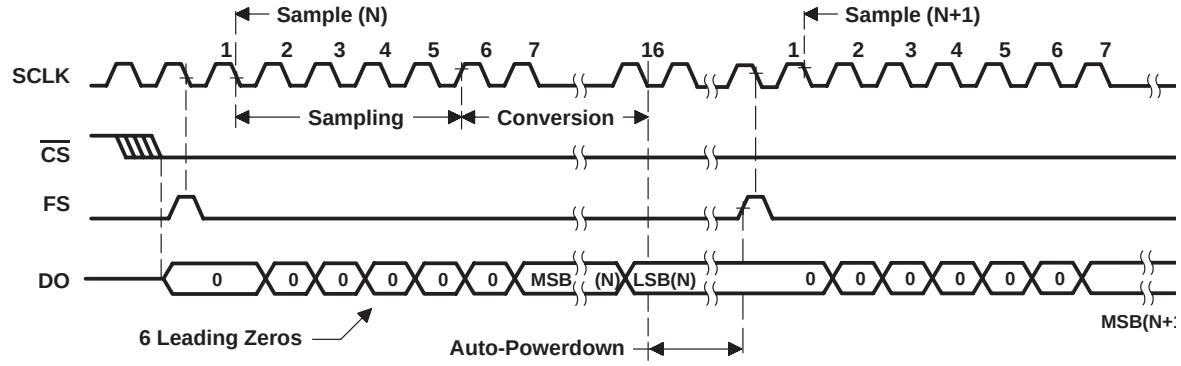
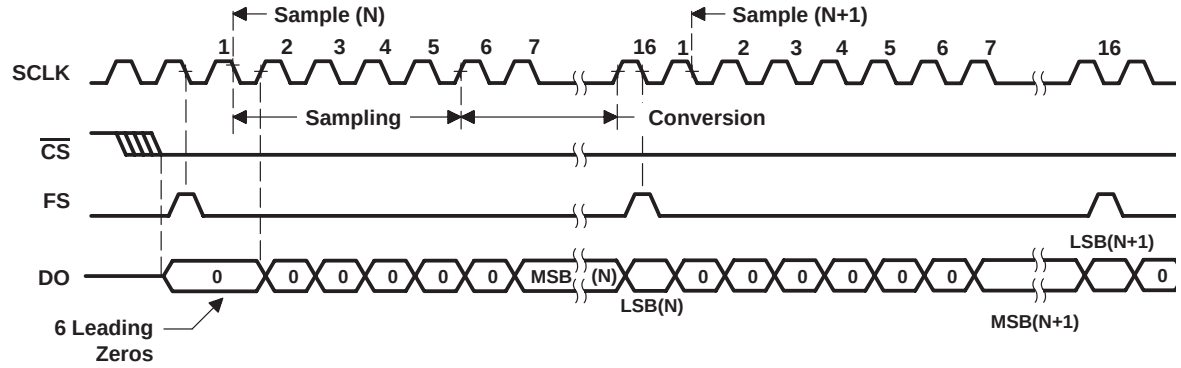


Figure 4–7. DSP Application Timing (Continuous Conversion)



4.2.1 Key Points

- When $\overline{CS}$ goes low, if FS is low, the device is in DSP mode. FS is sampled twice by $\overline{CS}$ falling edge and again by internally delayed $\overline{CS}$ falling edge. Even if a glitch appears and one latch latches 1 and another latches 0, the device goes into DSP mode (µC mode requires both latches to latch 1). A hold time before FS can go high again after the $\overline{CS}$ falling edge ensures proper mode latching as detailed above. With $\overline{CS}$ going low, DO is in 3-state and the chip is in powerdown until the FS rising edge.
- The TLV1572 checks for FS at every falling edge of SCLK. If FS is detected high, the chip goes into reset. When FS goes low, the TLV1572 waits for DSP to latch the first bit 0.
- Sampling occurs from the first falling edge of SCLK after FS going low until the rising edge when the 6th bit 0 is given out. Thereafter, decisions are taken on rising edges and data is given out on rising edges a bit delayed. The DSP samples on the falling edge of SCLK. Data is padded with 6 leading zeros.
- Note that chip goes into auto-power down on the 17th falling edge of SCLK (just after LSB). FS rising edge pulls it out of auto-power down. If FS comes on the 16th bit itself, the next conversion cycle starts from next rising edge allowing back to back conversions. An FS in the middle of a conversion cycle starts a new conversion cycle. Thus variable-bit transfer is supported if FS appears earlier.

- DO goes into 3-state on the 17th rising edge and comes out on FS rising edge.
- $\overline{CS}$ can be pulled high asynchronously to put the chip into 3-state and powerdown. $\overline{CS}$ may also be pulled low asynchronously to start checking for FS on the falling edges of clock

For applications where the analog input must be sampled at a precise instant in time, the data conversion can be initiated by an external conversion start pulse which is completely asynchronous to the SCLK as shown in Figure 4–4b. When a conversion start pulse is received, the pulse is used as a Frame Sync (FS) signal to initiate the data conversion and transfer. The corresponding timing diagram is shown in Figure 4–7.

4.3 Interfacing TLV1572 to SPI/QSPI Compatible Microcontrollers (μCs) Interface

The TLV1572 is compatible with SPI and QSPI serial interface standards. The TLV1572 supports the following SPI clock options: CLOCK_POLARITY= 0, i.e., SCLK idles low, and CLOCK_PHASE = 1. Figure 4–8 shows the pin connections to interface the TLV1572 to the SPI/QSPI compatible microcontrollers.

Figure 4–8. μC to TLV1572 Interface

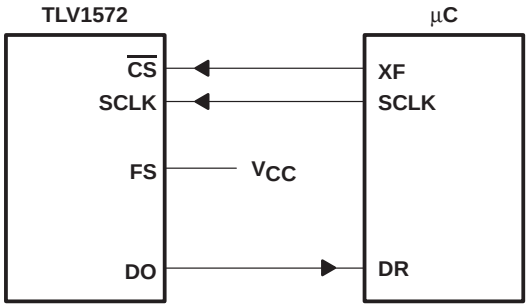
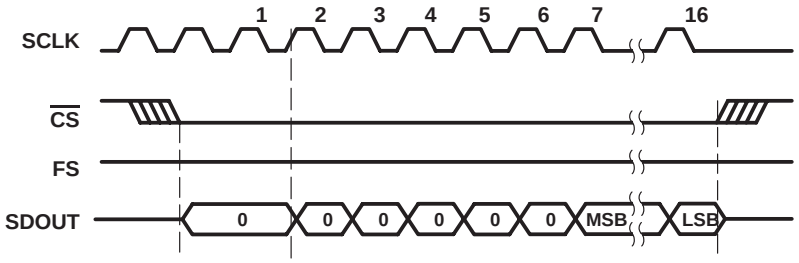


Figure 4–9. Typical Timing Diagram for μC Application



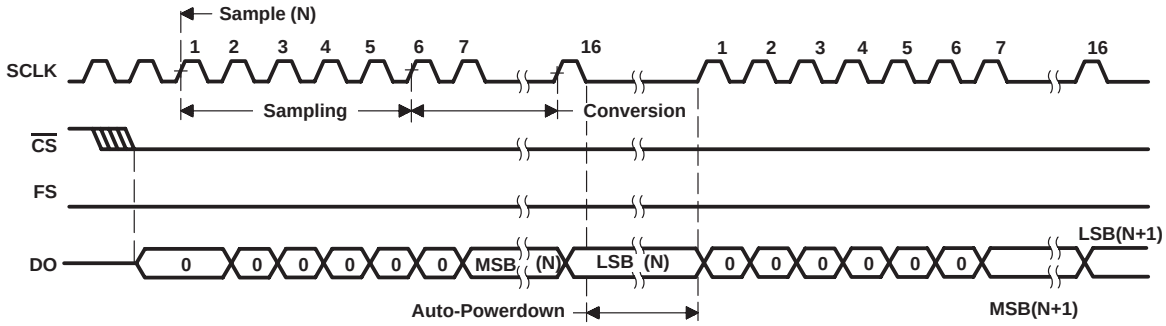
To use the TLV1572 in a non-DSP application, the FS input should be pulled high as shown in Figure 4–9.

A total of 16 clocks are normally supplied for each conversion. If μC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and the next 8 bits with another 8 clocks. The $\overline{CS}$ should be kept low throughout the conversion. The delay between these two 8-clock periods should not be longer than 100 μs.

Unlike the DSP mode, in which the conversion is initiated by the FS input signal from the DSP, the conversion is initiated by the incoming SCLK after the $\overline{CS}$ falls. The sampling of input is started on the first rising edge of the SCLK after the $\overline{CS}$ goes down. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by μC on the falling edges. The $\overline{CS}$ can be pulled high during the conversion before the LSB is shifted out to use the chip as a lower resolution ADC. Figure 4–10 shows the μC mode timing diagram.

The chip goes into auto-power down after the LSB is shifted out and is brought out of the power down by the next clock rising edge as shown in Figure 4–10.

Figure 4–10. µC Application



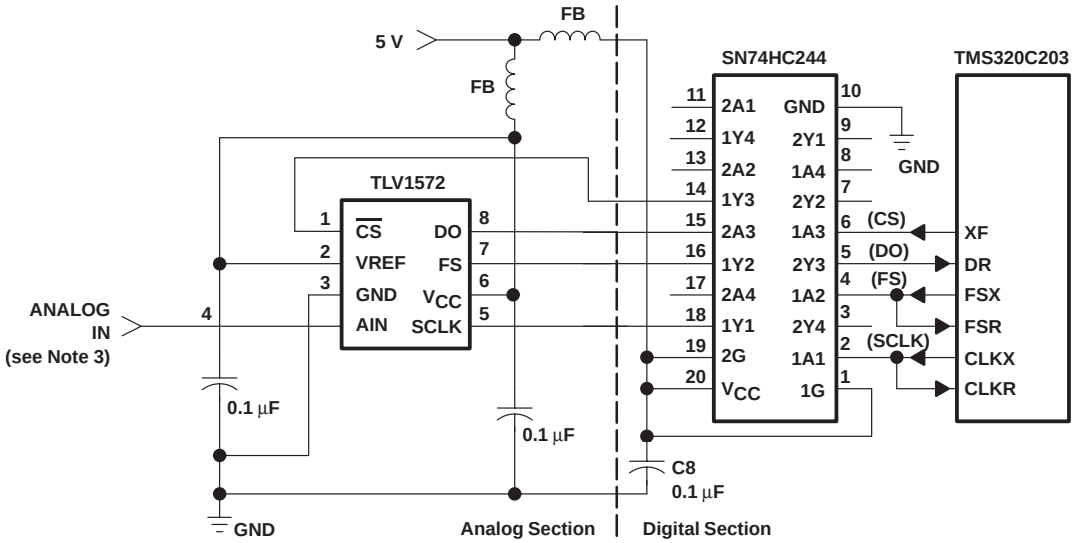
4.3.1 Key Points

- When $\overline{CS}$ goes low, if FS is high, the device is in µC ({Q}SPI) mode. Thus, FS should be tied to VDD. FS is latched twice, on the $\overline{CS}$ falling edge and again on the internally delayed $\overline{CS}$ falling edge. The µC mode is set only if both latches latch 1; otherwise, the DSP mode is set. Only polarity = 0 is supported i.e. SCLK idles low. Only clock_phase = 1 is supported, as shown in timing diagrams.
- 16 clocks have to be supplied for each conversion. If µC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and the next 8 bits with another 8 clocks, keeping $\overline{CS}$ low throughout the conversion. The delay between these two 8-clock periods should not be higher than 100 ns.
- Sampling starts on the first falling edge of SCLK and ends on the edge when 6th bit 0 is given out. Decisions are made on the rising edge and data is output on the same edge, but a bit delayed to avoid noise.
- The chip goes into auto-power down on the 16th clock's falling edge and is brought out of it by the next 1st(17th) clock's rising edge.
- If (Q)SP wants less than a 16-bit transfer, $\overline{CS}$ must go high after each transfer. The falling edge of $\overline{CS}$ will reset the TLV1572 for the next conversion. Thus the user may do a 14-bit transfer to use the chip as an 8-bit A/D.
- $\overline{CS}$ going high puts the chip in 3-state and complete power down. $\overline{CS}$ going low merely sets the mode and pulls DO out of 3-state.

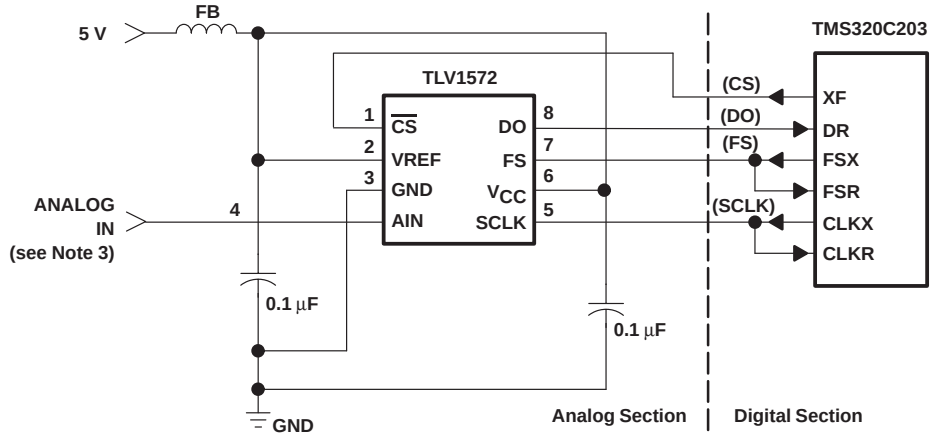
4.4 TLV1572 to TMS320C203

Figure 4–11 is the schematic diagram showing the hardware connections between the TLV1572 and the TMS320C203.

Figure 4–11. Schematic Diagram



(a) Hardware Connection with Cabling Longer than 6 Inches to the DSP



(b) Hardware Connection with Cabling Equal to or Shorter than 6 Inches to the DSP

NOTES: 1. FB is a ferrite bead, Fair-Rite™ #2744044447 or equivalent.
2. Bypass capacitors for terminals VREF and V_{CC} should be as close to the device pins as possible.
3. The analog input voltage should be band limited.

Appendix A

Grounding Considerations

This appendix contains general information on grounding techniques for a printed circuit board using the TLV1572.

Topic **Page**

A.1 Printed Circuit Board Grounding Considerations

When designing analog circuits that share a ground with digital and high current power supplies, the voltage drop along the high current paths must be considered. This voltage drop is a result of the current flowing through the greater than zero resistance of the current path, or high frequency current transients flowing through a greater than zero inductance of a current path.

If the signal ground is connected to the power supply ground at an improper location, an excessive voltage drop may occur in the signal ground and appear as part of the signal, causing an error.

The solution for low frequency analog signals is to establish a single ground point on the PC board and connect all low frequency grounds to that point. By using this method, currents flowing along any one path to ground do not produce error voltages in any other ground path.

Analyzing the current flow paths within the analog section gives an indication of which components can be lumped together to a common ground path and which should be separate. One half LSB error with a reference of 4.1 volts would be approximately 0.5 mV, so the ground trace resistance would have to be greater than 0.5 ohms with 1 mA of ground current.

When input source signals are low current, a common ground trace may be appropriate. Higher input current sources, however should always have a separate ground trace to the most robust ground point location, usually at the ground entrance to the PCB.

Even though the TLV1572 operating current is low, some high-speed current transients are present. These are usually caused by output digital switching requiring a ground plane or wide ground return trace to the central board entry ground for these signals. All signal paths and their respective ground returns must be examined to minimize signal loop area.

The power inputs and V_{CC} lines must be analyzed in the same manner and detail as the ground returns.

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