Application Note

Inter Chip Limiter Alignment in TAx5xxx-Q1 Devices

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ABSTRACT

The TAx5xxx family of audio CODECs and DACs are stereo, high-performance converters for audio applications, with the TAx5xxx-Q1 variants tailored for automotive use.

The TAx5xxx-Q1 series, exclusively TAC5xxx-Q1 and TAD5xxx-Q1, incorporate the Limiter Bank algorithm, which use the Distortion Limiter, Brown-Out Protection, and Thermal Foldback feature to adjust output based on VBAT or AVDD levels. The Limiter Bank algorithm is covered in the *Dynamic Voltage and Temperature Tracking Based Limiter in TAx5xxx-Q1,* application note.

This article explains how to configure multiple TAx5xxx and TAx5xxx-Q1 devices for synchronized output attenuation of the limiter bank.

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1 Introduction

The TAx5xxx-Q1 device incorporates a dynamic Limiter Bank algorithm designed to enhance audio performance and protect system integrity. This algorithm includes several key features:

- **Distortion Limiter**
  Prevents audio distortion by automatically adjusting the output levels during high volume peaks or drops in battery voltage.
- **Brown-Out Protection**
  Safeguards against voltage drops, making sure of consistent audio performance.
- **Thermal Foldback**
  Reduces output levels to prevent overheating and protect the device.

In automotive audio applications, these features make sure of high quality audio delivery and equipment reliability. For example, the Distortion Limiter maintains sound clarity during sudden volume changes, while Brown-Out Protection makes sure of stable operation despite fluctuations in a vehicle's electrical system. Thermal foldback prevents damage to audio components, such as speaker amplifiers driven by the device, during extended use, making sure of long term durability.

The Inter-Chip Limiter Alignment (ICLA) supports the synchronization of limiter functions across multiple devices. This process is crucial in modern vehicles equipped with multi-speaker systems, making sure of consistent output attenuation and audio quality throughout the vehicle, maintaining a balanced and high-fidelity sound experience.

2 Signal Chain Architecture

For systems with up to 8 analog input channels, 8 digital input channels, or 16 digital microphone inputs routed through the DAC signal chain, four TAx5xxx-Q1 devices can synchronize gain adjustments with the ICLA algorithm. TAx5xxx-Q1 supports a shared I^2C control bus and audio serial bus using a time-division multiplexed (TDM), Inter-IC Sound (I^2S), or Left-justified (LJ) interface. Figure 2-1 shows a diagram of four TA(C/D)5XXX devices connected for ICLA with digital inputs on a shared audio serial bus.

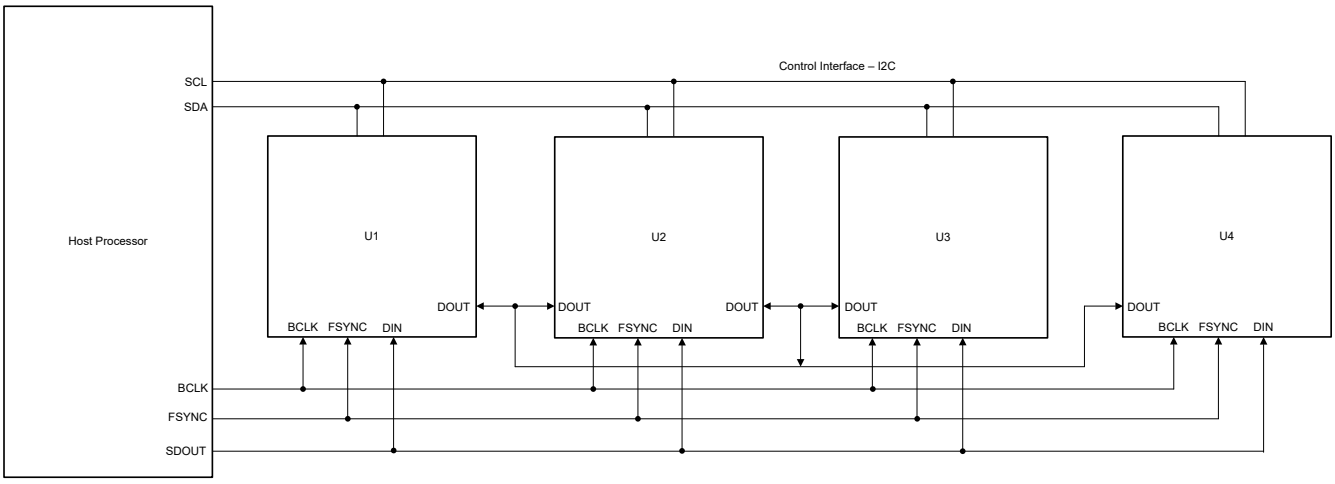

Figure 2-1. Playback Signal Path Configuration

Figure 2-2 shows a diagram of four TAC5xxx-Q1 devices connected for ICLA with 8 analog channels.

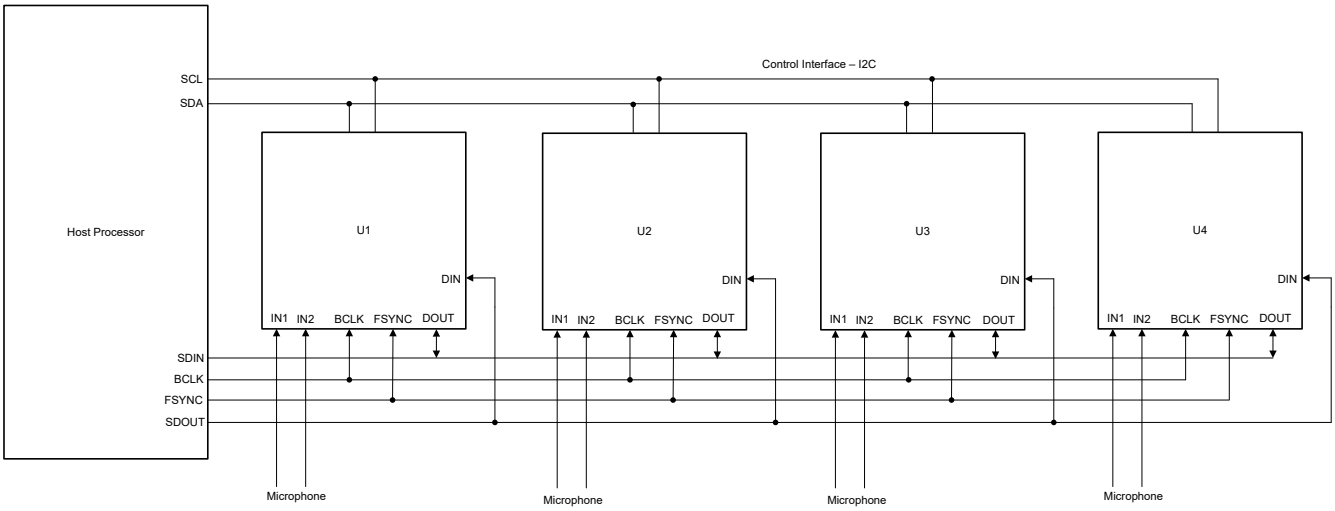

Figure 2-2. Record and Playback Signal Path Configuration

Internal ADC channel output loopback is not supported when configuring more than 2 devices for ICLA synchronization due to slot reservation for ICLA communication. Figure 2-3 shows a diagram for routing multiple devices to record and playback with a manual loopback circuit design.

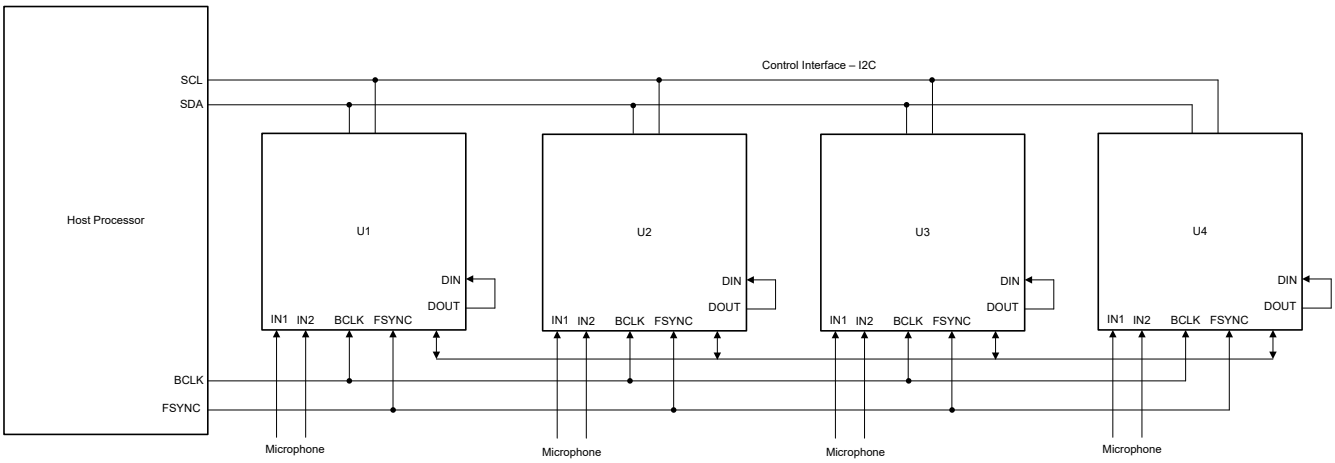

Figure 2-3. Record and Playback Path with Loopback

3 ASI Configuration for ICLA

The ASI buses of multiple TAX5XXX-Q1 devices are connected together through the digital output pin (DOUT) of each corresponding device. When ICLA is enabled, DOUT is a bidirectional transmitter and receiver for changes made within the limiter bank. The ICLA algorithm is mapped to transmit the data to other devices in the PASI_TX_CH8_CFG (P0_R37_D5) register and receive data from other devices in the PASI_RX_CH[6-8]_CFG (P0_R45-R47_D6:5) registers. The slot assignment for each channel is configured in the PASI_TX_CHx_CFG (P0_R30-R37_D4:0) and PASI_RX_CHx_CFG(P0_R40-R47_D4:0). Figure 3-1 shows an example slot configuration for four devices configured for ICLA.

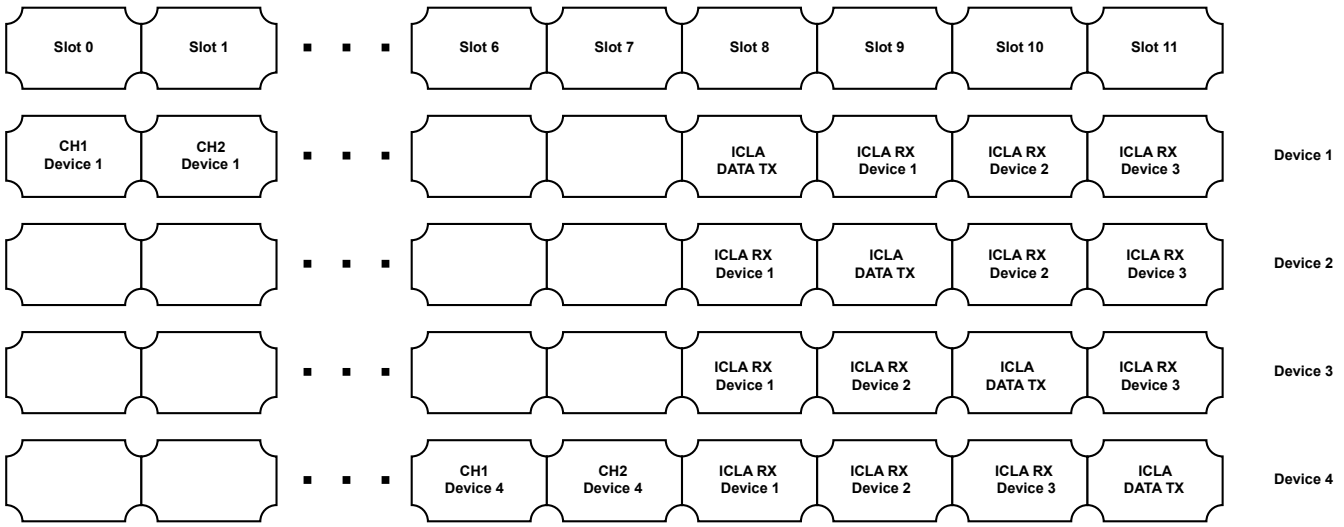

Figure 3-1. Four Device Slot Configuration for ICLA

4 Decision Tree

ICLA aligns the minimum gain applied by the limiter bank to any connected device at any time when ICLA is enabled. For example, when the Distortion Limiter Threshold Maximum on device 1 is set to -6dB and the maximum threshold is set to 0dB on device 2, ICLA aligns the DAC output level to be -6dB on both devices, even if the battery voltage has not dropped below the Inflection Point. A gain adjustment made as a result of the Distortion Limiter, Brown-Out Protector, or Thermal Foldback algorithm is aligned among all devices.

5 Application Example

In this example, there are two TAC5412Q1EVM's connected for ICLA synchronization with the distortion limiter enabled on each device. Two independent DC power generators supply VBAT_IN on each device. Figure 5-1 showcases the block diagram of the TAC5412-Q1 devices connected for ICLA functionality.

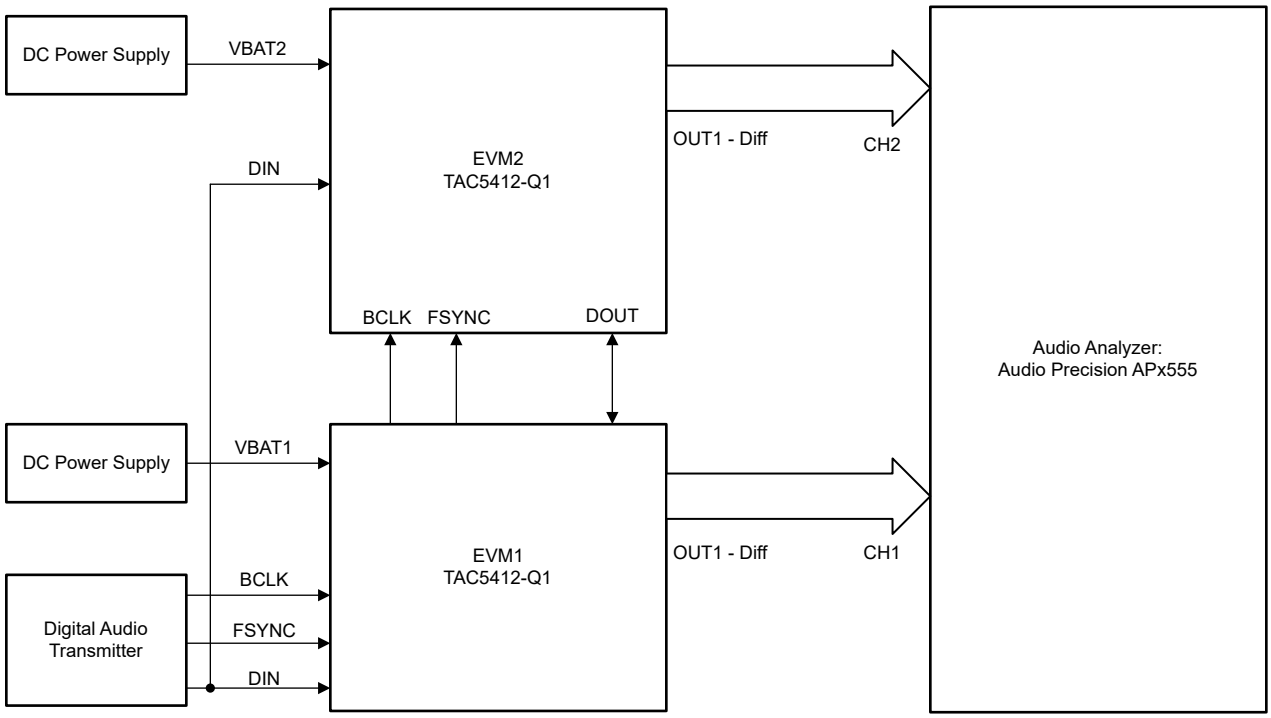

Figure 5-1. EVM Test Setup

Both TAC5412Q1EVM's have the distortion limiter enabled, EVM1 is configured to an output level maximum threshold of 0dB and EVM2 has a maximum threshold set to -5dB. The inflection point, which triggers the engagement of the distortion limiter, is configured to 9V on each device. VBAT1 and VBAT2 on each device are measured above the inflection point at 12V. Figure 5-2 shows the output level of each device with ICLA disabled and DOUT unconnected between EVM1 and EVM2.

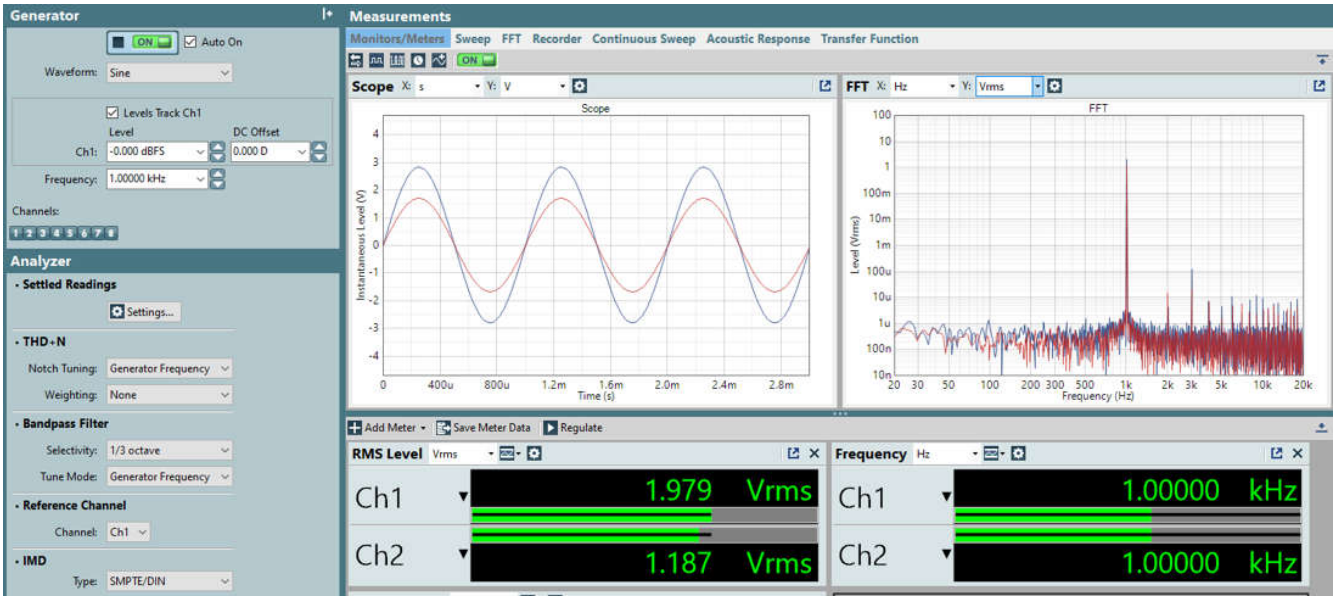

Figure 5-2. Output Waveform, ICLA Disabled, DOUT Unconnected

Figure 5-3 shows the output level of each device with DOUT connected between EVM1 and EVM2 and ICLA enabled. The limiter maximum threshold is aligned on both EVM's, as a -5dB attenuation is applied to the output signal level. VBAT1 and VBAT2 remain above the inflection point at 12V.

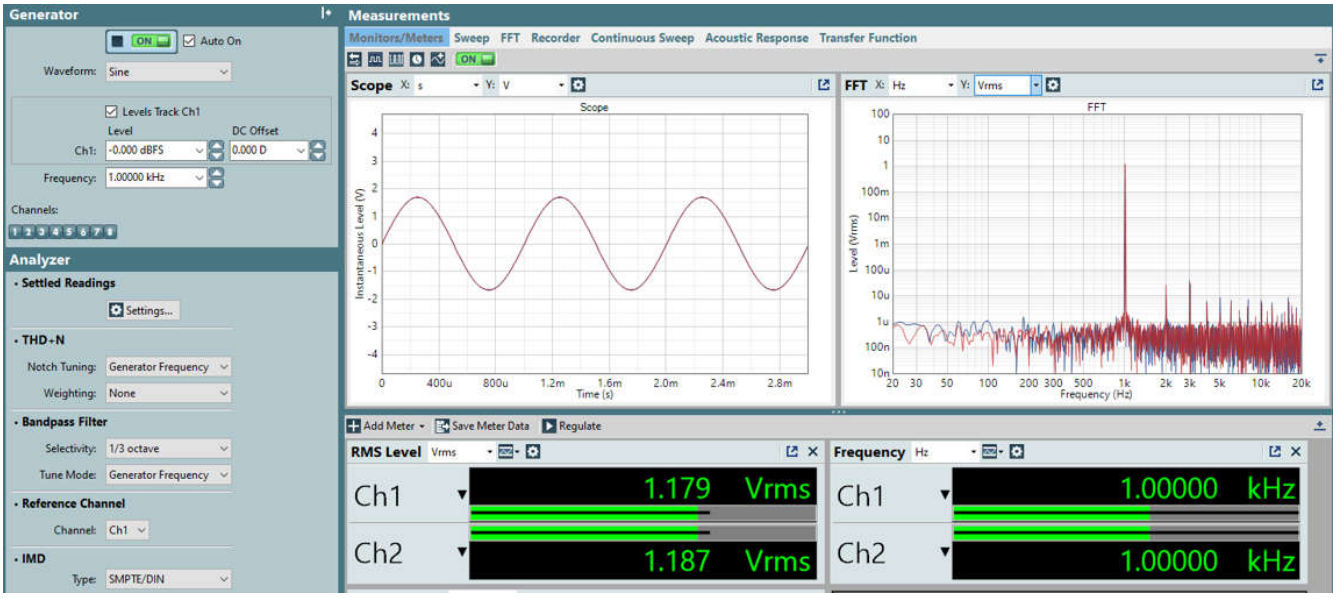

Figure 5-3. Output Waveform, ICLA Enabled, DOUT Connected

The limiter minimum threshold is set to -25dB and -50dB on EVM1 and EVM2 respectively. As VBAT1 decreases below the inflection point, the output level of both devices is attenuated to 118 mVrms, an attenuation close to -25dB, which is expected according ICLA settings.

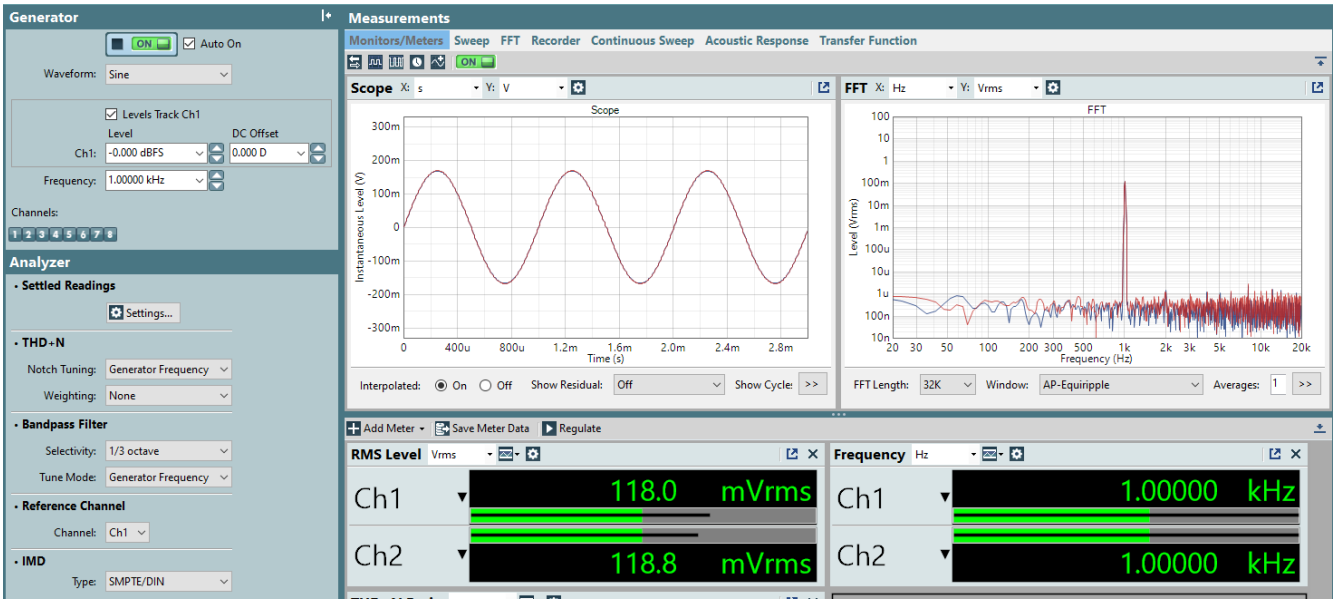

Figure 5-4. Output Waveform, -25dB Attenuation

Shown in Figure 5-5, as VBAT2 decreases below the inflection point to 8V, the output attenuates to approximately 6.6 mVrms, an attenuation close to-50dB, which is expected according to ICLA settings.

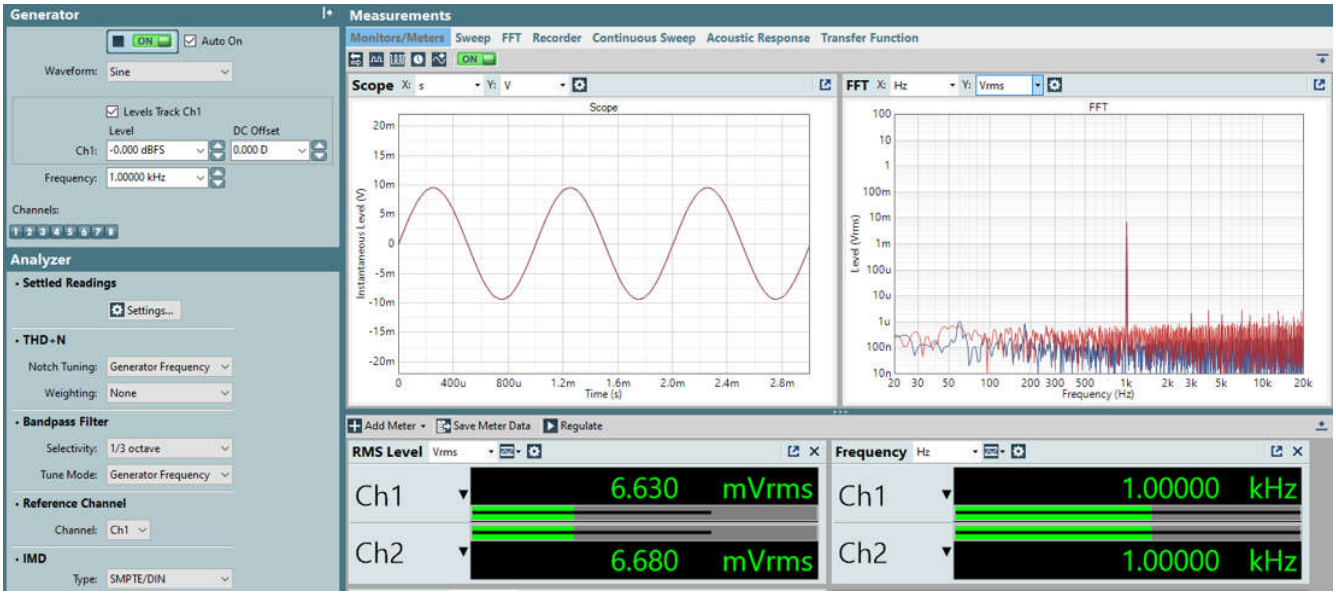

Figure 5-5. Output Waveform, -50dB Attenuation

As shown in the waveforms, the output channels of the DAC can have a difference measured less than 0.1dB with respect to full-scale when connected for ICLA synchronization.

5.1 Application Example Script

Table 5-1 is an example script for TAx5xxx-Q1 devices under the parameters outlined in the application example section.

Table 5-1. Example Script for TAx5xxx-Q1

EVM 1 Parameters	EVM 2 Parameters
Distortion Limiter enabled	Distortion Limiter enabled
Inflection point: 9V	Inflection point: 9V
Threshold Max: 0dB	Threshold Max: -5 dB
Slope: 1V/V	Slope: 2V/V
ICLA TX: Slot 5	ICLA TX: Slot 4
ICLA RX: Slot 4	ICLA RX: Slot 5

EVM 1 example script:

```
# Key: w a0 XX YY ==> write to I2C address 0xa0, to register 0xXX, data 0xYY
# # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Line-Out Fully-Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 12.288 MHz (BCLK/FSYNC = 256)
#####################################################################
Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.#
Release SHDNZ to HIGH.
# Wait for 1ms
#
w a0 00 00  #Go to page 0
w a0 01 01  # Software reset
w a0 02 09  # Come out of sleep mode, enable DREG, VREF
################
w a0 06 50  # Set HP cap charging time to 2ms
w a0 72 1a  # Enable ADC soft stepping
w a0 73 1a  # Enable DAC soft stepping
w a0 00 00  # Go to page 0
w a0 1b 48  # Enable bus keeper and HI-Z output
w a0 28 20  # CH1 data in slot 0
w a0 29 21  # Ch2 data in slot 1
w a0 25 25  # ICLA TX data on slot 5
w a0 2d 64  # ICLA RX Data on slot 4
#################
w a0 00 01           # Go to page 1
w a0 2d 80           # Enable distortion limiter
w a0 53 90           # VBAT Ch enable for diagnostics
w a0 00 19           # Go to page 25
w a0 60 78 d6 fc 9f  # Attack rate
w a0 74 00 00 48 00  # 9V inflection point
w a0 6c 01 69 9c 0f  # 0 dB Limiter Thr Max
w a0 64 40 bd b7 c0  # Release rate
w a0 70 00 14 55 b6  # -25dB Limiter Thr Min
w a0 78 10 00 00 00  # Slope 1 V/V
###############
w a0 00 00  # Go to page 0
w a0 76 cf  # DAC CHs enabled
w a0 78 c0  # ADC & DAC powerup
```

EVM2 example script:

```
# Key: w a1 XX YY ==> write to I2C address 0xa1, to register 0xXX, data 0xYY
# # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Line-Out Fully-Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 12.288 MHz (BCLK/FSYNC = 256)
######################################################################
Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.#
Release SHDNZ to HIGH.
# Wait for 1ms
#
w a1 00 00  #Go to page 0
w a1 01 01  # Software reset
w a1 02 09  # Come out of sleep mode, enable DREG, VREF
###############
w a1 06 50  # Set HP cap charging time to 2ms
w a1 72 1a  # Enable ADC soft stepping
w a1 73 1a  # Enable DAC soft stepping
w a1 00 00  # Go to page 0
w a1 1b 48  # Enable bus keeper and HI-Z output
w a1 28 22  # CH1 data in slot 2
w a1 29 23  # CH2 data in slot 3
w a1 25 24  # ICLA TX data on slot 4
w a1 2d 65  # ICLA RX Data on slot 5
################
w a1 00 01           # Go to page 1
w a1 2d 80           # Enable distortion limiter
w a1 53 90           # VBAT Ch enable for diagnostics
w a1 00 19           # Go to page 25
w a1 60 78 d6 fc 9f  # Attack rate
w a1 74 00 00 48 00  # 9V inflection point
w a1 6c 00 cb 59 18  # -5dB Limiter Thr Max
w a1 64 40 bd b7 c0  # Release rate
w a1 70 00 01 24 bd  # -50dB Limiter Thr Min
w a1 78 20 00 00 00  # Slope 2 V/V
##############
w a1 00 00  # Go to page 0
w a1 76 cf  # DAC CHs enabled
w a1 78 c0  # ADC & DAC powerup
```

6 Summary

Texas Instruments has integrated three features into the TAx5xxx family of devices for audio processing in battery powered applications – Distortion Limiter, Brown-Out Protection, and Thermal Foldback. ICLA allows the synchronization of the three features across multiple devices while maintaining audio performance. Together, these features exemplify a comprehensive approach to balancing audio excellence and power efficiency in battery powered applications.

7 References

- Texas Instruments, *Dynamic Voltage and Temperature Tracking Based Limiter in TAx5xxx-Q1,* application note.

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