TEXAS INSTRUMENTS

Application Report
SLAA902–January 2020

PCB Layout Guidelines for TAS2xxx Series Class-D Non-boosted Audio Amplifier

ABSTRACT

As the performance of class-D audio amplifiers gets better and system complexity increases, special care must be taken in the printed circuit board (PCB) layout phase of a design to ensure a robust solution. As in most engineering practices, there is no unique solution to a given problem. There is no unique layout, but this application note can help guide you to reach an optimal layout solution.

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1 Introduction

1.1 Scope

This application note can help system designers implement best practices and understand PCB layout options while designing the audio segment of the system. It serves as a guide to laying out critical nets reliably. This helps in extracting the best possible audio quality from the class-D audio amplifier. This is intended for the audiences who are involved in designing audio systems.

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1.2 Critical Signals

The main concern while designing audio systems is choosing the right passive component which maintains quality of the audio, along with small system size and less cost. Another big concern that arises due to the System-on-Chip (SoC) IC is routing analog, digital, and power signals with integrity, avoiding interference with each other and maintaining audio quality. The third concern while routing signals is that other system devices must not negatively interfere with the audio chip and vice versa due to EMI and other voltage and current switching.

Table 1. Critical Signals and Description

SIGNAL NAME	DESCRIPTION
DREG	Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load.
GND	Digital ground. Connect to the PCB GDN plane.
OUT_N	Class-D negative output for the receiver channel.
OUT_P	Class-D positive output for the receiver channel.
PGND	Power stage ground. Connect to the PCB GND plane.
PVDD	Power stage supply. Decouple with the capacitor.
VBAT/VBAT1S	Battery power supply input. Decouple with the capacitor.
VDD	Analog, digital, and IO power supply. Decouple with the capacitor.
VSNS_N	Voltage sense negative input
VSNS_P	Voltage sense positive input
ADDR/MODE	Address detect pin
AVDD	Analog and digital power supply. Decouple with the capacitor.
IOVDD	IO supply. Decouple with the capacitor.
BST_N	Class-D negative bootstrap. Connect a capacitor between BST_N and OUT_N.
BST_P	Class-D positive bootstrap. Connect a capacitor between BST_P and OUT_P.

2 Layout Guidelines

After selecting the right set of components, the next important task is to lay out the PCB in such a way that the device gives optimum performance for the particular system. See the *Passive Component Selection Guide for Class-D Audio Amplifier Application Report* for a selection guide to choose the right set of passive components for an audio amplifier. Four to six layers of epoxy-filled vias should be ideal for the optimum layout of the device.

AVDD/VDD and IOVDD must be routed from the PMIC/source as star-connected thick traces (20 mils–30 mils) at the source for several ICs in the system.

Bypass capacitors serve two main purposes. It fulfills the sudden switching current requirement for the device and helps in decoupling voltage noise fluctuations on power pins, ensuring a reliable constant solid power supply seen by the device pin, thus better performance. In order to reduce parasitic inductance and resistance of the routing, the decoupling capacitors must be placed right next to the corresponding pin on top layer itself and route with as thick of trace as possible. For internal pins where the connection to decoupling capacitor is not possible on the top layer, try to route it in the immediate layer to top layer in order to reduce parasitic.

2.1 Power Planes

Power planes should be routed thick enough to carry the maximum current supply the pin demands. Take special care when the supply plane is shared among multiple ICs in the system. The best layout practice is providing the planes/thick traces to different ICs in the system from the power management IC or main supply source in a star-connected way at the source itself. This reduces the adverse effect caused on other ICs because of the high switching ICs shared on the same line.

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2.2 Ground Plane/Connections

All the ground pins of the devices are expected to be connected to the ground plane as strongly as possible. All the device grounds are expected to be shorted in such a way that no multiple ground loops form. A direct via on the device pads to ground plane is preferable. The point to consider here is all the ground pins should be connected to plane strongly because the logical current return path for different supplies is served by different ground pins (for example, VDD-GND, DREG-GND, PVDD-PGND, and so forth). A dedicated layer for the ground is strongly recommended. Figure 1 and Figure 2 show an example of the TAS2770 device where all the ground pins are shorted on the top layer just below the device balls and then stitched to the ground layer present on layer 2 through multiple vias on the device balls and as close to device balls as possible.

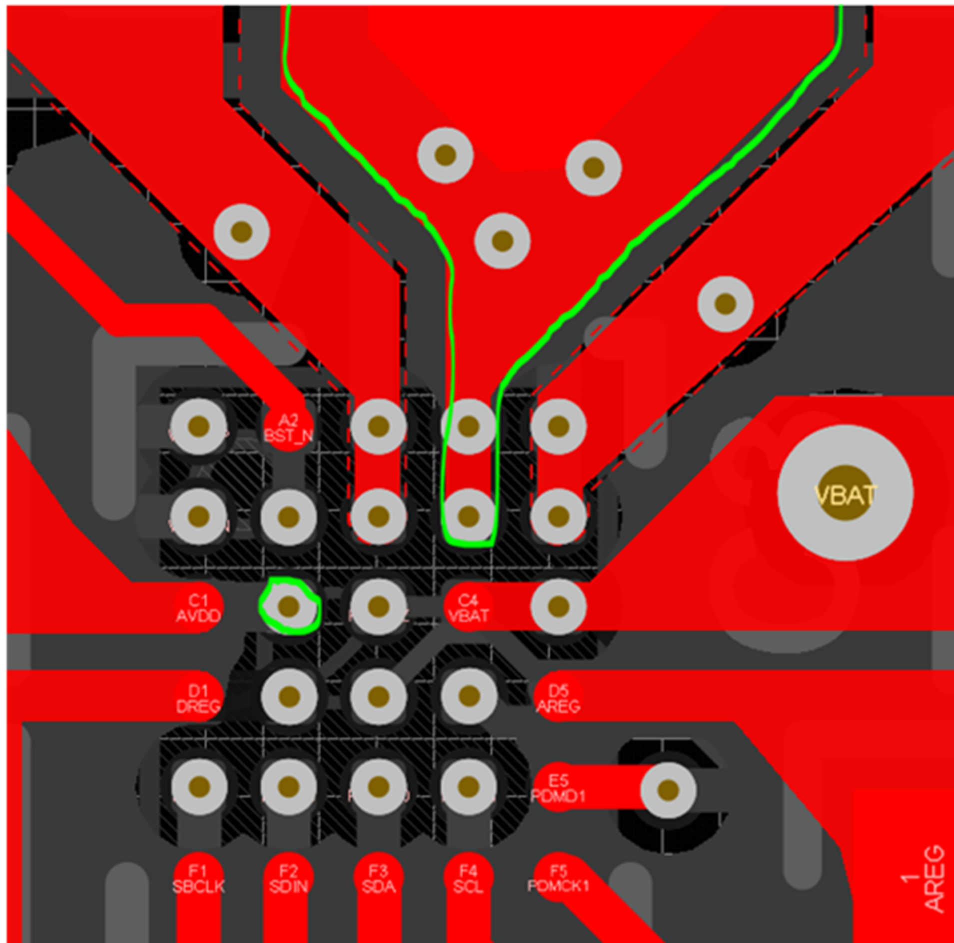

Figure 1. Top Layer for the TAS2770 PCB Shows All GND Pins are Shorted to the GND Plane

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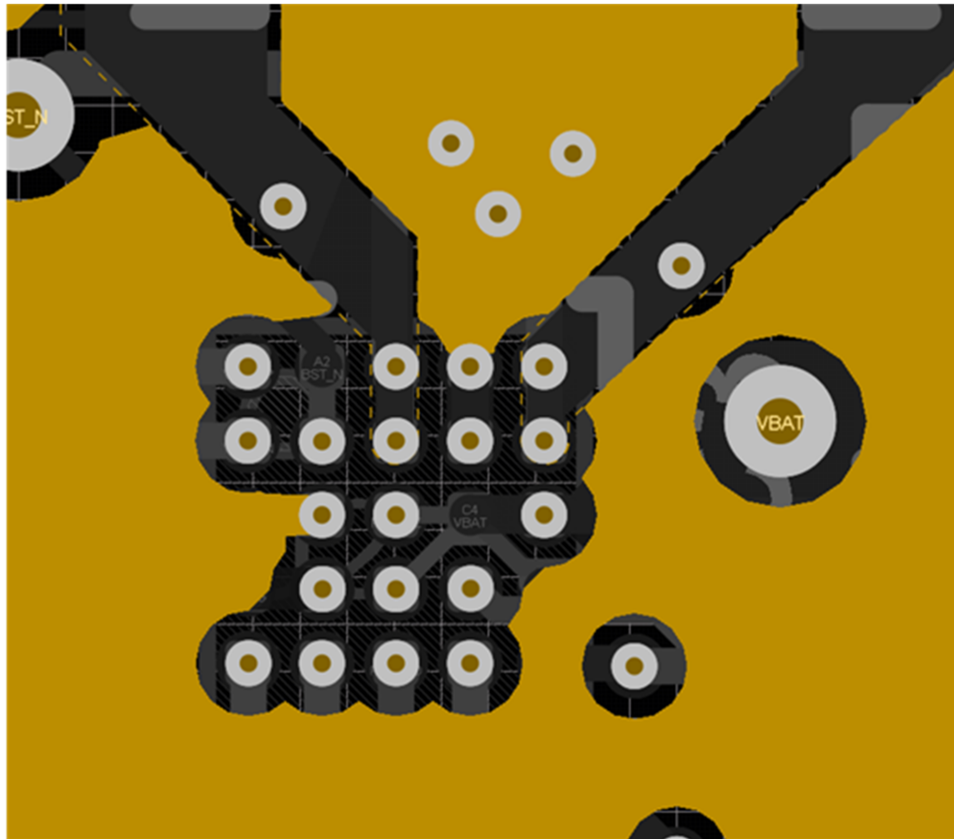

Figure 2. Layer 2 is Solid Ground Just Below the Device Area to Provide the Shortest Return Current Path

2.3 Capacitor Placement

Decoupling capacitors should be placed as close to the specific pin on the top layer as possible in order to avoid parasitic resistance and inductance. Higher resistance and inductance can lead to overshoot/undershoot in the voltage spike due to switching current requirements per Equation 1.

$$V = -L\frac{di}{dt} \quad (1)$$

The small finite time duration equation can be approximated to Equation 2.

$$V = -L\frac{\Delta i}{\Delta t} \quad (2)$$

The voltage spikes due to the switching current requirement from the power supplies. Due to the sudden current requirement, even nH of the inductance can cause large voltage ripple and hinder the device operation. Another reason for keeping the parasitic inductance and resistance minimal is to provide the decoupling path with the least impedance.

The expectation from the system design is that the smallest decoupling cap is placed less than 1 mm of the distance from the device pin and any further caps are placed next to it as close as possible.

Parasitic matters for the complete decoupling loop, which include parasitic from the power supply, pin to one end of the decoupling capacitor, parasitic of the capacitor component, and between the second end of capacitor to the ground pin of device. Using multiple vias to connect the capacitor to ground helps reduce parasitic inductance. Because of multiple parallel via connections, vias must be placed as close to the capacitor pad as possible. Table 2 shows the total acceptable loop inductance on different supply pins for optimum device performance for the TAS2770. Table 2 also shows the requirement for the bootstrap capacitor.

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Table 2. Optimum Parasitic on the Device Pin

PIN-PIN	PARASITIC INDUCTANCE (pH)	CAPACITOR ESL (pH)	TOTAL (pH)
DREG-GND	550	500	1050
BST-OUT	1000	400	1400
VBAT-GND	300	700	1000
PVDD-PGND	200	700	900
VDD-GND	400	500	900

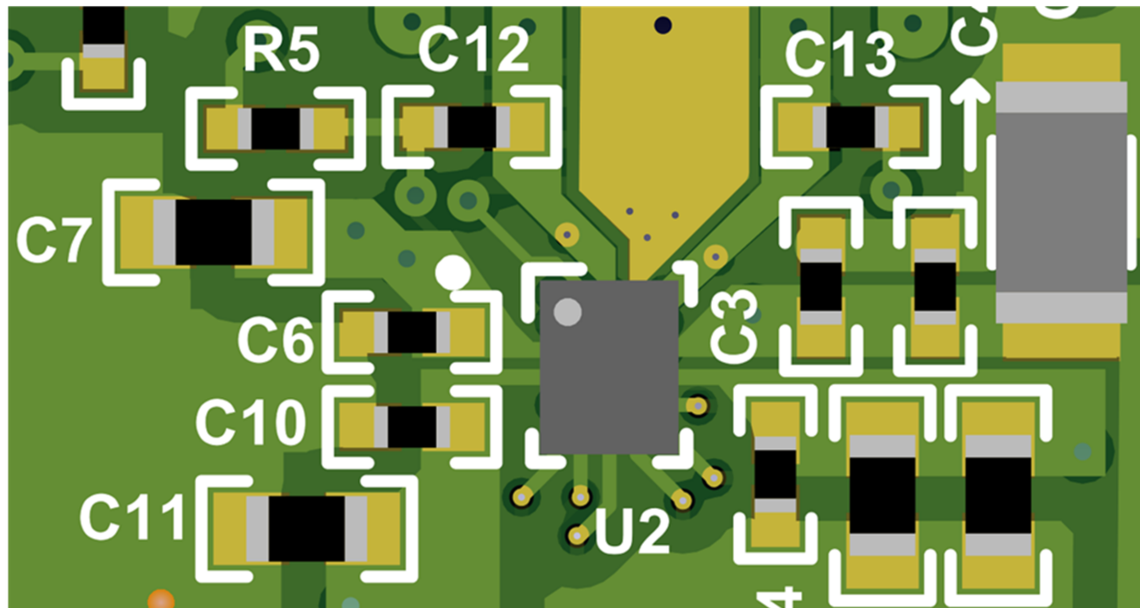

Figure 3. Capacitor Placement for the TAS2770 Device as Close to the Device as Possible

2.4 *Switching Signals*

Class-D output, Vsense signals, and Bootstrap node are continuously switching signals and should be routed in such a way that they should not couple with each other or any other signal on the PCB and interfere with them. They must not be routed in the adjacent layer with any other signal without ground shielding in between layers.

Figure 4, Figure 5, and Figure 6 illustrate the carebout for routing a switching net. Figure 4 shows top level view of the PCB and demonstrates the nets on the different layers. The basic principle here is to avoid coupling between different switching net and between switching net and any other signal. Figure 4 and Figure 5 show valid routing conditions while Figure 6 shows an invalid scenario.

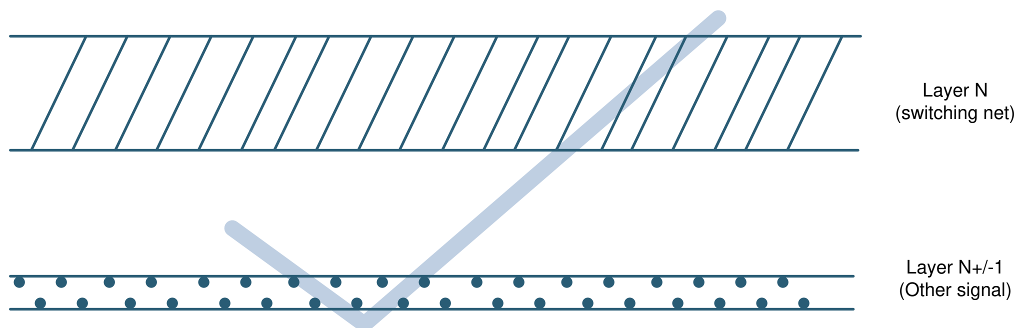

Figure 4. PCB Top View Shows Routing Switching Net Without Providing a Cross Sectional Area for Coupling with Other Net in an Adjacent Layer

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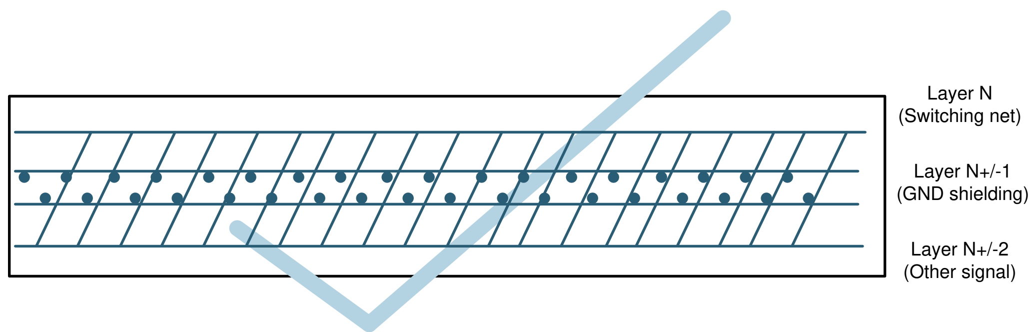

Figure 5. PCB Top View Shows the Decoupling of Switching Net with Other Net by Having a Ground Layer Between the Two

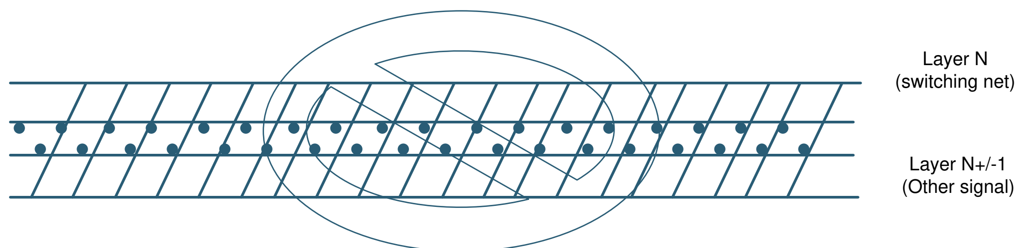

Figure 6. PCB Top View Shows Switching Net Routed Parallel to Other Signal in Adjacent Layer Without Any Ground Shielding Between the Two

2.5 Vsense Signals

Vsense signals should be routed as close to speaker terminals as possible. Vsense is used to sense actual voltage across speaker terminals and used for speaker protection. A speaker protection algorithm works optimally if the Vsense is closed closest to the speaker terminals. A 6-mil trace width is sufficient for these signals and preferably should be routed differentially to avoid any non-differential noise coupling to these signals.

2.6 Bootstrap Capacitor

A bootstrap capacitor must be connected between the BST_P pin with respect to the OUT_P pin and the BST_N pin with respect to OUT_N pin with the least possible parasitic inductance and resistance. See Table 2 for quantitative details. Note that the bootstrap capacitor should be connected as close as possible to the OUT pin as a star connection and not somewhere away from the device pin on the thick output routing. Use thick routing and immediate to the top layer to route this signal to offer minimum parasitic on this pin.

2.7 Class-D Output Signals

Class-D output signals must be routed at least 30 mil wide in two layers. Effectively each output should be routed 60 mil wide to the speaker for EM requirements. In case the EMI filter is placed on the board, it must be placed as close to the device pins as possible. For best THDN performance, output signals should be length matched to each other to avoid any mismatch degraded THDN due to a difference in routing resistance.

2.8 Digital Signals

Digital signals should be routed in a way so they do not interfere with other signals and their integrity is maintained. Make sure they are not routed adjacent to any switching net which can couple and inject noise in digital signals.

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3 Typical Board Parasitic

For a quick estimation of the parasitic while layout, Table 3 and Table 4 can be quite helpful.

Tables in this section consider the most common fabrication practice of the FR-4 STD material, 1-oz of copper, 62 mil PCB thickness, and epoxy-filled via.

Table 3. Resistance and Current Carrying Capability of Output Trace

WIDTH	DC RESISTANCE (mΩ/INCH)	CURRENT CARRYING CAPABILITY (A)
30	9.68	3.18
40	7.08	3.63
50	5.58	4.32
80	3.41	5.55

Table 4. Resistance, Inductance, and Current Carrying Capability of Typical Epoxy-filled Via(1)

VIA DIAMETER (mils)	DC RESISTANCE (mΩ)	INDUCTANCE (nH)	CURRENT CARRYING CAPABILITY (A)
4	2.9	1.61	1.4
6	2.1	1.48	1.53
10	1.3	1.32	2.01
12	1.1	1.26	2.21
18	0.7	1.14	2.72

(1) Via properties mentioned in table is for the complete 62-mil via. In case signals are routed in internal layer, these numbers can be linearly scaled. For example, a 4-mil via offers 0.8-nH inductance between the top layer and a layer 32 mil below the top layer.

4 Summary

This article concludes the optimum layout for a class-D non-boosted audio amplifier. The following table is a checklist that can be used as a quick reference while you are in the layout stage.

PIN	
GND, PGND, and GNDD	Short GND, GNDD, and PGND below the package and connect them to the PCB ground plane strongly through multiple vias. Minimize inductance as much as possible.
DREG	Bypass to GND with a capacitor that is recommended in the previous section. Do not connect to the external load. Both ends of the decoupling cap see as low inductance as possible between this pin and GND pins.
BST_P,BST_N	Connect it to OUT_P and OUT_N respectively with a star connection as recommended in the previous section. Do not connect to the external load. It does not couple with any other net in the system.
PVDD	Short it to a designated supply plane through a strong connection. Bypass to the GND with a capacitor.
VBAT	Short it to a designated supply plane through a strong connection. Bypass to the GND with a capacitor.
VDD	Bypass to the GND with a recommended capacitor. Both ends of the decoupling cap see as low inductance as possible between this pin and the GND pin.
OUT_P and OUT_N	They do not couple with any other net in the system. If required, connect an EMI filter as close to the device pin as possible. Traces do support currents up to the device overcurrent limit.

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5 References

- Texas Instruments, *TAS2562 6.1-W Boosted Class-D Audio Amplifier with IV Sense Datasheet* (SLASE17)
- Texas Instruments, *Layout Guidelines for TPA300x Series Parts Application Report* (SLOA103)
- Texas Instruments, *Post Filter Feedback Class-D Amplifier Benefits and Design Considerations Application Report* (SLOA260)
- *Singing Capacitors (Piezoelectric Effect)*
- *Saturn PCB Tool*

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