Application Report
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AFE74xx as a single-chip wideband repeater using loopback mode

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ABSTRACT

This application report evaluates the performance of the AFE7422 and AFE7444 (AFE74xx) devices as an RF sampling wideband repeater capable of operating with a frequency bandwidth as low as 130 MHz.

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1 Introduction

5G networks demand RF repeaters that can support very large signal bandwidth. The AFE7422 and AFE7444 (AFE74xx) include dual- and quad-channel, 14-bit, RF-sampling analog front ends (AFEs) that integrate four digital-to-analog converters (DAC) and four analog-to-digital converters (ADC) capable of sampling up to 9 GHz and 3 GHz, respectively.

Features include:

- No requirement of FPGA or ASIC
- No requirement of JESD link establishment
- No need for physical SerDes receiver and SerDes transmitter lanes
- Single-chip operation
- Wide-RF instantaneous bandwidth supporting 130 MHz to 1.2 GHz
- RX to TX loopback latency = 1.2 µs

2 Repeater Mode (RX-TX Loopback With SerDes Bypassed)

2.1 Overview of the AFE74xx Repeater Mode

The AFE74xx support the internal loopback of the 20-bit digital stream from the receiver to the transmitter with the SerDes bypassed. This feature can be used in applications such as repeaters, where the digital output of the RX must be fed back to the input of TX. With this loopback feature, users do not have to physically connect the STX lanes to SRX lanes on their board (through FPGA or ASIC), and gives the following advantages:

- No requirement to establish a link between the AFE and FPGA because the loopback is established within the device
- Saves cost and board space because FPGA or ASIC is not required (if no baseband processing is required on the platform)
- No need for external loopback between SRX and STX lanes; loopback is handled internally

2.2 Configuration of the AFE74xx as a Repeater

The loopback feature emulates physically connecting the STX lanes to SRX lanes. To make sure the correct JESD decoding and coding is used, both receiver paths and transmitter paths within the device must be configured to the same JESD mode (that is, the same values for L, M, F, S, and K). The scrambler must either be enabled for both or disabled for both. Then program the SPI to switch to loopback mode. SYSREF is free running until this programming is done. Figure 1 shows a block diagram of the AFE74xx in repeater mode.

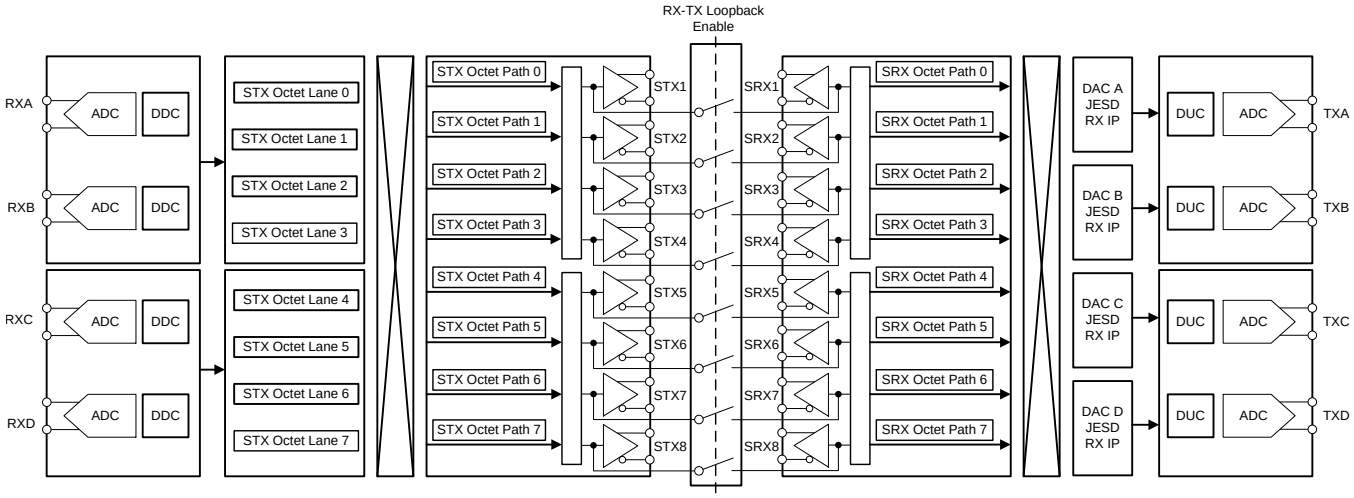

Figure 1. Repeater Mode (RX-TX Loopback With SerDes Bypassed)

Data from the STX1 lane are looped back to the SRX1 lane, and then data from STX2 to SRX2, and so on. Lane mux of receiver path and transmitter path must be set to send the data from the STX lanes to the SRX lanes in the intended way.

The sync out from the JESD RX can be looped back to sync in of the JESD TX. To achieve this loopback, externally connect the LVDS sync out pin to the LVDS sync in pin. However, because there is no JESD physical layer involved, the loss of SYNC is not expected. Therefore, the JESD TX can be configured to ignore the SYNC request from sync in pin and send RX out data after SYNC is initially established.

The following summary lists the must-do items in order to use this repeater mode through the loopback with SerDes bypassed:

- L, M, F, S, and K for both ADC and DAC must be same
- Correct configuration of lane mux on both the RX and TX
- Sync looped back externally

2.3 Programming the Repeater Mode

2.3.1 Hardware Setup

The AFE74xxEVM user's guide shows the hardware setup. Remember that in loopback mode, a capture card is not needed. Therefore, ignore any content in the user guide referring to HSDC pro or the TSW14J57.

2.3.2 Software Setup and GUI Configuration

Programming the AFE74xx EVM in repeater mode is simple. After the AFE74xxEVM is programmed normally in a desired mode, a configuration file containing a specific sequence of register writes required to enable repeater mode must then be loaded to the device through the *Low Level View* tab in the AFE74xx GUI. The mode used to program the AFE74xx must have the same LMFSK values for both RX and TX. Table 1 shows the sequence of register writes that must be loaded to the AFE74xx EVM in order to enable repeater mode (RX-TX loopback mode).

NOTE: The configuration file containing the following register writes is provided in the AFE7444 product folder. Save the file titled *loopback_mode_enable.cfg*.

Table 1. Register Sequence for Repeater Mode (RX-TX Loopback)

Process (W for Write)	Address (Hex)	Register Value (Hex)	Comment
W	0x10	0x55	Open txducp0 page for all TX
W	0x7E	0x1F	Set RBD register (0x7E) to hex value of 64 / F – 1. For example: LMFSHd = 44210, F= 2, RBD value is 64 / 2 – 1 = 31. Hex value for 31 = 0x1F. Therefore, register 0x7E is programmed to 0x1F.
W	0x10	0x00	Close txducp0 page for all TX
W	0x11	0x8	Select TRAFFICCNTL page
W	0xC5	0x5	RX-TX loop-back enabled for both 2T2R_TOPs
W	0xCF	0x1	Loopback FIFO init_state set
W	0x11	0x0	Close TRAFFICCNTL page
W	0x17	0x0	Select SerDes_JESD_TX page
W	0x45	0xC0	RX init_state clear
W	0x45	0x80	FB init_state clear
W	0x45	0x0	FIFO inti_state clear
W	0x26	0x0	RX jesd_clear_data clear
W	0x17	0x0	Close SerDes_JESD_TX page
W	0x11	0x3	Select TXDIG_P0 page
W	0x20	0x0	TX init_state clear for both TX_TOPs
W	0x11	0x0	Close TXDIG_P0 page
W	0x11	0x8	Select TRAFFICCNTL page
W	0x1A0	0xFC	Gate SYSREF
W	0x11	0x0	Close TRAFFICCNTL page
If sync out is not looped back to sync in, use the following SPI programming to establish SYNC			
W	0x17	0xC	Select SerDes_JESD_TX page
W	0x72	0xFF	Override STX output with K28.5
Delay 100 ms			
W	0x72	0xF0	Override STX output with K28.5
W	0x17	0x0	Close SerDes_JESD_TX page

The following steps show how to bring up the AFE74xx EVM and then enable repeater mode. In this example, the AFE74xx is programmed in mode 4 and then a config file enabling repeater is loaded in the *Low Level View* tab. For more details on how to bring up the AFE74xx EVM, reference the AFE74xxEVM user's guide. After the AFE74xx is powered up, launch the AFE74xx GUI, and then reference the following steps:

1. Click the *EVM Selection* button, and verify that the proper EVM is selected, as shown in Figure 2.

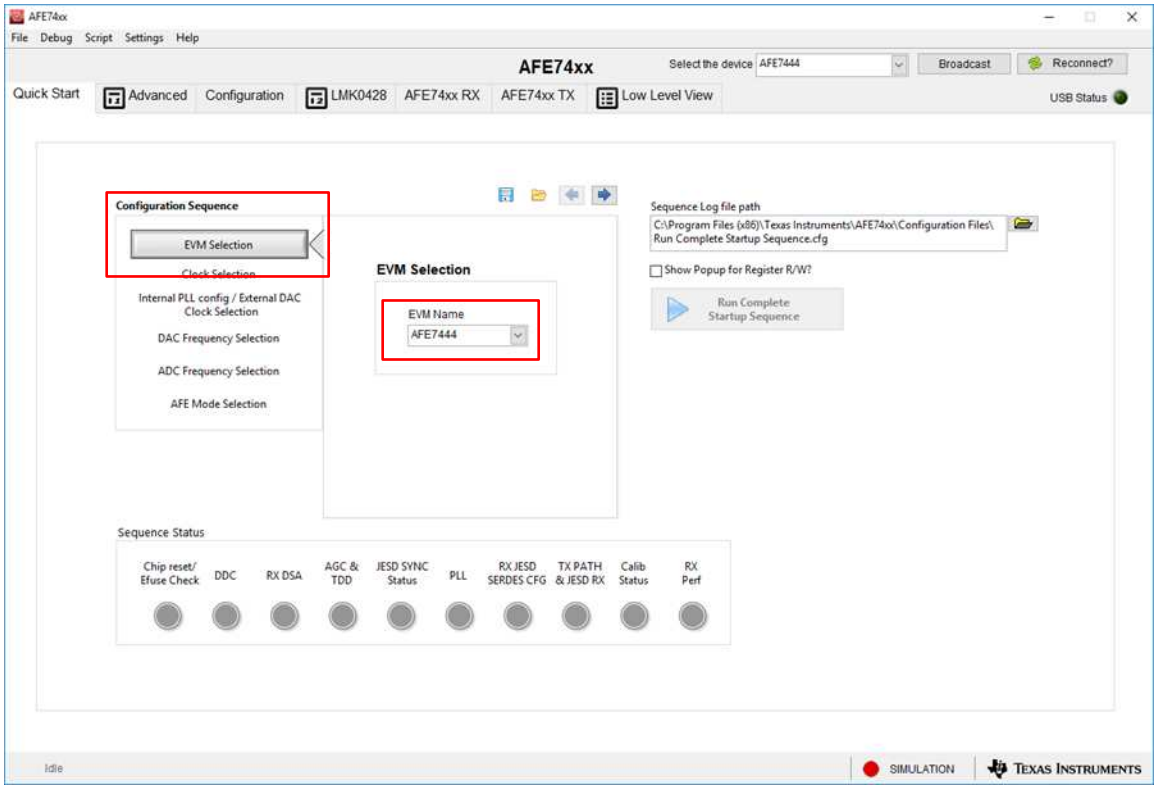

Figure 2. EVM Selection

2. Click the *Clock Selection* button, and select *Internal PLL*, as shown in Figure 3.

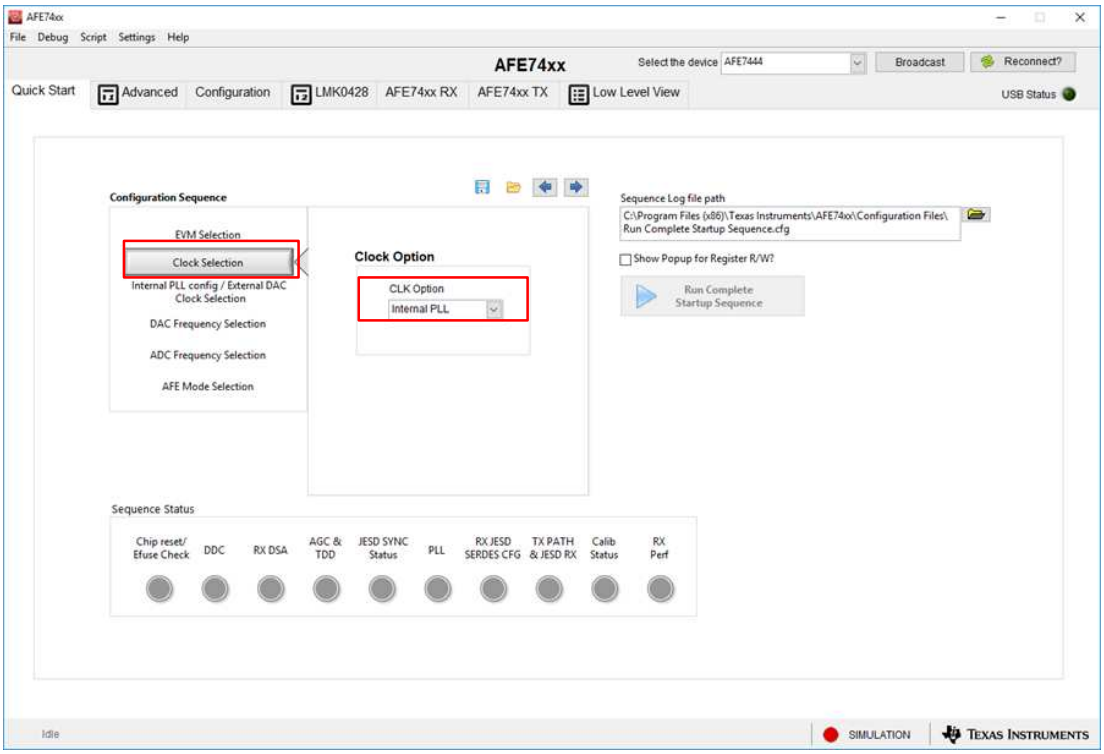

Figure 3. Clock Selection

3. Click the *DAC Frequency Selection* button, and select a DAC clock frequency of 8847.36 MHz, as shown in Figure 4.

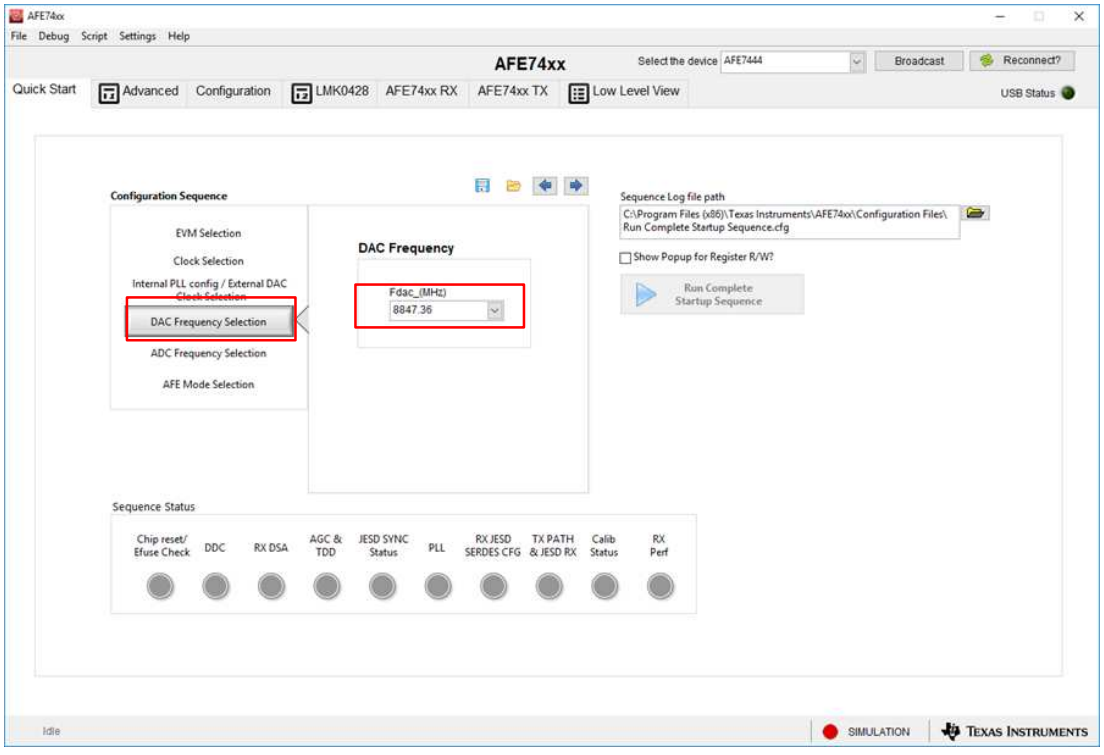

Figure 4. DAC Frequency Selection

4. Click the *ADC Frequency Selection* button, and choose a DIV factor of 3 to program the ADC clock to 2949.12 MHz, as shown in Figure 5.

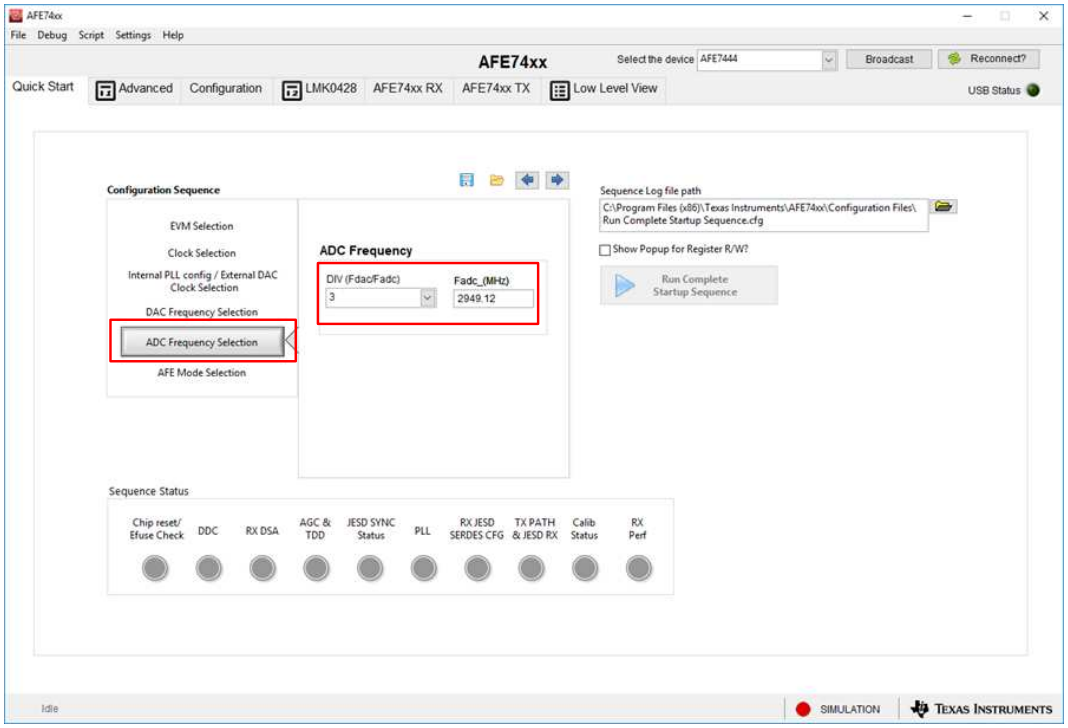

Figure 5. ADC Frequency Selection

5. As shown in Figure 6, click the *AFE Mode Selection* button, and select Mode 4.
6. Click *Set Mode*.
7. Click *Run Complete Startup Sequence* to program the AFE.

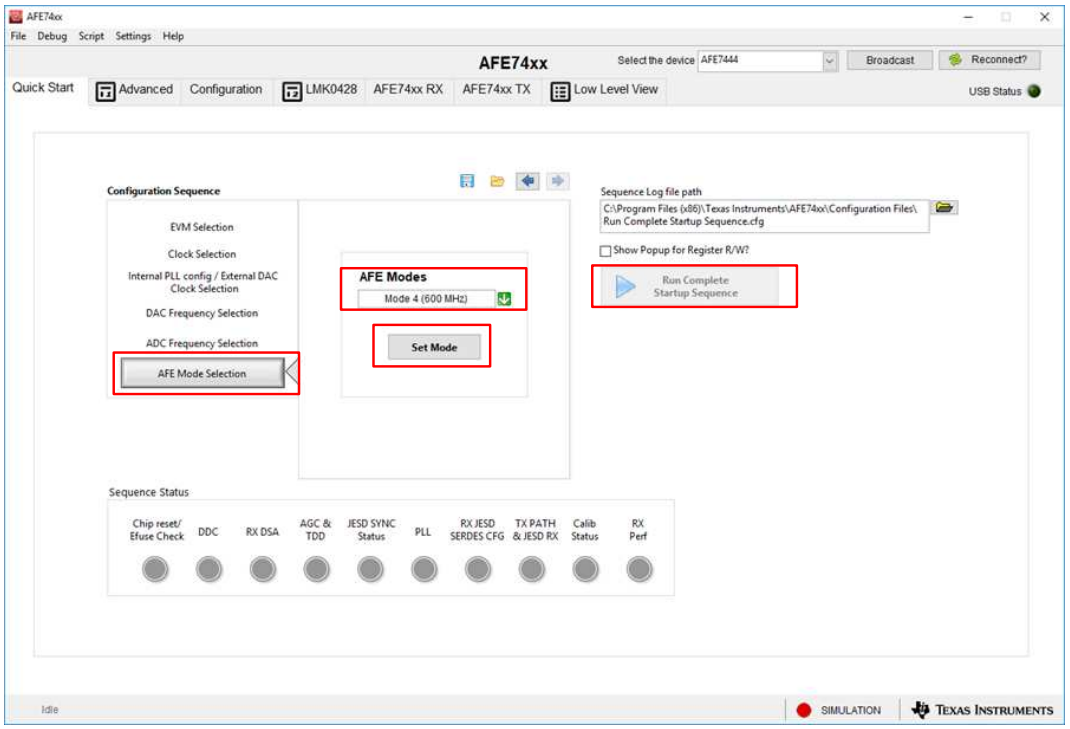

Figure 6. AFE Mode Selection

8. Select the *Advanced* tab, and click on the SYSREF continuous mode (SYSREF Cont. M) button shown in a red box in Figure 7.

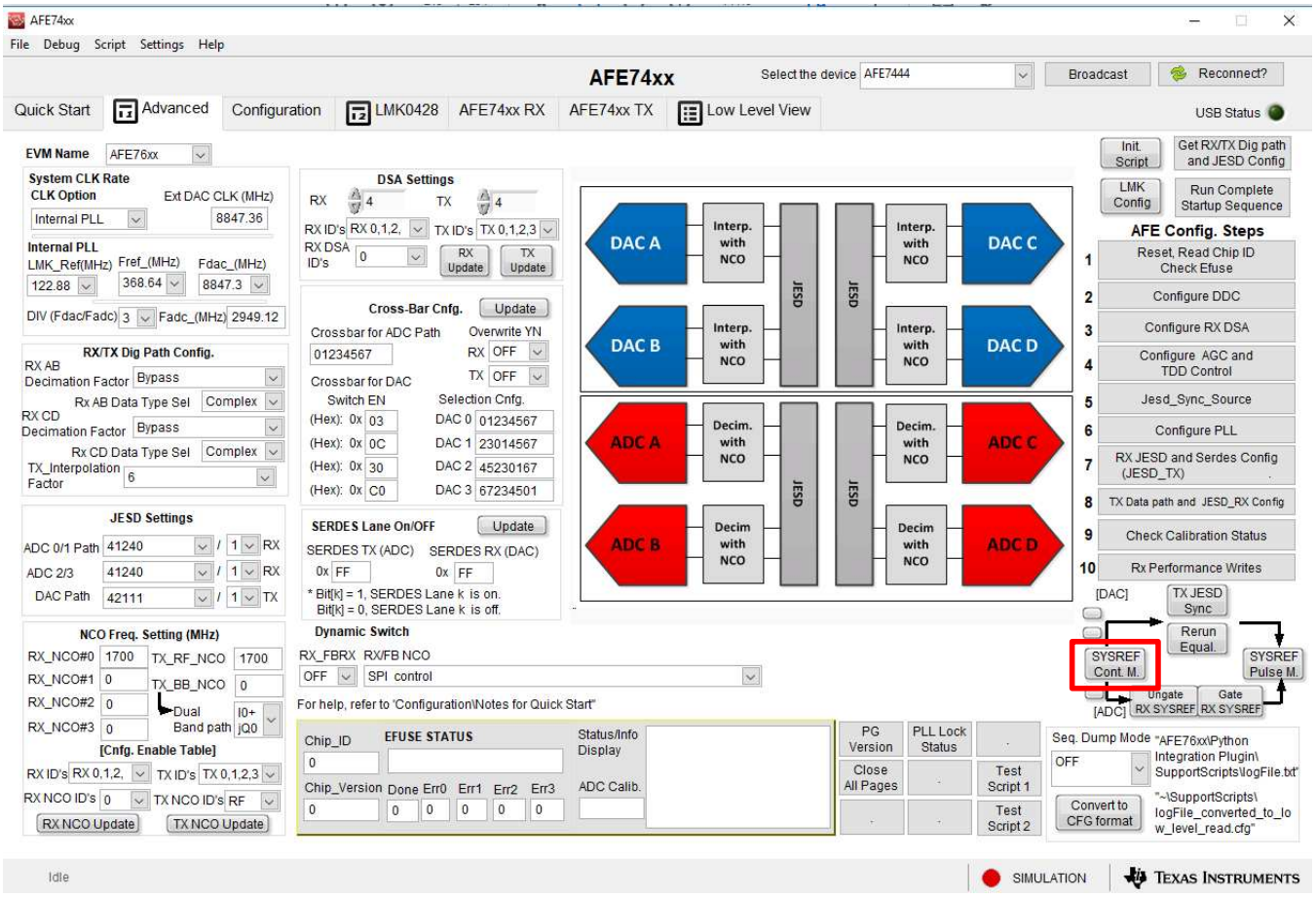

Figure 7. Advanced Tab

9. In the *Low Level View* tab, click on the open folder icon, as shown in Figure 8.
10. Load the *loopback_mode_enable.cfg* config file that was saved previously.

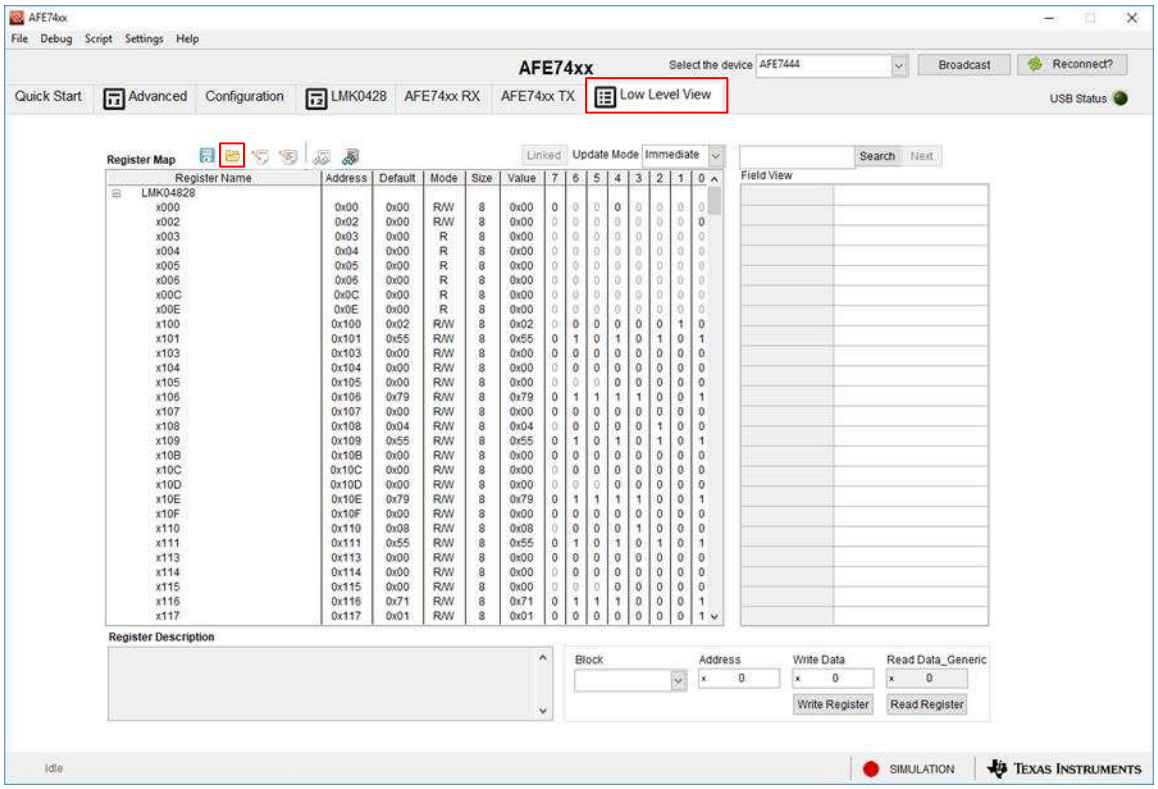

Figure 8. Low Level View Tab

11. At this point, the input signal should be visible on the DAC A output. If the output is not visible, verify that register 0x7E is set to the correct RBD value for your configuration. The RBD value depends on the F value in the AFE74xx JESD configuration mode. The RBD should be set RBD register (0x7E) to a hex value of 64 / F – 1. For example, in mode 4, LMFSHd = 44210. where F= 2. Therefore, the RBD value is 64 / 2 – 1 = 31. The hex value for 31 = 0x1F. Therefore, register 0x7E is programmed to 0x1F.
12. After the looped back input tone is verified, go back to the *Advanced* tab and adjust the RX and TX NCO values as desired, as shown in the red box of Figure 9. After the desired NCO frequency is entered, click the *RX NCO Update* or *TX NCO Update* button. The RX NCO downconverts the input signal to a digital baseband frequency. The baseband signal is upconverted to the frequency set by the TX RF NCO value. For example, the current RX NCO and TX NCO values are both set to 1700 MHz. If the input signal applied to the AFE74xxEVM is 1750 MHz, then the RX NCO downconverts the signal to a baseband frequency of 50 MHz. Then, the TX NCO upconverts the baseband signal to 1750 MHz.

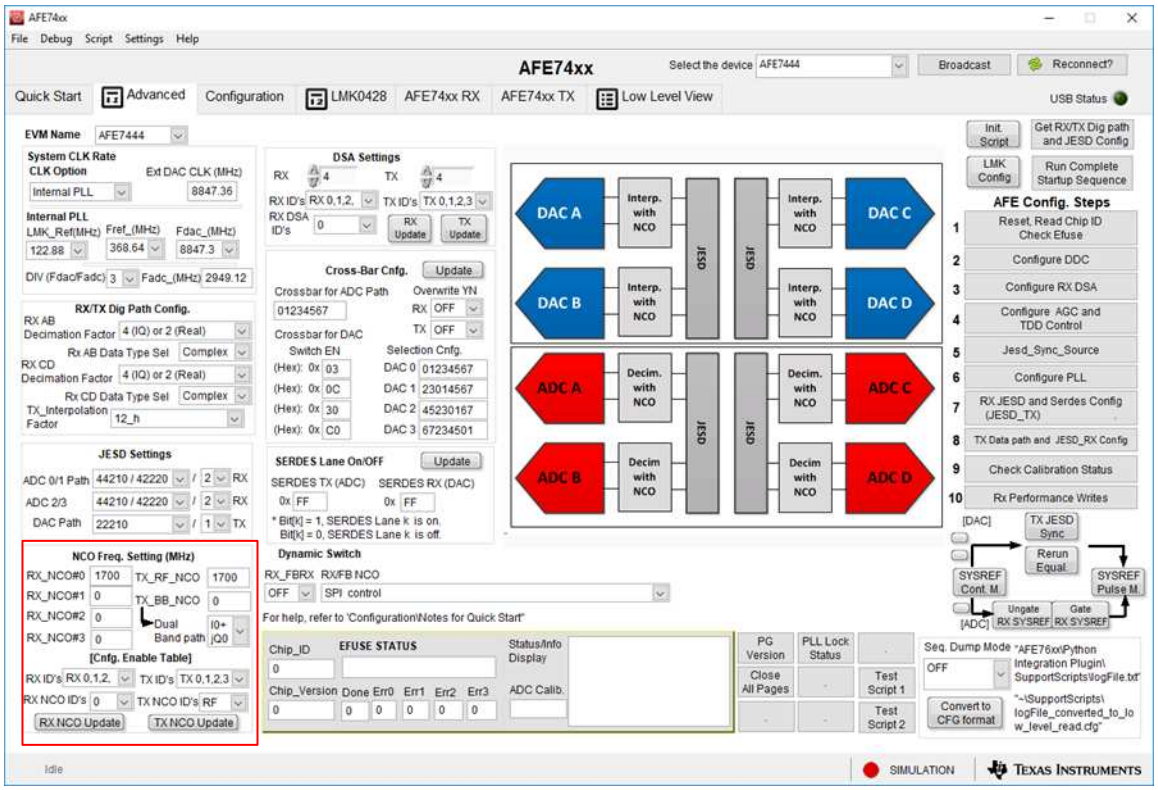

Figure 9. Adust RX and TX NCO Values to Desired Frequencies

3 130-MHz Digital Repeater System Overview

In this example, the AFE74xx is evaluated as a direct RF-sampling, single-chip 4T4R wideband repeater. The AFE74xx as a repeater supports signal bandwidths from 130 MHz to 1.2 GHz. The bandwidth of operation for the experiments conducted in this application report is 130 MHz. The goal for all wireless communication systems is to effectively distribute signals to and from users while providing optimum coverage. Such goals have driven the demand for systems to operate at higher data rates. Although not yet permanently decided, 5G is supposed to support peak data rates in the Gbps range and average user data rates of up to 100 Mbps. To achieve these data rates, wide signal bandwidths of 500 MHz, 1 GHz, and even up to 2 GHz are required. The demand for wide-band RF repeaters capable of operating with such high bandwidths is sure to increase in order to achieve optimum coverage for wireless systems. In general, RF repeaters are located throughout cells where RF signal-path obstructions exist between users and base stations. A few different repeater types follow:

- Analog: performs analog processing on received signal
- Digital: performs digital processing on received signal
- On-frequency: retransmits frequency on the same frequency that it was received
- Off-frequency: retransmits frequency on frequency other than the received signal

Typical repeater systems configurations are 4T4R made up of four 1T1R or two 2T2R subsystems. This application report showcases the AFE74xx as an integrated, single-chip, 4T4R, digital wideband repeater.

3.1 Key System Specifications

Table 2 shows the key system specifications.

Table 2. Key System Specifications

Parameter	Specifications
Selectivity	–50 dBc at +23 MHz offset from effective decimation bandwidth –70 dBc + 30 MHz offset from effective decimation bandwidth
Effective decimation bandwidth	131.07 MHz
Adjacent-channel power ratio (ACPR) degradation	approximately 9.5 dB
Latency	1.12 µs
Maximum gain	9 dBm

4 System Overview

4.1 Block Diagram

Figure 10 shows the system block diagram.

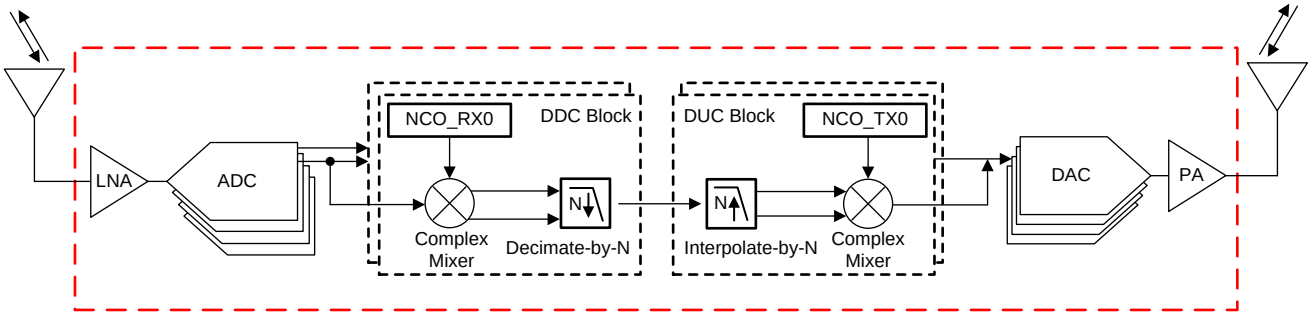

Figure 10. AFE74xx Repeater Block Diagram

4.2 Design Considerations

Important metrics when evaluating the performance of a repeater include isolation, selectivity, ac performance degradation, maximum gain and latency. Selectivity is easily one of the most important metrics when it comes to defining overall repeater system performance. The idea is to eliminate unwanted signals from being transmitted within the desired signals pass band of the repeater. This is crucial to reducing interference to operators in other bands. Antenna isolation is also very important because the output signal at the donor antenna can easily feedback to the service antenna, ultimately interfering with the input signal. The isolation between the donor antenna and the service antenna must be at least 30 dB. Repeaters introduce delay due to digital processing and filtering. The time for an input signal to travel from RX input to TX output is referred to as input-to-output group delay, and is usually denoted in terms of microseconds. Ideal repeaters are 100% transparent to the overall communication system, so latency must be as low as possible. Typical latency can range from 2 µs to 6 µs, depending on the architecture. Ideally, the repeated signal is an exact, amplified replica of the input signal. Poor ACPR performance, poor antenna isolation, and poor selectivity in a repeater can undesirably distort the input signal before the signal reaches the final destination. Therefore, a good repeater introduces minimum performance degradation at the input signal.

4.3 Highlighted Products

The AFE74xx family has an integrated (DSA) on the receiver channels, and also supports DSA equivalent functionality on the transmitter channels. Each receiver channel has one analog RF peak power detector and various digital power detectors to assist in automatic gain control (AGC) for receiver channels, and two RF overload detectors for device reliability protection. The AFE74xx family has eight JESD204B-compatible SerDes transceivers running up to 15 Gbps. The devices have up to two DUCs per TX channel, and two digital downconverters (DDC) per RX channel, with multiple interpolation and decimation rates. These devices also have digital quadrature modulators and demodulators with independent, frequency flexible NCOs. The devices support up to 600-MHz RF signal bandwidth in single-band mode, and up to 300-MHz RF signal bandwidth per band in dual-band mode. A low-jitter phase-locked loop (PLL) voltage-controlled oscllator (VCO) simplifies the sampling clock generation by allowing use of a lower-frequency reference clock. The primary components discussed in this application report are the AFE7422 and AFE7444 (4T4R capable). As a 4T4R system, this repeater has the ability to operate on two separate bands using a 2T2R configuration for each repeating link.

4.3.1 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. An onboard 122.88-MHz, voltage-controlled crystal oscillator (VCXO) provides the reference frequency. This reference frequency can be locked to an external 10-MHz reference if desired. The LMK04828 supplies the JESD204B SYSREF clocks to the ADC and FPGA, and passes the 122.88-MHz reference signal to the LMX2582 for the reference.

4.4 System Design Theory

A digital RF repeater accomplishes the following goals:

- Shows good selectivity by eliminating unwanted signals from being transmitted within the desired signals passband, which reduces interference in other bands
- Shows good antenna isolation between the donor and the service antenna
- Has low RX to TX latency
- Shows low ac-performance degradation.

Figure 11 shows the basic, traditional, RF-repeater design architecture.

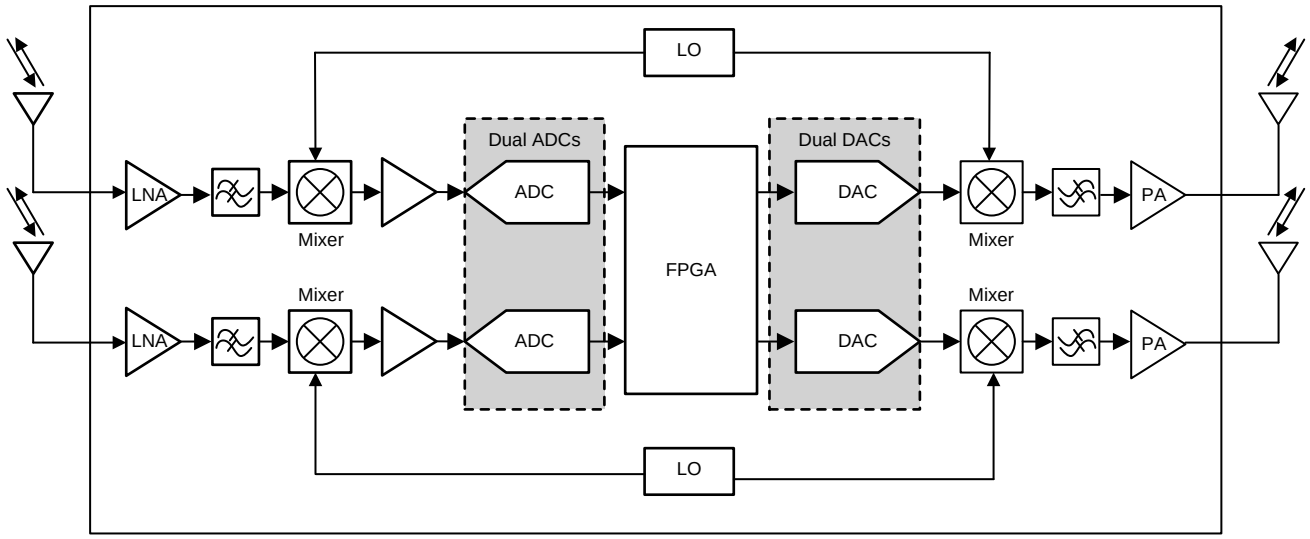

Figure 11. Traditional Digital RF Repeater

The traditional repeater architecture first conditions the input signal using filters and LNAs. The local oscillator (LO) mixer downconverts the band to an intermediate frequency. The signal is filtered, sampled, and then sent to an FPGA for digital processing. The downmixing process is then reversed, and the final signal is output through the donor antenna to the desired base station.

All of the frequency translation functions of the traditional RF repeater are performed in the digital domain of the integrated AFE74xx system. This system replaces the need for discrete mixers, IF filters, and LOs (PLLs) from the analog-signal chain in order to achieve direct synthesis.

5 Hardware and Testing

5.1 Measured Latency and Gain

The goal of this measurement is to evaluate the group delay and maximum gain of the RX-TX repeater using an Agilent E5071B network analyzer.

5.1.1 Hardware

The hardware used to test is as follows:

- Rohde and Schwarz SMA 100 signal generator
- DAC38RF82 RF DAC EVM
- Agilent E4443A spectrum analyzer
- Agilent E5071B network analyzer

5.1.2 Test Setup and Results

Figure 12 shows the setup. Port 1 drives the input of the repeater with frequencies ranging from 1900 MHz to 1920 MHz, and port 2 receives the signals from port 1, documenting the time of flight from Port 1 to Port 2. The average group delay is approximately 1.12 µs. Figure 13 shows a graph of latency as a function of frequencies between 1900 MHz and 1920 MHz.

The maximum gain was determined using the same setup as group delay and is approximately 9 dBm when both of the RX and TX DSA settings are set to 0. Figure 14 shows a graph of gain verses frequencies between 1900 MHz and 1910 MHz.

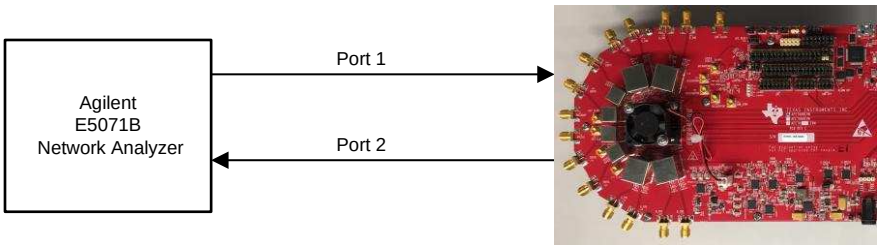

Figure 12. Latency and Gain Test Setup

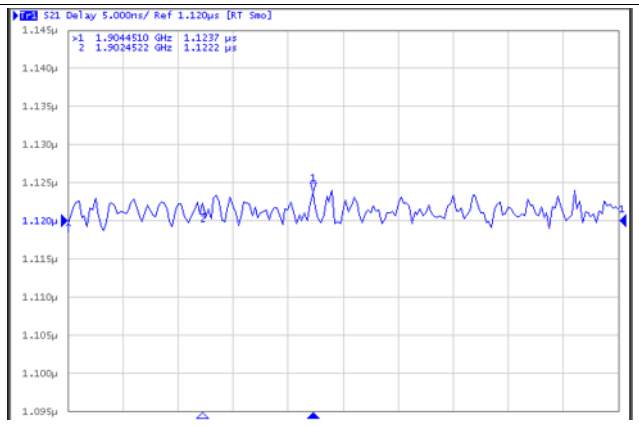

Figure 13. Latency Measurement, Average Latency = 1.12 µs

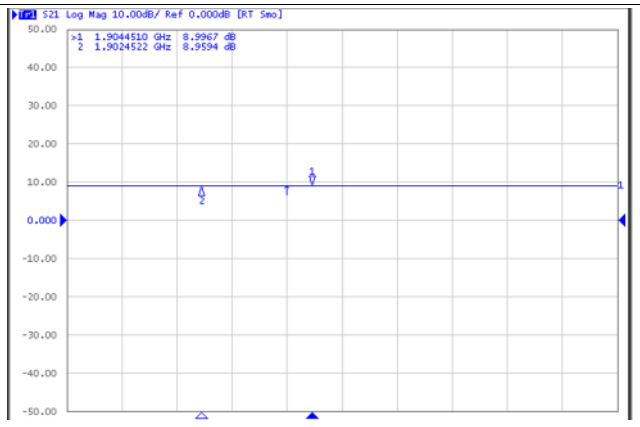

Figure 14. Gain Measurement: Gain is Flat at 9 dBm With TX/RX DSA Set to 0

5.2 Measured Linearity Performance

The goal of this measurement is to evaluate the transparency of the repeater by showing the ACPR degradation of a signal through loopback.

5.2.1 Hardware and Test Setup

The DAC38RF82 is an RF DAC that generates the signal of the ACPR performance measurements. When measuring ACPR degradation, the RF DAC outputs a clean 20-MHz long-term evolution (LTE) signal centered at 1907 MHz. The output signal of the DAC first passes through a band-pass filter before being connected to the input of the repeater.

Figure 15 shows the test setup for ACPR degradation. The ACPR of the LTE waveform is measured directly at the output of the DAC and also at the output of the repeater using the spectrum analyzer. The comparative difference in ACPR is the degradation of the LTE waveform due to the repeater.

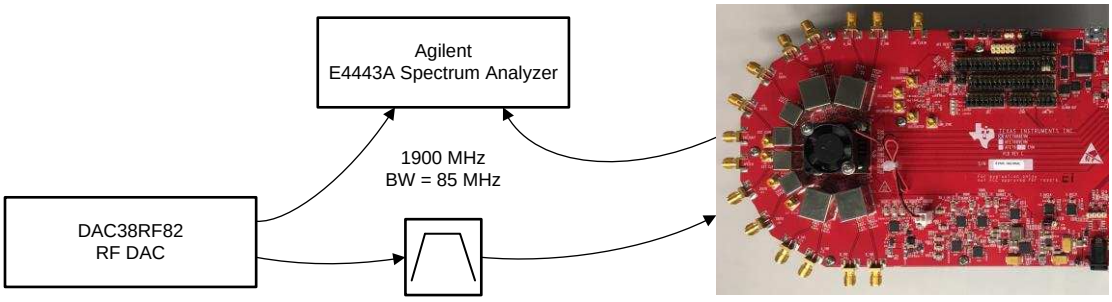

Figure 15. Test Setup for ACPR Degradation

5.2.2 Test Results

Figure 16 and Figure 17 show that the before and after LTE ACPR measurements of the repeater are approximately 73 dB and 65 dB, respectively. The ACPR degradation caused by the receiver is approximately 9 dBm. Notice that the reference level offset in Figure 17 increased by 2 dB to account for the loss due to the filter and the extra SMA cables. The RX and TX DSAs were set to 1 and 0, respectively, in order to yield an overall gain of 6 dB.

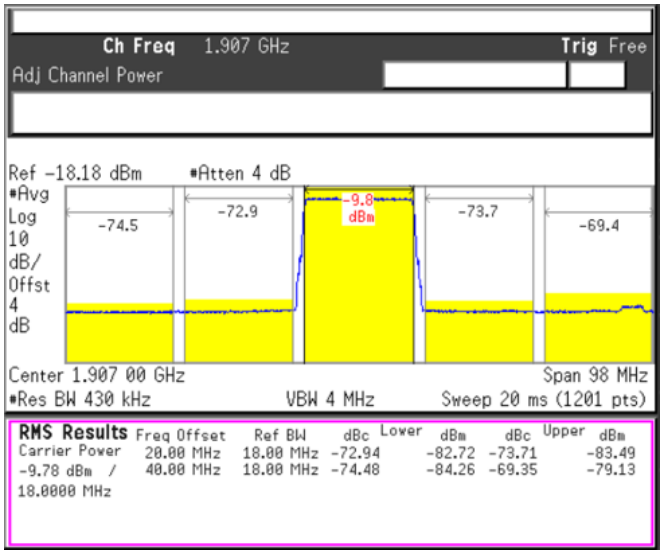

Figure 16. Clean ACPR Measurement Directly From DAC38RF82

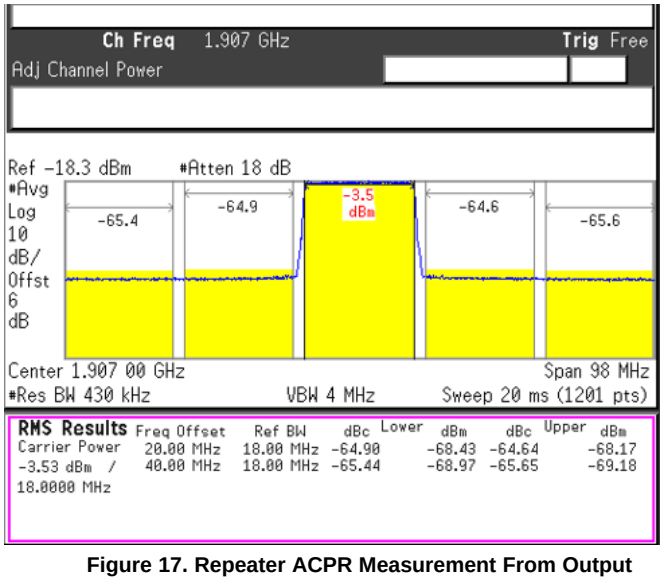

Figure 17. Repeater ACPR Measurement From Output Shows 6-dB Gain of Waveform and 8-dB ACPR Degradation

5.3 Measured Selectivity (Out-of-Band Jammer)

The goal of this measurement is to characterize the in-band selectivity by sweeping a jammer in the transition band of the repeater and recording the rolloff. Digital processing takes place in the on-chip DDC and digital upconverter (DUC). Therefore, the transition-band rolloff is fully dependent on the interpolation and decimation filters.

5.3.1 Hardware and Test Setup

A DAC38RF82 is used to generate two 20-MHz LTE carriers spaced at 100 MHz and centered at 1870 MHz. The LTE carriers simulate a 120-MHz wideband signal. A jammer signal is simulated by a CW tone produced by a SMA Rhode and Schwartz signal generator. A 350-MHz to 6-GHz, mini-circuits power splitter combines the wideband signal and CW tone to the input of the repeater. Figure 18 shows a block diagram of the setup.

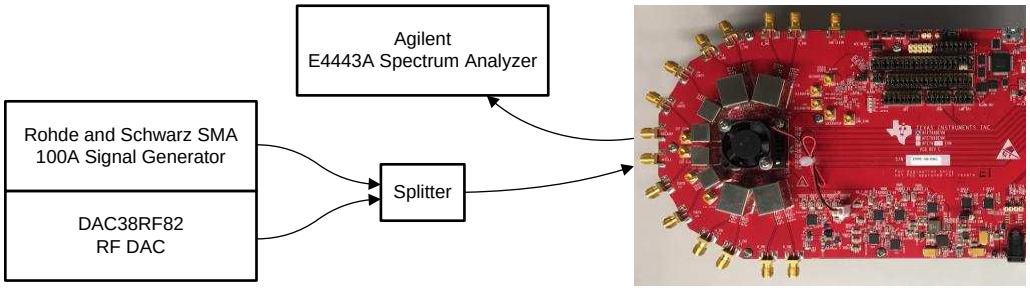

Figure 18. Hardware Setup for Jammer Simulation

5.3.2 Test Results

Figure 19 shows a repeated 120-MHz wideband signal at the output of the repeater without the jammer present. Figure 20 shows the jammer swept from the edge of the effective decimation pass band, through the transition band until the jammer is fully attenuated. The resulting measurement shows –50 dBc of attenuation at 23 MHz, as denoted by marker 2.

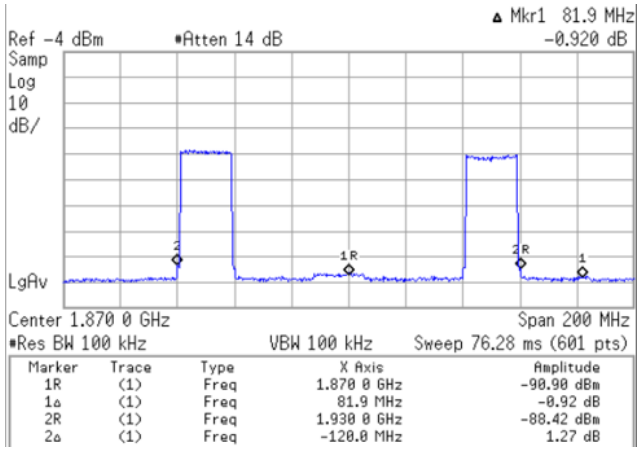

Figure 19. Repeated Wideband Signal Simulating a 120-MHz Carrier

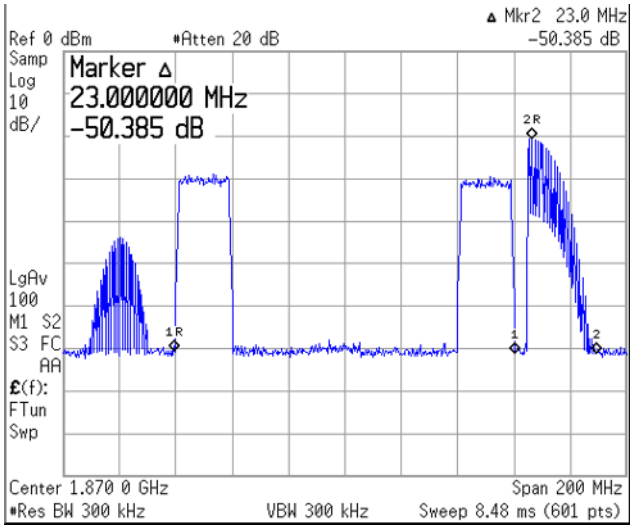

Figure 20. –50-dBc Attenuation at 23-MHz Outside Decimation Bandwidth

6 Terminology

Downlink: Traffic transmitter for the communication link, with respective to the main data source at the service provider

TX: Traffic transmitter for the communication link

TXDAC: Digital-to-analog converter used for traffic transmitter

Uplink: Traffic receiver for the communication link, with respective to the main data source at the service provider.

RX: Traffic receiver for the communication link

RXADC: Analog-to-digital converter used for traffic receiver or feedback receiver

DPD: Digital predistortion for power amplifier linearization

PA: Power amplifier for transmitter link

LNA: Low-noise amplifier for receiver link

DAS: Distributed antenna system

MU: Master unit in DAS

RU: Remote unit in DAS

BTS: Base station unit

MIMO: Multiple-input-multiple-output

JESD204B: JEDEC standard for high-speed serial link for data converters.

PLL: Phase-locked loop

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