Application Report
SLAA488–August 2011

MSP430AFE253 Test Report for China State Grid Specification

Percy Yu, Vincent Chan — *MSP430 Systems Applications*

ABSTRACT

The Flash-programmable 16-MHz MSP430AFE253 device developed by Texas Instruments is a highly flexible and powerful single-chip mixed-signal measurement device targeting electricity meter and sub-meter applications.

In such applications, high reliability and accuracy of better than 0.1% is often required.

This applicaton report demonstrates robust real-time embedded software running on the MSP430AFE253 device and the test cases it has passed. This firmware is developed to meet the China State Grid (CSG) specification for single-phase electricity meters. The software covers the use of the on-chip analog front end to measure electricity as well as other related metering parameters.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/slaa488.

Contents

1 Introduction 2
2 Test System Setup 2
3 Use of the GUI 7
4 Demo E-Meter Host MCU Program 10
5 CSG Firmware Briefing 11
6 Test Specification 12
7 References 20
Appendix A MSP430F4481 Communication Protocol 21
Appendix B CSG Firmware Access and Operation 25

List of Figures

1 Demo Meter and MSP-EXP430FG4618 Demo Board 3
2 Test System Setup 4
3 Connection Between Demo Meter and MSP-EXP430FG4618 Demo Board 5
4 Check Serial Port Number for MSP-EXP430FG4618 Demo Board 6
5 Modify Serial Port Number in calibration-config.xml 6
6 Main Frame Window of calibrator.exe 7
7 Meter Status Window 8
8 Meter Configuration Window 9
9 Meter Calibration Factors Window 10
10 MSP430F448 Host Program Flowchart 11
11 MSP430AFE CSG Firmware Flowchart 12
12 Demo E-Meter Connection for CSG Test 13
13 Corrupted Data Through SPI 18
14 Corrupted Clock - Additional Clock 19
15 Corrupted Clock - Missed Clock 19

16 Power-On Sequence 20
17 SPI Timing 25
18 CSG Firmware Communication Packet 26
19 CSG Firmware Phase Calibration 37

1 Introduction

The test cases developed for this application are divided into three parts:

- Functional tests
- Performance tests
- Robustness tests

This firmware is referred to as CSG firmware in this document.

Note that a key focus of this document is to describe the test procedures developed for the CSG specification-based electricity metering code. For a description of the actual CSG specification itself, see the GB standard documentation (GB/T 17215.321-2008).

2 Test System Setup

A complete single-phase meter is built to enable the development and testing of the embedded software. This meter consists of an MSP430F4481 device as the main MCU and the MSP430AFE253 as the front-end measurement device. The 'F4481 drives the serial peripheral interface (SPI) to the 'AFE253. A serial port connects the meter to an external PC. A GUI, running on the PC, allows you to set the modes of the 'AFE253 and to calibrate the system. Figure 1 to Figure 3 display the system setup.

2.1 Hardware Setup

Four parts are used in this test:

- Single-phase demo meter
- MSP-EXP430FG4618 demo board
- Laptop
- E-meter test facility

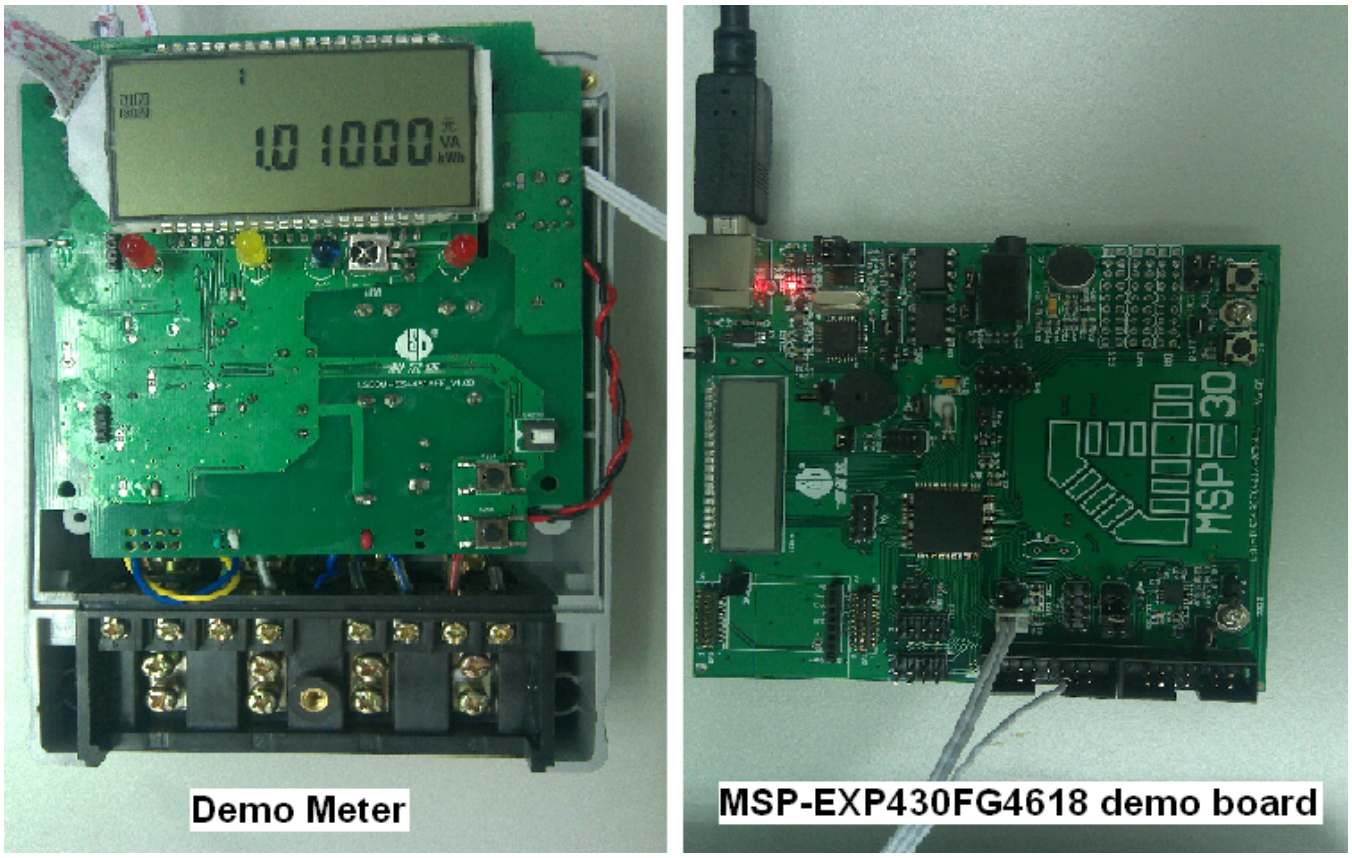

Figure 1. Demo Meter and MSP-EXP430FG4618 Demo Board

The test system is arranged as illustrated in Figure 2.

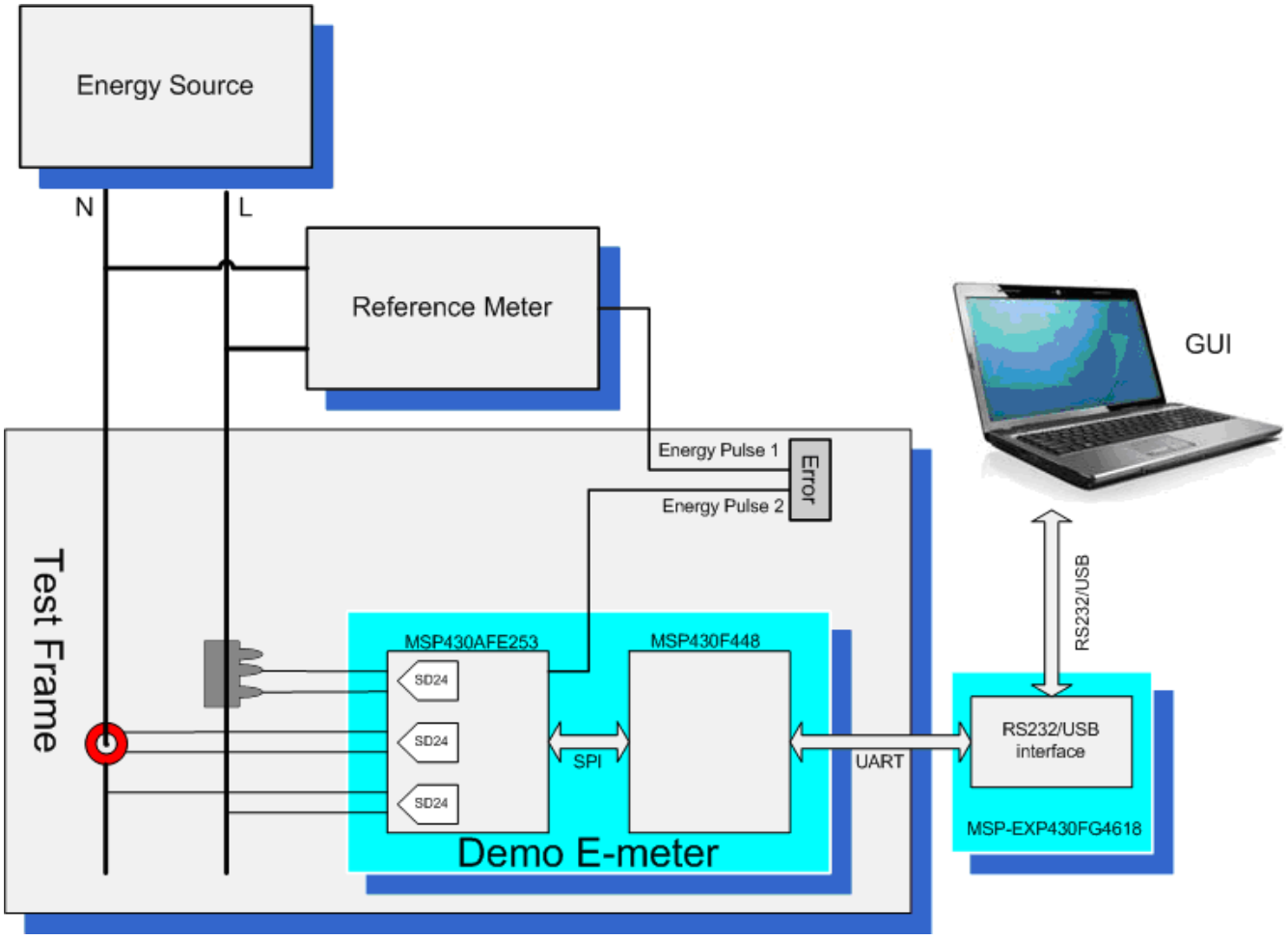

Figure 2. Test System Setup

Figure 3 shows the connection between the demo meter and the MSP-EXP430FG4618 board.

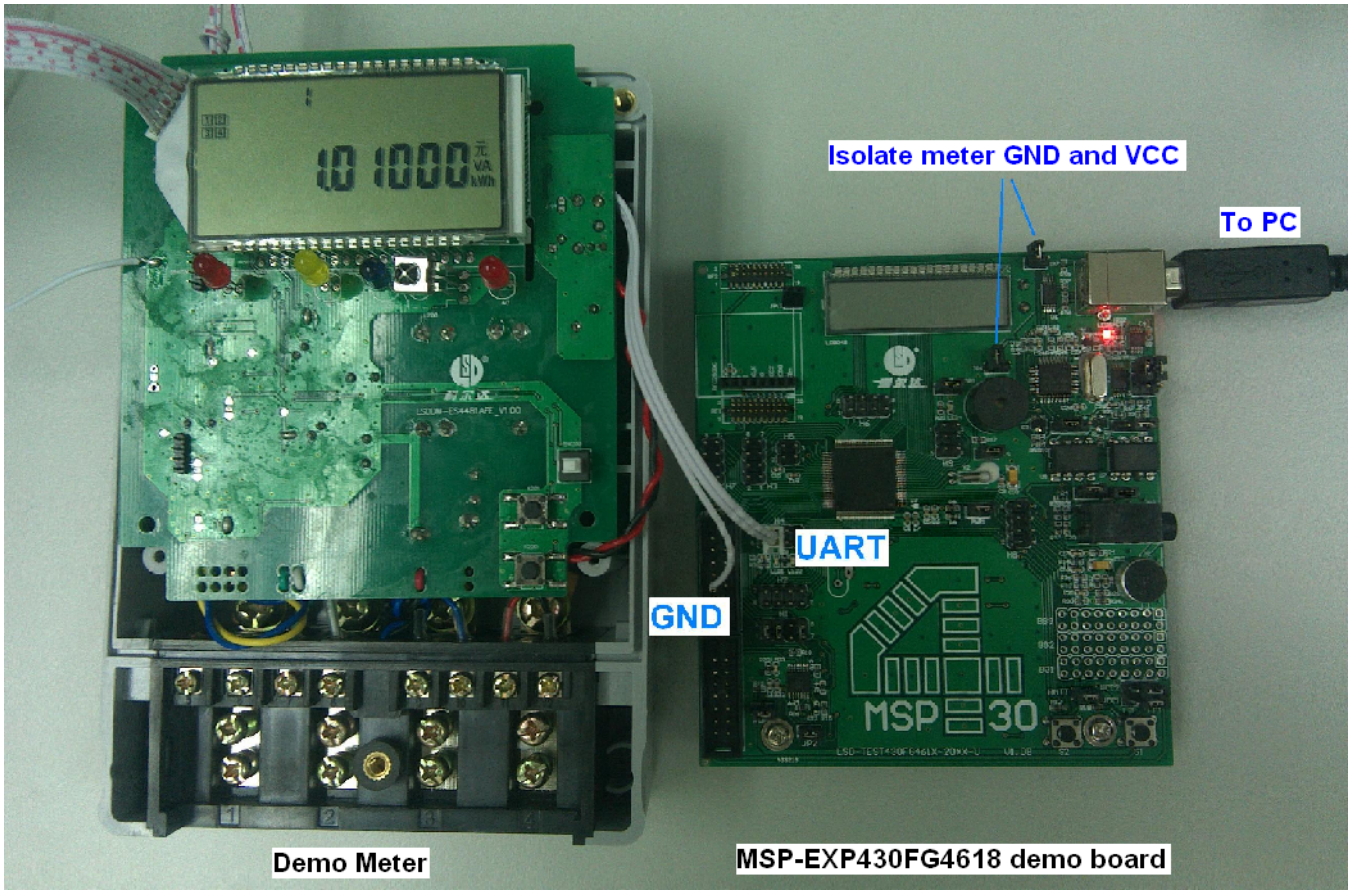

Figure 3. Connection Between Demo Meter and MSP-EXP430FG4618 Demo Board

2.2 Communication link Setup

The software include three parts:

- MSP430AFE253 firmware
- MSP430F4481 host firmware
- Windows® GUI calibrator.exe

Program MSP430AFE253 and MSP430F4481 with corresponding firmware before test.

There are two kinds of MSP-EXP430FG4618 boards: one with RS232 interface and the other with USB interface. If the RS232 interface board is used, it defaults to COM1 in the laptop computer. In these tests, the USB version of the MSP-EXP430FG4618 board from a third party LSD was used, which integrates USB interface to the PC and can provide higher baud rate communication. The Windows system dynamically assigns a port number to it. Follow these steps to choose the right port for the GUI.

1. Plug the USB connector into the MSP-EXP430FG4618 board.
2. Check the Device Manager in Windows and find the serial port number that MSP-EXP430FG4618 device occupies (see Figure 5).

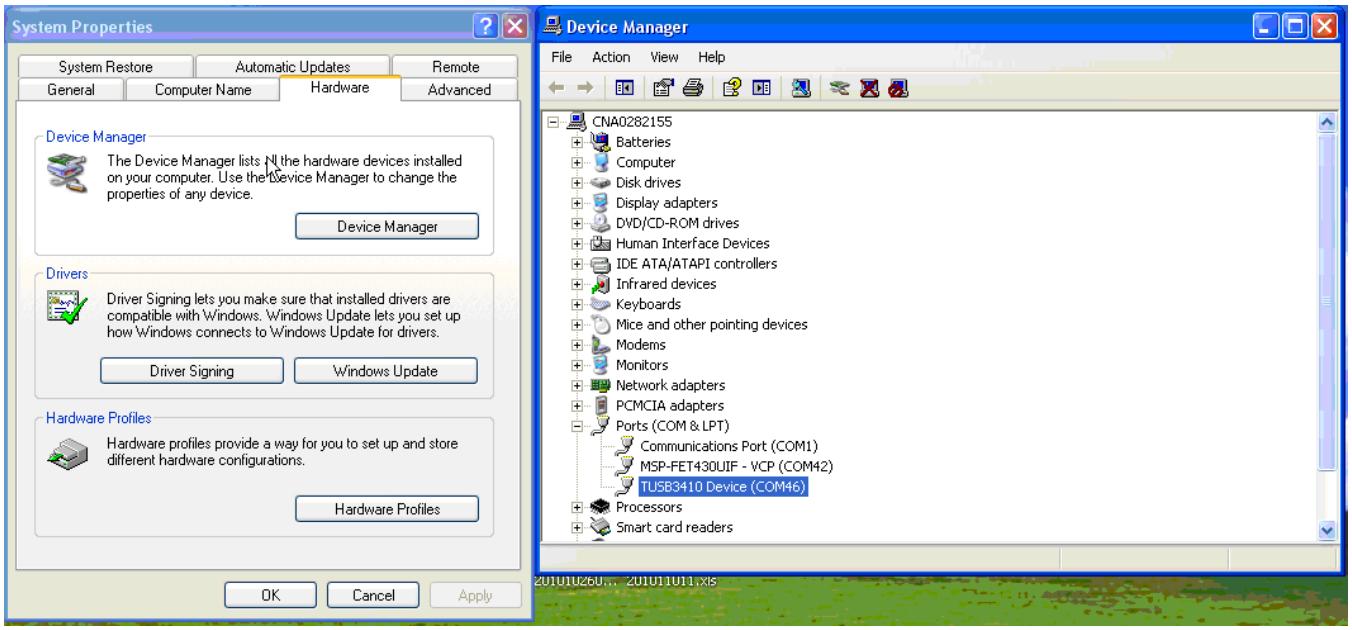

Figure 4. Check Serial Port Number for MSP-EXP430FG4618 Demo Board

3. Modify the port number setting in calibration-config.xml (included in the GUI packet) and give the correct port number (see Figure 5). The calibration-config.xml file is used by Calibrator.exe as the configuration file.

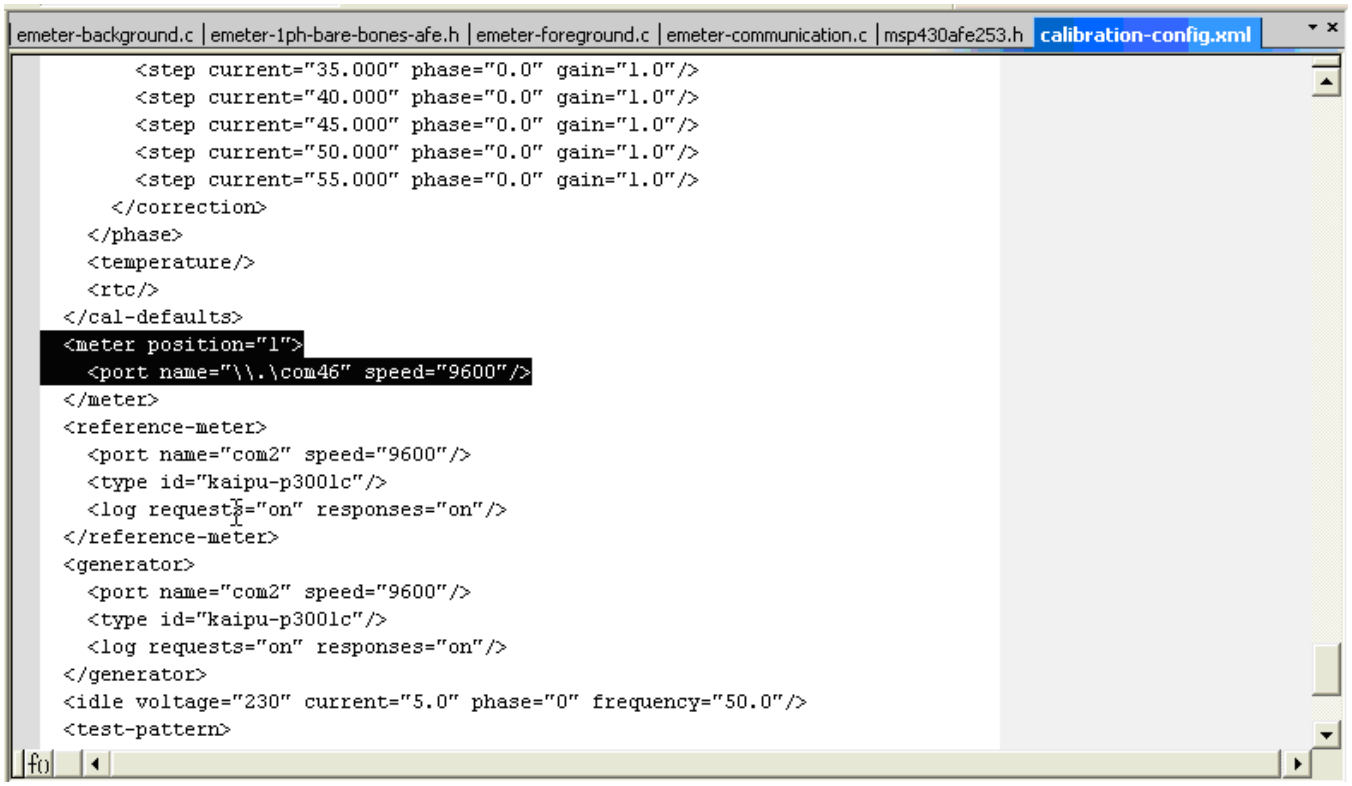

Figure 5. Modify Serial Port Number in calibration-config.xml

3 Use of the GUI

Calibrator.exe provide the following functions:

- Read out metering parameters
- Calibrate meter
- Set meter registers

The main frame window of Calibrator.exe is shown in Figure 6:

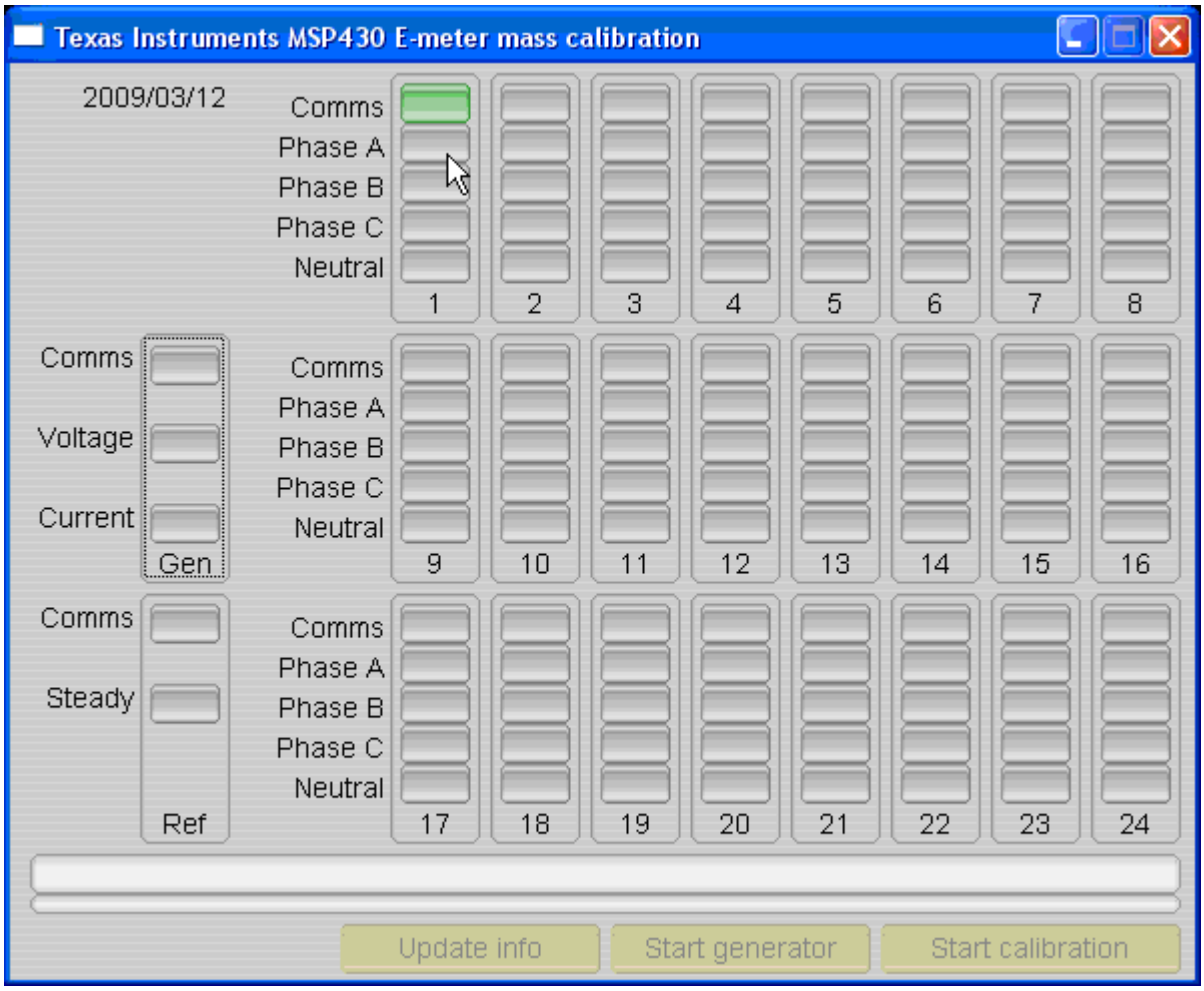

Figure 6. Main Frame Window of calibrator.exe

3.1 Metering Parameters Window

Calibrator.exe supports communication up to 24 meters. There are 24 columns on the control panel of the main frame window (see Figure 6), each represents one communication task for one meter. The green light on column 1 shows communication to meter 1 (here the demo e-meter) is active.

Click on column 1 on the main frame window to prompt the meter status window as illustrated in Figure 7:

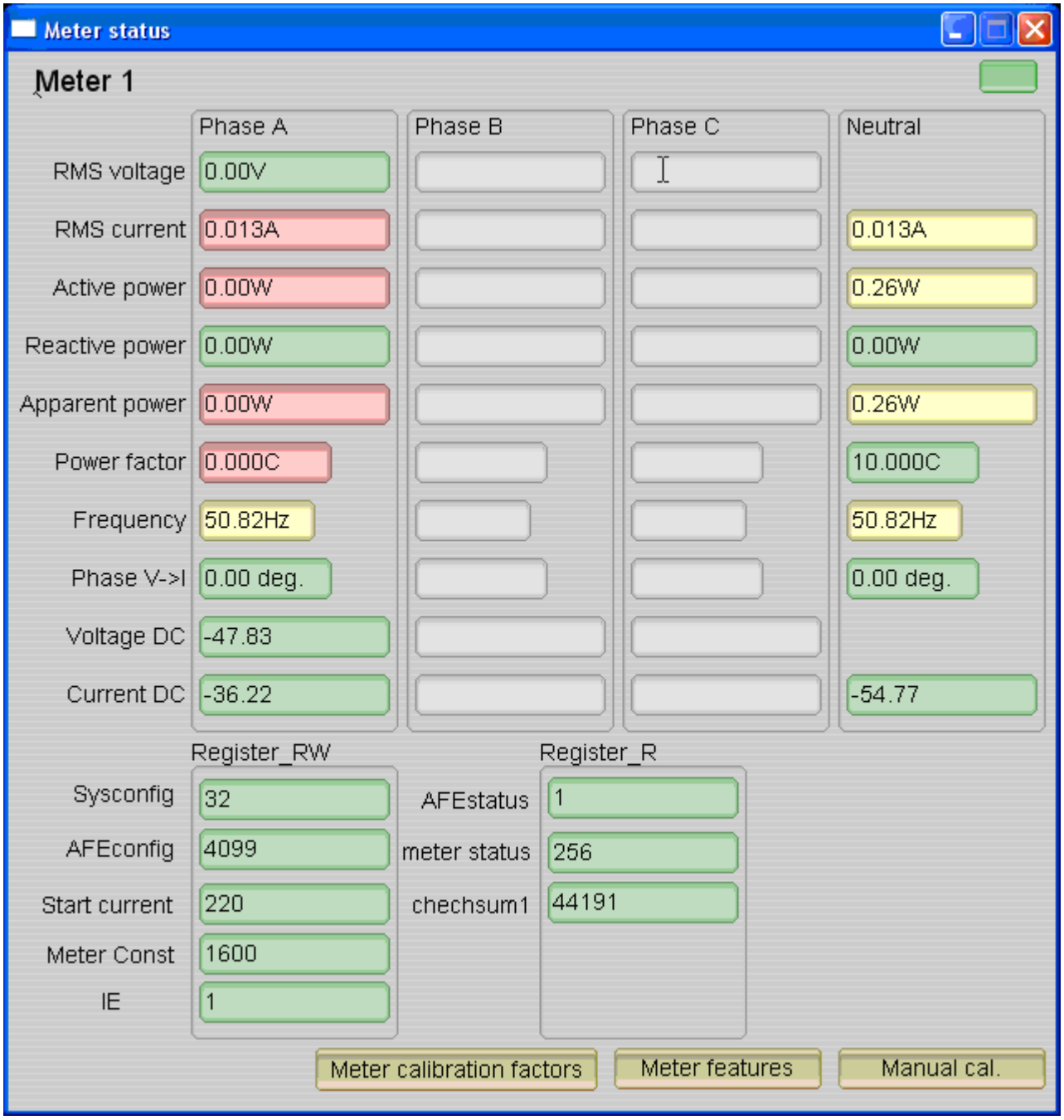

Figure 7. Meter Status Window

The meter status window shows all metering parameters and registers read from the demo e-meter. This is a read-only window.

3.2 Meter Calibration and Function Setting

Click on the manual calibration button on the meter status window (see Figure 7) to prompt the meter configuration window (see Figure 8):

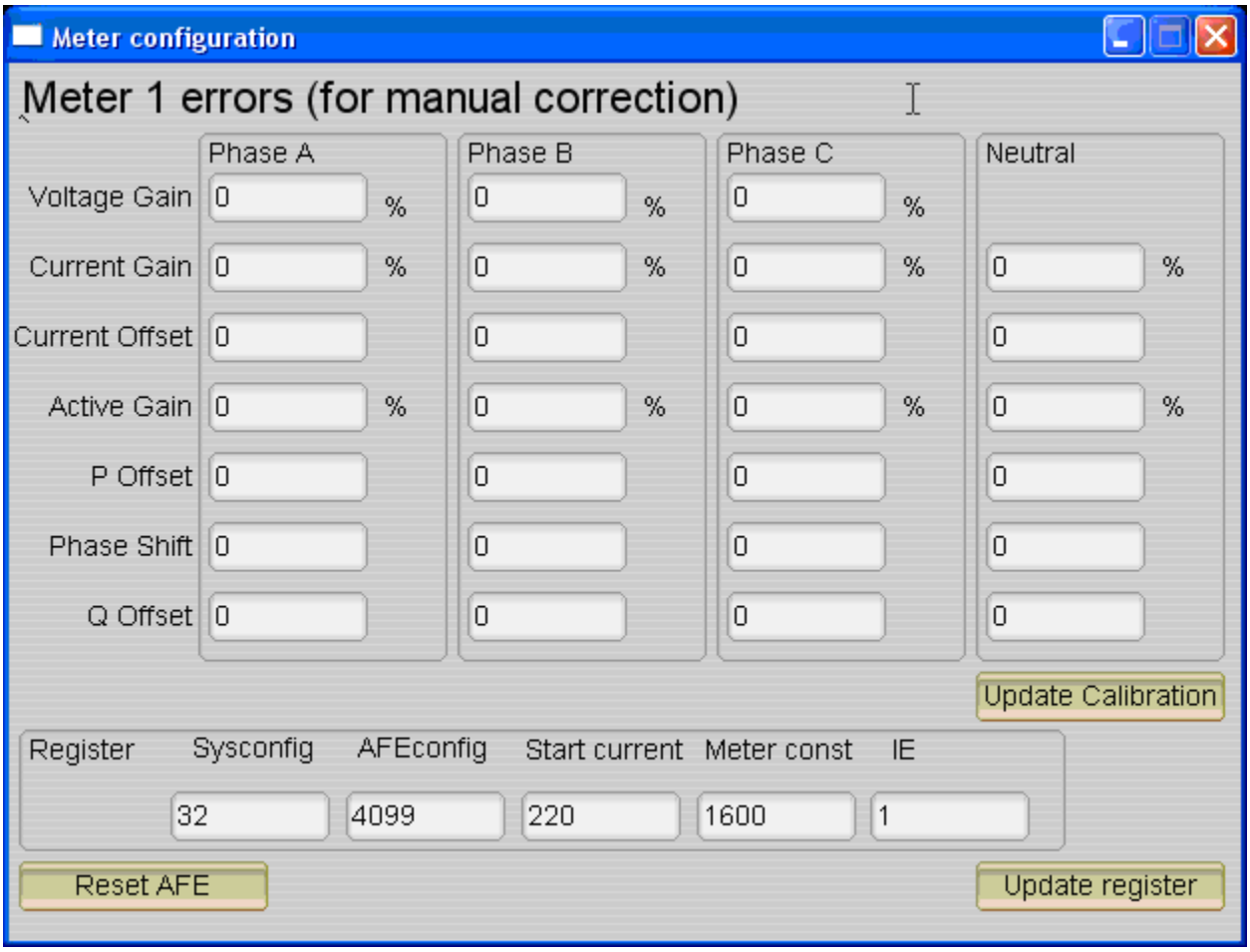

Figure 8. Meter Configuration Window

The meter configuration window contains two parts: upper and lower.

The upper part of the meter configuration window is used for meter calibration. It allows you to calibrate the demo meter on active power slope, phase shift, power offset (including active power and reactive power), Vrms slope, Irms slope, and Irms offset by entering measurement errors in the corresponding edit box and clicking on the Update Calibration button. For example, if the calculated active power slope error for phase A is 0.3% and the active power offset for phase A is 2200 mW, just type 0.3 on the Active Gain edit box and 220 on the P Offset edit box within Phase A column, then press the Update Calibration button. The GUI calibrates the demo e-meter according to the entered number. As for how to calculate calibration factors, see Section B.2.4.

You can also check the demo e-meter's current calibration factors from the Meter calibration factors window (see Figure 9), which is activated by clicking on the Meter calibration factors button on the Meter status window (see Figure 7).

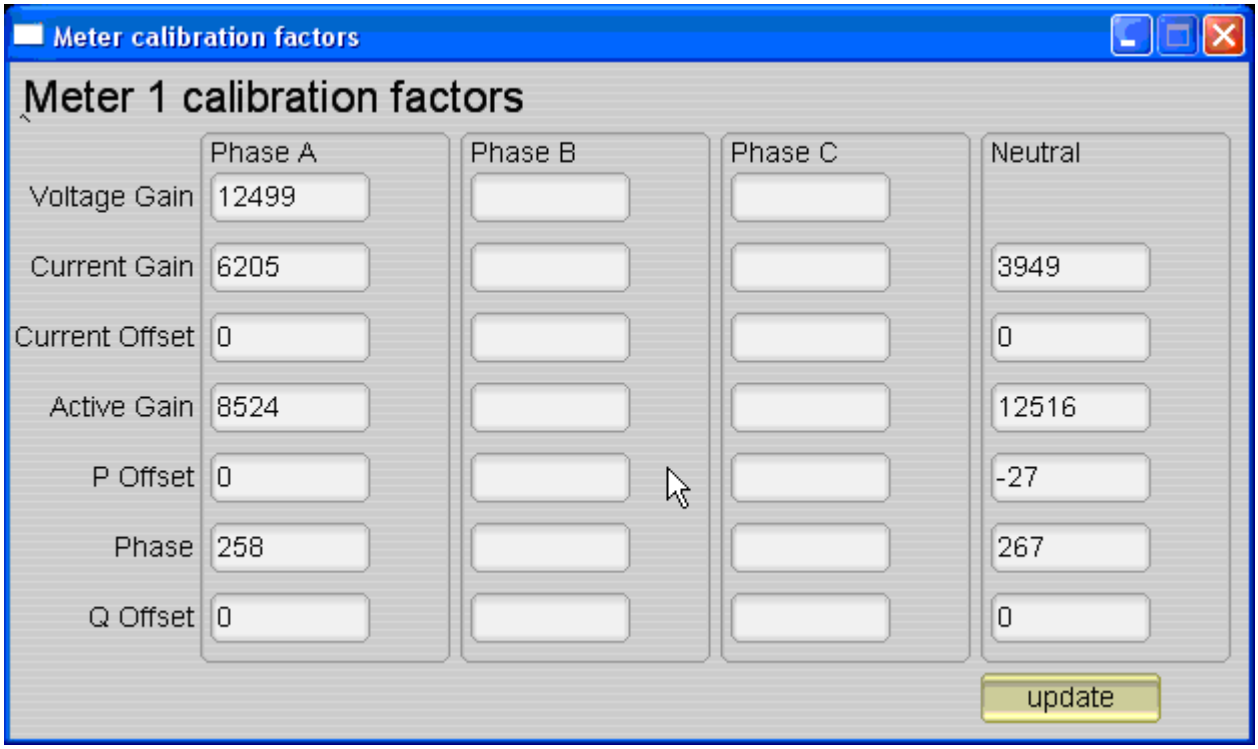

Figure 9. Meter Calibration Factors Window

The lower part of the meter configuration window (see Figure 8) is used to set the demo e-meter's system registers. It allows you to change the demo e-meter functions by entering new system register values in corresponding edit boxes and click the Update register button. For example, if you want to set meter energy pulse const to 800, type 800 on the Meter const edit box and press Update register button.

The detailed information of calibration and meter registers is discussed in Section B.2.4.

4 Demo E-Meter Host MCU Program

The host MCU MSP430F4481 provides application level service of a typical energy meter and acts as a bridge between the analog front end (AFE) and the end user; in this case, the end user refers to the GUI calibrator.exe. Its functions mainly includes two parts:

- Decode GUI requests and operate on AFE accordingly.
- Access AFE253, readout metering parameters, and set AFE function mode.

In MSP430F4481, universal synchronous/asynchronous receiver/transmitter (USART0) is configured in SPI mode and used to talk with the MSP430AFE253. USART1 is configured in universal asynchronous receiver/transmitter (UART) mode and used to talk with the PC GUI in 9600 baud rate. The MSP430F4481 program always waits for the PC GUI command, then decodes it and performs the required operation accordingly

The basic timer is set to trigger 1 second interrupt, in which time the ISR F4481 program reads all of the MSP430AFE253 parameters and stores them in static array. This action is without control of the PC GUI and assures that the MSP430F4481 device always has the most updated image of all the AFE registers.

Figure 10 illustrates the data flowchart of the MSP430F4481 program.

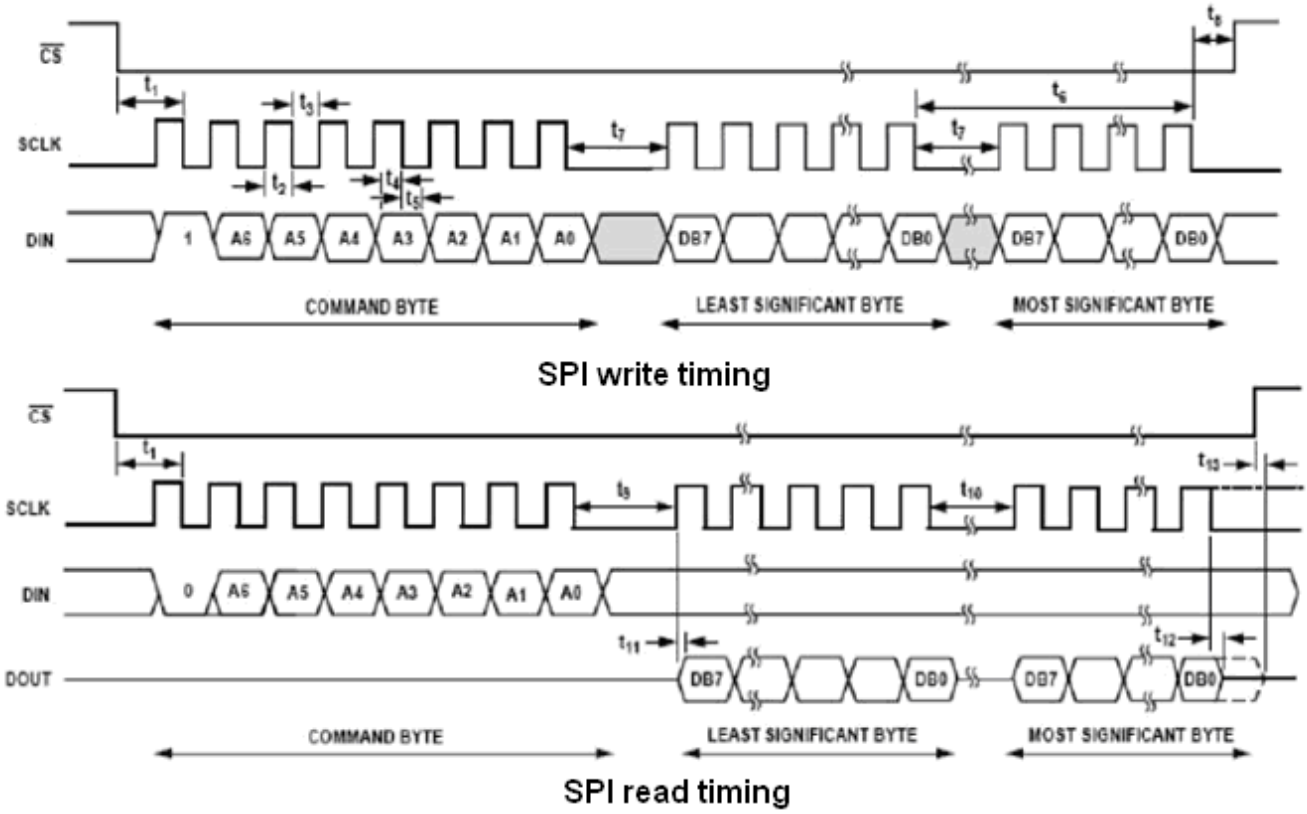

Figure 10. MSP430F448 Host Program Flowchart

Detailed communication protocol and timing is described in Appendix A.

5 CSG Firmware Briefing

The MSP430AFE253 running the CSG firmware enables a hardware and software self-contained system that measures electrical parameters without the need of a host processor. The MSP430AFE253 integrates on-chip a 3-channel SD24 module, a hardware multiplier module, and an SPI interface.

Features of the CSG firmware include:

- A complete analog and digital functionality for China State Grid's single-phase meter specification
- Reactive power and apparent power support
- Two-wire and three-wire applications
- Tamper detection functionality
- Built-in calibration features and flexible user-configurable system setup
- Integrated AFE for voltage and current sampling
- Independent configurable analog input gain
- Self adaptable three-wire or four-wire SPI communication

5.1 CSG Firmware Operation

In MSP430FAFE253, three channel SD24 are grouped and set to be triggered in 4-HKz intervals and sampled on mains voltage, live current and neutral current. Using the integrated multiplier, the AFE253 MCU calculates electrical parameters based on sampled values in a self-contained manner.

CSG firmware setup, control, and access are provided by accessing CSG registers. These registers fall into three categories: system, calibration, and parameter registers. The host MCU accesses CSG firmware via SPI interfaces.

In CSG firmware, USART0 is configured in SPI mode and the RX interrupt is switched on. CSG firmware decodes all receiving packets and performs register accessing based on the host MCU command.

Figure 11 shows the data flowchart of the MSP430AFE253 CSG firmware.

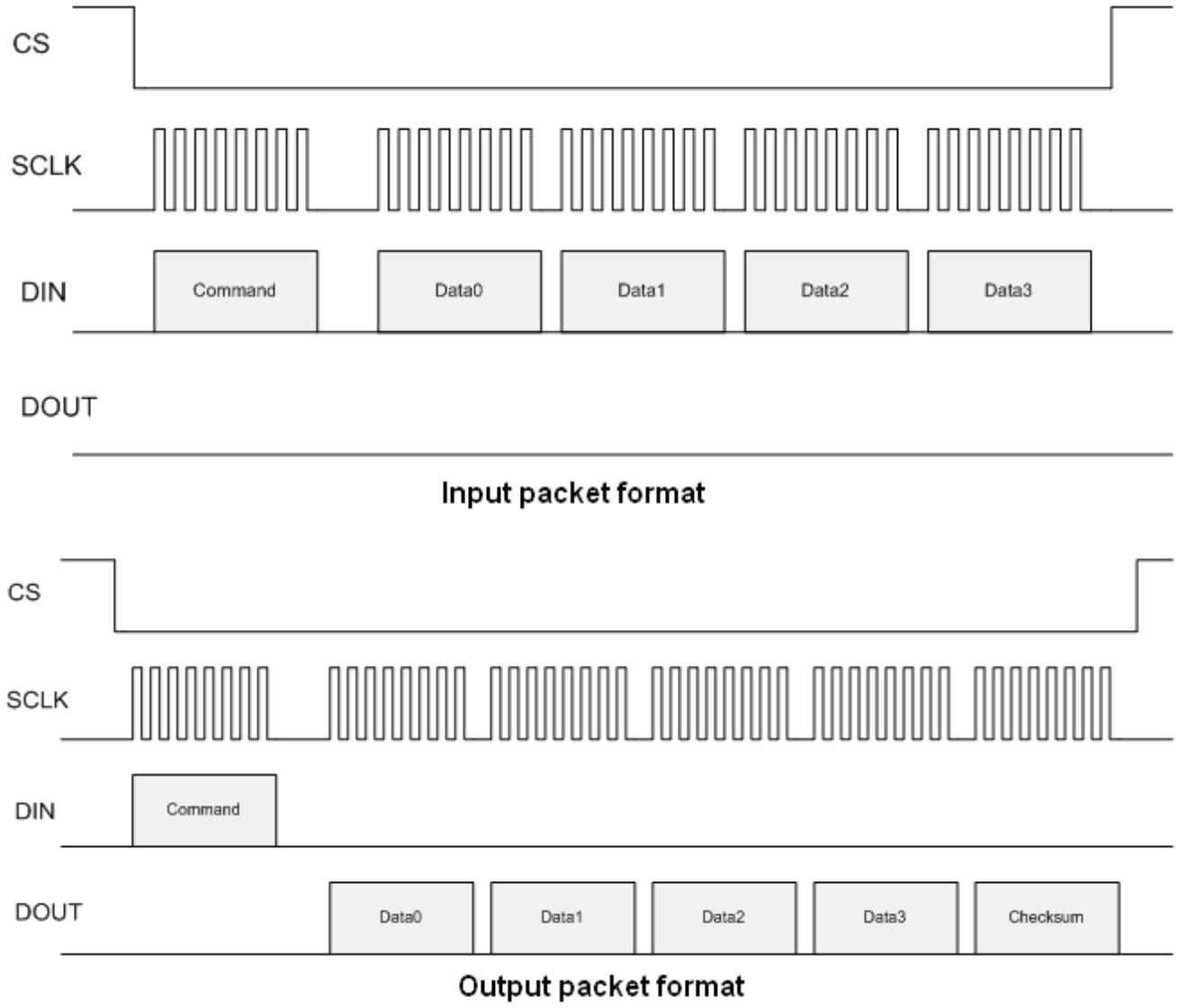

Figure 11. MSP430AFE CSG Firmware Flowchart

Detailed communication protocol and register introduction are described in Appendix B.

6 Test Specification

6.1 Terms

E-meter test facility settings:

- Ib: Basic ac current, 5 A in this test specification
- Imax: Maximum ac current, 60 A in this test specification

- Un: Nominal ac voltage, 220 V in this test specification
- E: Accuracy error in percentage, denotes the error between CSG firmware output and the reference meter

Demo meter setting

There are three signal input channels on the front-end circuit of the demo meter:

- L: Live line, feed to a shunt resistor of 300 μΩ
- N: Neutral line, feed to a transformer with n1:n2=1000:1, 10-Ωm burden resistor used
- V: An 1000:1 scaling down resister ladder used
- A0, A1, A2: 3 SD24 input channels on MSP430AFE253

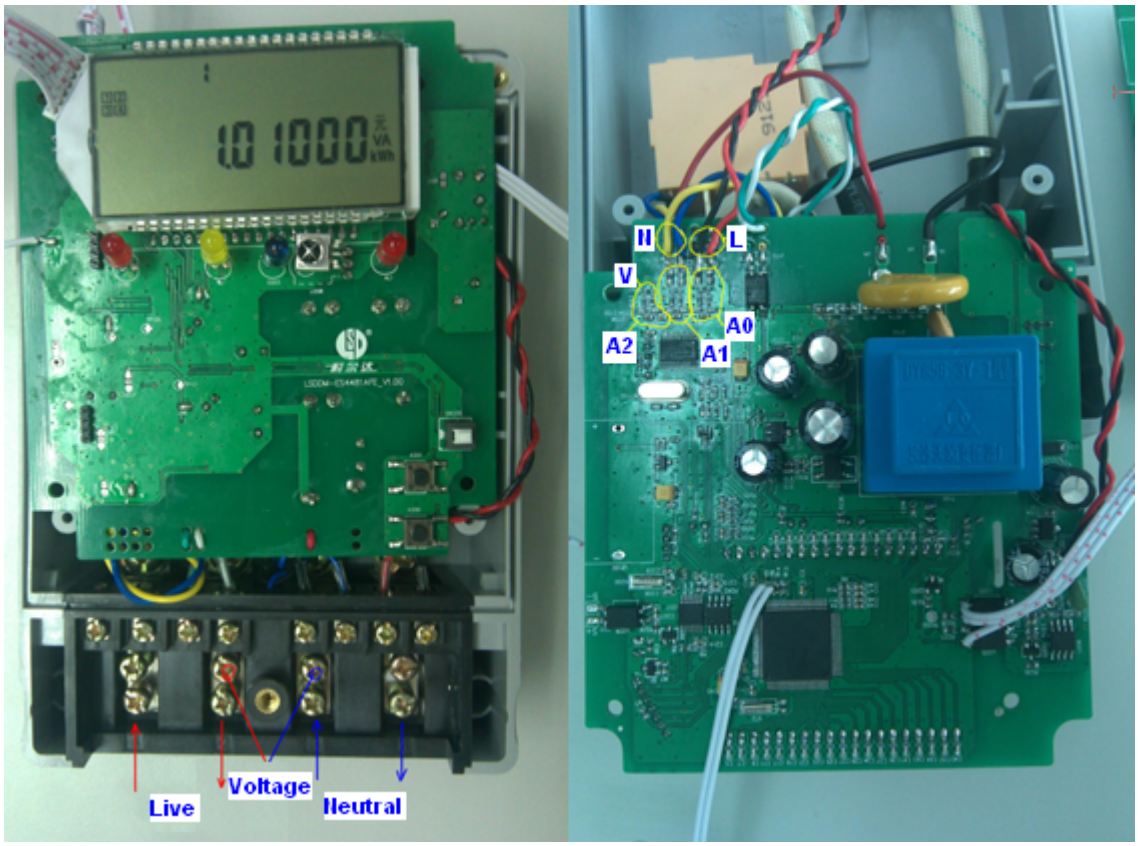

Figure 12. Demo E-Meter Connection for CSG Test

6.2 Function Test

The demo meter needs to be well calibrated before any of the following test.

6.2.1 Test Environment Setup

1. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to Live
     - Voltage to voltage

2. Connect the demo meter's active energy-pulse output pin to the reference meter so that you can determine the measurement error.
3. Assemble the demo meter on the test frame. Set the signal generator to output 100% Ib current and 100% Un voltage. The phase angle between current and voltage is 0.
4. Set the signal generator output frequency to 50 Hz.
5. Switch on the generator and reference meter.

6.2.2 Energy Pulse Enable/Disable Test

The error reading should be less than 0.2% at current setting. Then:

1. Clear the PPEN bit of the CSGCONF register and see if the active energy pulse stopped (error will not update anymore).
2. Set the phase angle between V and I to 90° in the generator and see if the error reading is less than 0.2%.
3. Clear the QPPEN bit of the CSGCONF register and see if the reactive energy pulse stopped (error will not update anymore).
4. Set the phase angle between V and I back to 0° in the generator.
5. Set the PPEN and QPEN bits of the CSGCONF register.

CSG firmware passes this test.

6.2.3 Pulse Constant and Fast Pulse Test

1. Set the POWER_CONST register of CSG firmware to 800 (default is 1600) and set the pulse constant of the generator to 800 as well, see if the error is still reading less than 0.2%.
2. Set the FPEN bit of the CSGCONF register and see if the error is still less than 0.2%.
3. Set the FPF bits of the CSGCONF register to 01, 10, 11, respectively, and set the pulse constant of the generator to 1600, 3200, 6400 accordingly; the error in every case should be less than 0.2%.
4. Reset FPEN and FPF of the CSGCONF register. Set the POWER_CONST register of the CSG firmware back to 1600 and set the pulse constant of the generator back to 1600.

CSG firmware passes this test.

6.2.4 Negative Energy Accumulation Test

1. The default value of the CSG firmware CSGCONF register EMOD bits are 00 to allow negative energy accumulation. Set the phase angle between V and I to 180° in the generator for 1 minute and see if the energy pulse stops. Read the CSG firmware STATUS register and see if the I1_REV bit is set. Read the CSG firmware EP1_ACT register and see if its value decreases gradually. Switch the phase angle back to 0° for 1 minute, then see if the energy pulse resumes and if the error is less than 0.2%.
2. Set the CSG firmware CSGCONF register EMOD bits to 01 to prohibit negative energy accumulation. Set the phase angle between V and I to 180° in the generator. The energy pulse should still stop in this case. Read the CSG firmware STATUS register and see if the I1_REV bit is set. Read the CSG firmware EP1_ACT register and see if its value is unchanging.
3. Set the CSG firmware CSGCONF register EMOD bits to 10. In this mode, negative energy is treated as positive energy as well. Set the phase angle between V and I to 180° in the generator. The energy pulse will resume in this case and see if the error reading is less than 0.2%. Read the CSG firmware STATUS register and see if the I1_REV bit is set. Read the CSG firmware EP1_ACT register and see if its value keeps increasing.
4. Set the phase angle between V and I back to 0° in the generator and see if the energy pulse stops. Set the CSG firmware CSGCONF register EMOD bits back to 00.

CSG firmware passes this test.

6.2.5 Channel Selection Test

1. CSG firmware default chooses A0 channel as the current signal input. Set the CSG firmware CSGCONF register CSEL bits to 10 to choose A1 channel as the current signal input. The energy pulse should stop in this case. Shut down the generator and feed the generator current output to the demo e-meter live input. Switch on the generator again and the energy pulse should resume. See if the error rate is less than 0.2%
2. Set the CSG firmware CSGCONF register CSEL bits to 00. In this mode, the CSG firmware automotive chooses the larger signal between I1 and I2 channels as the current signal input. Now the energy pulse should remain working. See if the error rate is less than 0.2%. Check that the CSG firmware STATUS register CH2_USED bit is set indicating the A1 channel is used for energy pulse generating.
3. Shut down generator, feed generator current output back to demo e-meter live input. Switch on generator again. Now energy pulse should remain working. See if error rate less than 0.2%. Read CSG firmware STATUS register, CH2_USED bit is reset indicating A0 channel used for energy pulse generating.
4. Set CSG firmware CSGCONF register CSEL bits back to 01.

CSG firmware passes this test.

6.2.6 ADC Gain Setting Test

1. Shut down generator.
2. Modify demo e-meter signal input in such manner:
   - Front end to MSP430AFE253
     - L to A1
     - N to A0
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Set CSG firmware SYSCONF register GGAIN1 bits to 000 (1 time gain for CT channel) and GGAIN2 bits to 100 (16 times gain for shunt channel).
4. Recalibrate e-meter.
5. Repeat Channel Selection Test (see Section 6.2.5) and see if all error tested less than 0.2%.
6. Shut down generator. Feed L signal back to CSG firmware A0 pin pair; feed N signal back to CSG firmware A1 pin pair.

CSG firmware passes this test.

6.3 Performance Test

6.3.1 Accuracy Test

1. Shut down generator.
2. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Connect demo meter's active energy pulse output pin to the reference meter.

4. Set signal generator to output 100% Un voltage. Set signal generator output frequency to 50 Hz. Test the meter on the test points shown below (the grey test points are not required). On every test point, there were three error readings from the test bench. The final result is the arithmetic average value of three readings. The final result should be less than 0.2%

	Imax	Imax/2	300%Ib	100%Ib	50%Ib	20%Ib	10%Ib	5%Ib	2%Ib
1	0.014	0.023	0.023	-0.012	0.014	0.011	-0.001	0.014	-0.059
0.5L	-0.014	-0.006	-0.006	-0.003	0.003	-0.003	-0.076	-0.02	
0.5C	0.035	-0.006	-0.006	0	0.006	0.006	0.034	-0.021	

5. Connect the signal generator's output to the demo meter in the following manner and redo step 4.
   - Front end to MSP430AFE253
     - L to A1
     - N to A0
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage

CSG firmware passes this test.

6.3.2 Voltage Influence Test

1. Shut down generator.
2. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Connect demo meter's active energy pulse output pin to the reference meter.
4. Set signal generator to output 110% Un and 90% Un voltage, respectively. Set signal generator output frequency to 50 Hz. Test the meter on the test points shown below (the grey test points are not required). On every test point, there were three error readings from test bench. The final result is the arithmetic average value of three readings. The final result should be less than 0.2%

	110%Un			90%Un		
	100%Ib	10%Ib	5%Ib	100%Ib	10%Ib	5%Ib
1	-0.021	0.006	0.008	-0.016	0.008	0.014
0.5L	-0.011	-0.105		0.008	0.126	

5. Connect the signal generator's output to the demo meter in the following manner and redo step 4.
   - Front end to MSP430AFE253
     - L to A1
     - N to A0
     - V to A2
   - Generator to demo meter
     - Current to Live
     - Voltage to Voltage

CSG firmware passes this test.

6.3.3 Frequency Influence Test

1. Shut down generator.
2. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Connect demo meter's active energy pulse output pin to the reference meter.
4. Set the signal generator to output 100% Un voltage. Set the signal generator output frequency to 51 Hz and 49 Hz, respectively. Test the meter on the test points shown below (the grey test points are not required). On every test point, three error readings are found from test bench. The final result is the arithmetic average value of the three readings. Final result should be less than 0.2%

	51Hz			49Hz		
	100%Ib	10%Ib	5%Ib	100%Ib	10%Ib	5%Ib
1	-0.012	0.004	0.014	-0.012	0.011	0.008
0.5L	-0.007	-0.056		0	-0.078	

5. Connect the signal generator's output to the demo meter in the following manner and redo step 4.
   - Front end to MSP430AFE253
     - L to A1
     - N to A0
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage

CSG firmware passes this test.

6.3.4 Harmony Influence Test

1. Shut down generator.
2. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Connect the demo meter's active energy pulse output pin to the reference meter.
4. Set the signal generator to output 100% Un voltage and 0.5 Imax current. Set the signal generator output frequency to 50 Hz. Feed 10% Un 5th harmony on voltage and 40% Ib 5th harmony on current. Harmony power factor is set to 1.

CSG firmware passes this test.

6.4 Rubust Test

6.4.1 Communication Test

6.4.1.1 Setting

Connect front-end output to MSP430AFE253 in the following manner:

- Front end to MSP430AFE253
  - L to A0
  - N to A1
  - V to A2
- Generator to demo meter
  - Current to live
  - Voltage to voltage

Connect the demo meter's active energy pulse output pin to the reference meter.

6.4.1.2 Corrupted Data Test

Host MCU MSP430F4481 send package is shown in Figure 13.

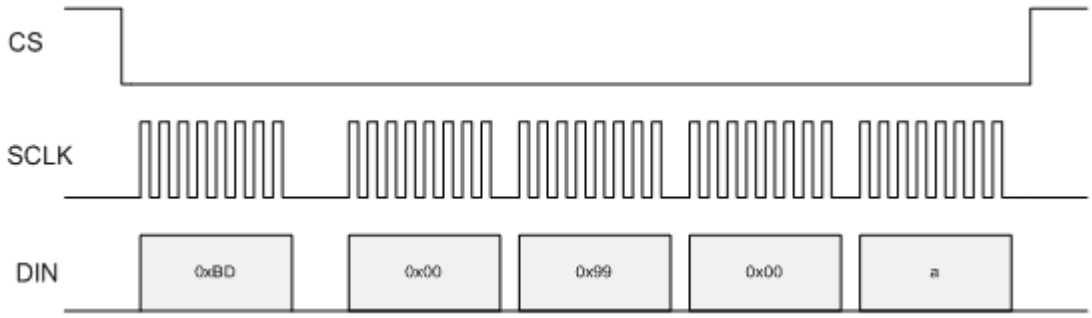

Figure 13. Corrupted Data Through SPI

In this package, the command area (1st byte) always contains 0xBD, which denotes this is a software reset command. In a valid software reset command packet, the data area (from 2nd byte to 5th byte) should contain 0x00990099. For the sake of checking AFE's response to a packet containing invalid data, send 0xBD, 0x00, 0x99, 0x00 on the 1st, 2nd, 3rd and 4th byte, respectively, but on the 5th byte (marked as variable a on Figure 13) send a number not equal to 0x99 to form an invalid packet.

The invalid package is sent for 255 times. Every time the value of the 5th byte adds one comparing to the 5th byte of the last package that is sent, but never equal to 0x99. In this way, you are able to check AFE's response to different invalid packages. The time gap between two packages is 10 ms. CSG firmware should indentify the invalid package and keep running in measurement mode. See if CSG firmware reset or other unexpected function is triggered.

CSG firmware passes this test.

6.4.1.3 Corrupted Clock Test

- The Host MCU MSP430F4481 send package is shown in Figure 14. An illegal clock is inserted between command and data. Keep sending this package 10 times. The time gap between two packages is 10 ms. CSG firmware should keep running in measurement mode. See if CSG firmware gets reset or any unexpected function is triggered.

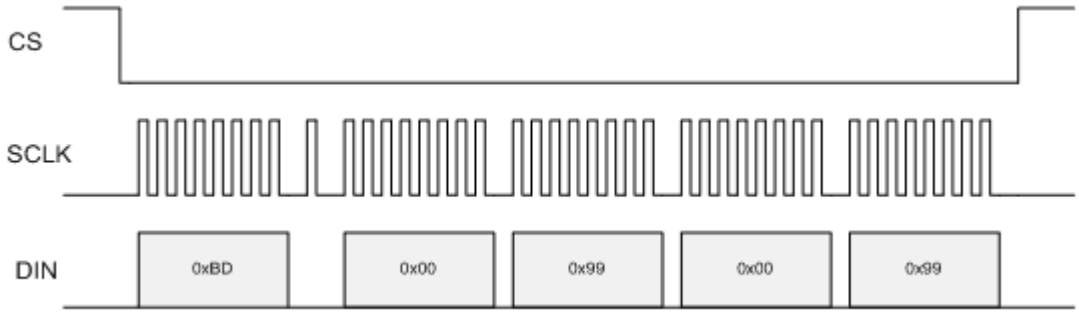

Figure 14. Corrupted Clock - Additional Clock

- Host MCU MSP430F4481 send package is shown in Figure 15. One clock for first data is missing. Keep sending this package 10 times. The time gap between the two packages is 10 ms. CSG firmware should keep running in measurement mode. See if CSG firmware gets reset or if any unexpected function is triggered.

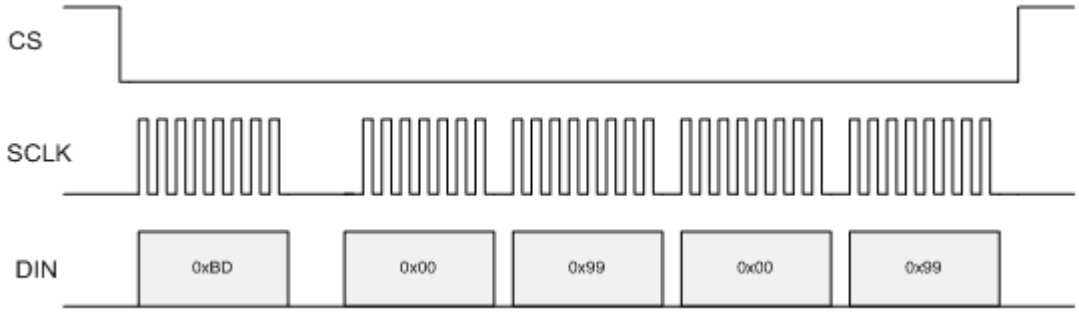

Figure 15. Corrupted Clock - Missed Clock

CSG firmware passes these two tests.

6.4.1.4 Random Noise Test

Program MSP430F4481 to output-random sequence on SPI interface, then check to see if meter accuracy is influenced.

CSG firmware passes this test.

6.4.2 Zero Load Test

1. Shut down generator.
2. Connect front-end output to MSP430AFE253 in the following manner:
   - Front end to MSP430AFE253
     - L to A0
     - N to A1
     - V to A2
   - Generator to demo meter
     - Current to live
     - Voltage to voltage
3. Connect the demo meter's active energy pulse output pin to the reference meter.
4. Set the signal generator to output 100% voltage and 0A current. Set output frequency to 50 Hz.
5. Switch on the generator for 1 minute and see if unexpected energy pulse is generated, then shut down the generator. Repeat this test 20 times.

CSG firmware passes this test.

6.4.3 Power Sequence Test

1. Power up MSP430F4481 first. Wait 10 seconds and slowly power up MSP430AFE253, as shown in Figure 16. See if MSP430AFE253 is dead.

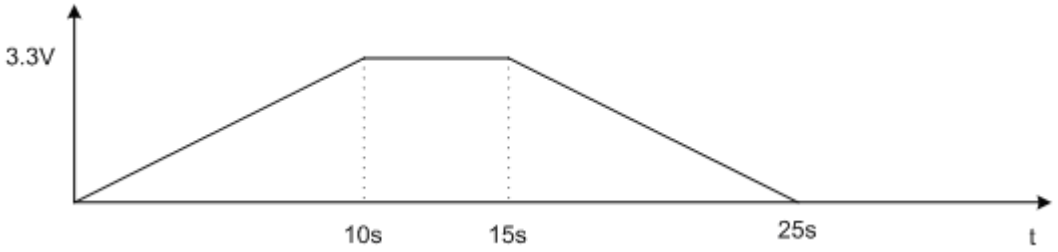

Figure 16. Power-On Sequence

2. Power up MSP430F4481 first. Program MSP430F4481 to keep sending packages on SPI interface. Then power up MSP430AFE253.
3. Keep MSP430F4481 running as step 2). Then power down MSP430AFE253.
4. Repeat step 2) and 3) 10 times.

CSG firmware passes this test.

7 References

- *MSP430x2xx Family User's Guide* (SLAU144)
- *MSP430AFE2x3, MSP430AFE2x2, MSP430AFE2x1 Mixed Signal Microcontroller Data Sheet* (SLAS701)

Appendix A MSP430F4481 Communication Protocol

A.1 Communication Protocol

Communication between GUI and F4481 follows DL/T645 protocol, which is widely used in China's current automatically metered reading system.

DL/T645 protocol defined packet format as shown below:

F_start	Address						F_start	C_code	Length	Packet_body			CS	End
0	1	2	3	4	5	6	7	8	9	len of bytes			len+10	len+11
0x68	0x99	0x99	0x99	0x99	0x99	0x99	0x68	0x23	len	H_CMD	nR/W	Data	sum	0x16

- F_start: Frame start notification, always be 0x68
- Address: Device address, 0x999999999999 denote broadcasting address
- C_code: Customer defined message type. 0x23 denote the message type for TI demo e-meter
- Length: Packet body length, in bytes
- Packet_body: Contain message body
- CS: Checksum, it equates to algorithm sum from 0 to len+9 in the frame
- End: Frame end notification, always 0x16

There is detailed description on frame format in《DL/T645—2007 Multi-function watt-hour meter communication protocol. In this report, the focus is on Packet_body part, which was used to contain GUI requests packet and F4481 feedback packet.

A.2 GUI Request Format

GUI request packet and F4481 feedback packets have similar format, which is composed of three parts:

- H_CMD: GUI command, 1 byte
- nR/W: Notify command direction, 1 byte. 0x80 denotes a command from GUI to F4481, 0x00 denotes F4481 feedback to GUI
- Data: Command parameters. Its length depends on which command is issued.

The command sets and corresponding parameters are:

- HOST_CMD_GET_READINGS_PHASE_1 = 0x61,
- HOST_CMD_GET_READINGS_NEUTRAL = 0x64,
- HOST_CMD_GET_CSG_REGISTER = 0x65,
- HOST_CMD_GET_CSG_CALIBRATION = 0x66,
- HOST_CMD_SET_CSG_CALIBRATION = 0x67,
- HOST_CMD_SET_CSG_REGISTER = 0x68,
- HOST_CMD_SET_CSG_SOFTRESET = 0x69,

A.2.1 GUI Read Out Metering Parameters

GUI to F4481

Index	0	1
value	0x61/0x64	0x00

F4481 to GUI

Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
value	0x61/0x64	0x80	Vrms		Irms		ActPowerH		ActPowerL		RctPowerL		RctPowerL		AppPowerH	

Index	16	17	18	19	20	21	22	23	24	25	26	27	28	29
value	AppPowerL		PF		F		V_dcH		V_dcL		I_dcH		I_dcL	

This command reads out all CSG parameter registers except active and reactive energy pulse counter registers. For more information of CSG firmware parameter registers, see Section B.2.

A.2.2 GUI Get CSG Firmware Register Value

GUI to F4481

Index	0	1
value	0x65	0x00

F4481 to GUI

Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
value	0x65	0x80	sysconf		afeconf		power const		start current		IE		status		checksum1		meter status	

This command reads out all CSG system registers. For more information of CSG firmware system registers, see Section B.2.2.

A.2.3 GUI Set CSG Firmware Register Value

GUI to F4481

Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13
value	0x68	0x00	sysconf		afeconf		power const		start current		IE		checksum	

F4481 to GUI

Index	0	1
value	0x68	0x80

This command updates all CSG system registers. For more information of CSG firmware system registers, see Section B.2.

A.2.4 GUI Get CSG Firmware Calibration Factors

GUI to F4481

Index	0	1
value	0x66	0x00

F4481 to GUI

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0x66	0x80	COffset0		CGain0		PGain0		PPhase0		POffset0		QOffset0		COffset1		CGain1	

18	19	20	21	22	23	24	25	26	27
PGain1		PPhase1		POffset1		QOffset1		VGain	

This command reads out all CSG calibration registers. For more information of CSG firmware calibration registers, see Section B.2.4.

A.2.5 GUI Set CSG Firmware Calibration Factors

GUI to F4481

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
0x67	0x00	COffset0		CGain0		PGain0		PPhase0		POffset0		QOffset0		COffset1		CGain1	

value	18	19	20	21	22	23	24	25	26	27	28	29
value	PGain1		PPhase1		POffset1		QOffset1		VGain		checksum	

F4481 to GUI

Index	0	1
value	0x67	0x80

This command updates all CSG calibration registers. For more information of CSG firmware calibration registers, see Section B.2.4.

Appendix B CSG Firmware Access and Operation

B.1 CSG Firmware Access and Operation

CSG firmware performs metering calculation independently of the host MCU. It can be accessed by the host MCU through SPI interface. The host MCU can read and set CSG registers to set the firmware working mode, to read energy metering parameters and to calibrate the meter.

B.1.1 SPI Interface

CSG firmware supports self-adaptable 3-wire or 4-wire SPI interface. Four pins are used: CS(4-wire only), SCLK, DIN, and DOUT. CSG firmware polls the CS pin approximately 2 ms after MSP430AFE253 start up. If CS pin is high, CSG firmware sets SPI to 4-wire mode; otherwise, firmware sets SPI to 3-wire mode.

Figure 17 shows SPI timing in working mode:

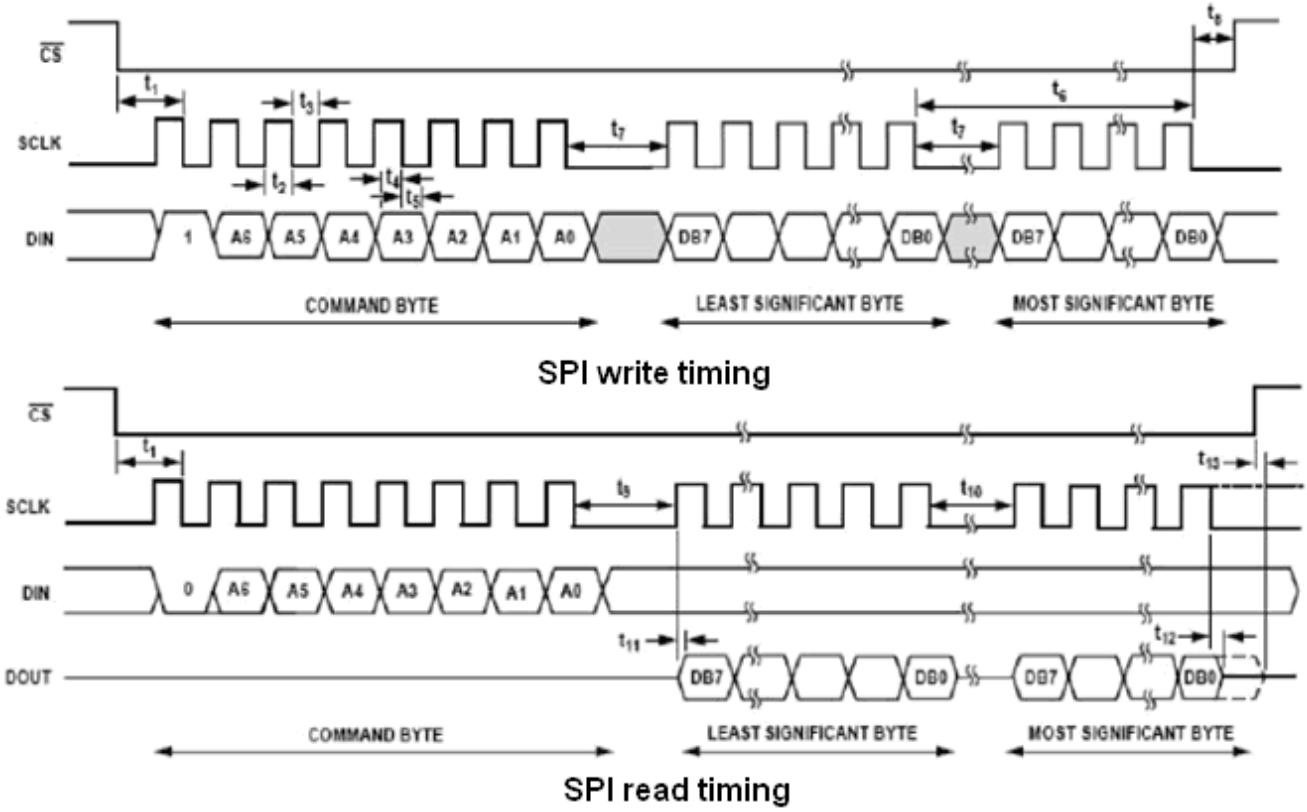

Figure 17. SPI Timing

B.1.2 CSG Firmware Communication Package

CSG firmware communication packet is composed of command, data, and checksum area. Input packet and output packet are defined as Figure 18 shows:

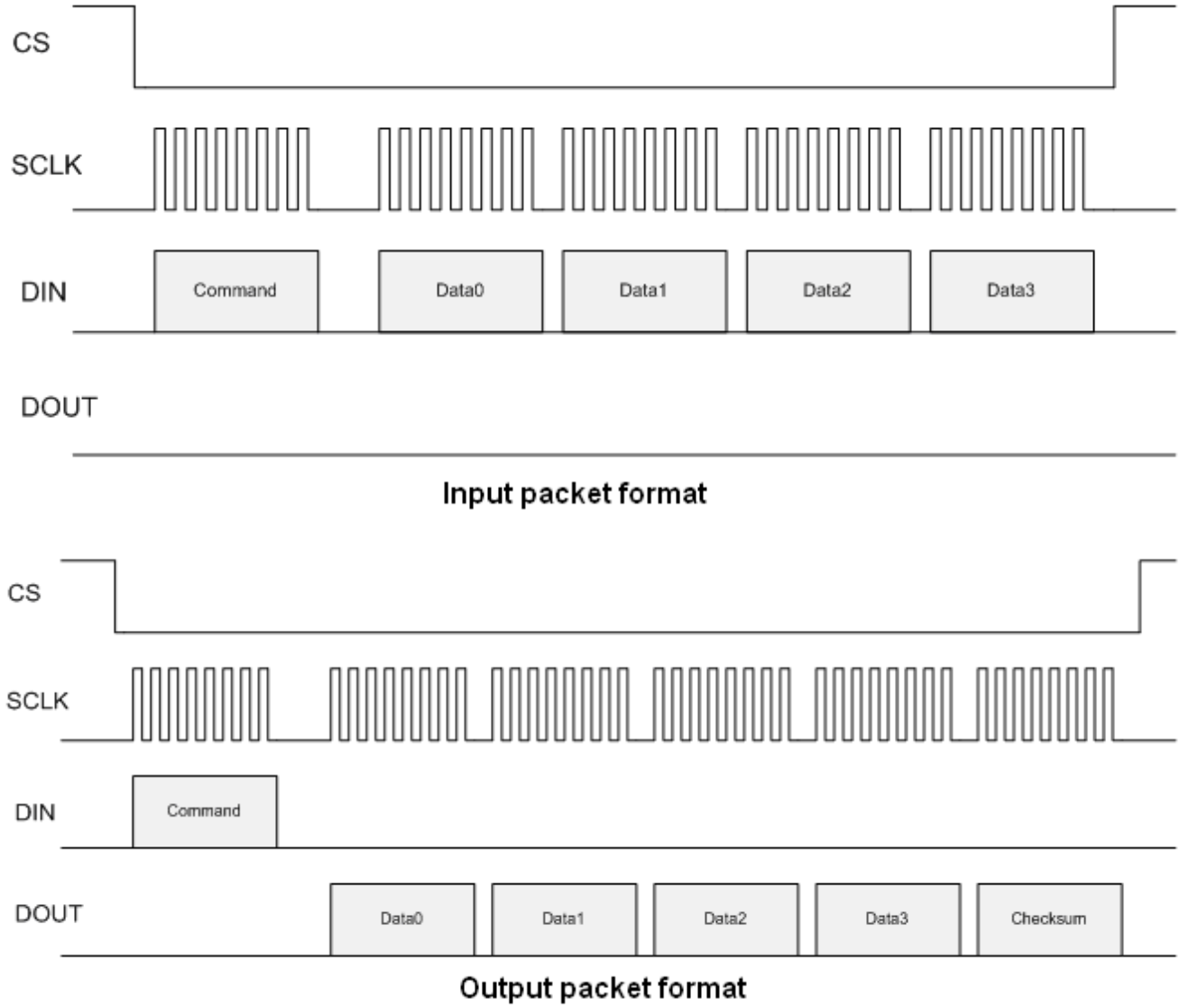

Figure 18. CSG Firmware Communication Packet

All SPI transmitting and receiving are done in 8-bit format.

Command has the following format:

- Bit7, Bit6: 01 host read command
- Bit7, Bit6: 10 host write command
- Bit5 to Bit0: register address

The date area is in double words format in both the input and output packet. For those 16-bit registers access, higher word and lower word of the data area in communication packets should be the same content.

The checksum area is only used in the output packet. It contains the sum of command and all 4 bytes data. For example, if host MCU wants to read channel 1 active power, it can send command 0x60 to MSP430AFE253, in which 0x40 denotes a read command and 0x20 is the address of channel 1 active power register in CSG firmware.

If the current active power reading is 2200 W, MSP430AFE253 sends a packet of 5 bytes back: 0x60, 0x5B, 0x03, 0x00, 0xBE; where, 0x00035B60 denotes 220000 in 10-mW step and 0xBE is the check sum of all previous 4 bytes. The host MCU can choose to read checksum or omit it.

B.1.3 SPI Timing

Parameter	description	min	max	unit
write				
t1	CS failing edge to SCLK failing edge	20		us
t2	Width of SCLK high	500		ns
t3	Width of SCLK low	500		ns
t4	Data hold time	250		ns
t5	Data setup time	200		ns
t6	Byte time	30		us
t7	Interval between data bytes	20		us
t8	CS hold time after SCLK failing edge	3	3	us
read				
t9	Interval between read command and data	40		us
t10	Interval between data bytes	20		us
t13	Data bus release time after CS leading edge	3		us
packet				
	Interval between packet	1		ms

B.2 Firmware Registers

B.2.1 Register Arrangement

MSP430AFE2xx CSG firmware provides three groups for register: system, parameter, and calibration register.

Calibration register:

address	Name	R/W	Length(Byte)	Default	discription
0x00	I1RMS_OFFSET	R&W	2	0	Channel1 IRMS offset
0x01	I2RMS_OFFSET	R&W	2	0	Channel2 IRMS offset
0x02	I1RMS_GAIN	R&W	2	last writen	Channel1 IRMS slope
0x03	I2RMS_GAIN	R&W	2	last writen	Channel2 IRMS slope
0x04	P1_GAIN	R&W	2	last writen	Channel1 active power slope
0x05	P2_GAIN	R&W	2	last writen	Channel2 active power slope
0x06	P1_PHASE	R&W	2	0	Channel1 phase shift
0x07	P2_PHASE	R&W	2	0	Channel2 phase shift
0x08	P1_OFFSET	R&W	2	0	Channel1 active power offset
0x09	P2_OFFSET	R&W	2	0	Channel2 active power offset
0x0A	Q1_OFFSET	R&W	2	0	Channel1 reactive power offset
0x0B	Q2_OFFSET	R&W	2	0	Channel2 reactive power offset
0x0C	VRMS_FACTOR	R&W	2	0	Voltage RMS slope

Parameter register:

address	Name	R/W	Length(Byte)	Default	discription
0x20	P1_ACT	R	4	0x0000	Channel1 active power
0x21	P2_ACT	R	4	0x0000	Channel2 active power
0x22	P1_REACT	R	4	0x0000	Channel1 reactive power
0x23	P2_REACT	R	4	0x0000	Channel2 reactive power
0x24	P1_APP	R	4	0x0000	Channel1 apparent power
0x25	P2_APP	R	4	0x0000	Channel2 apparent power
0x26	VRMS	R	2	0x0000	VRMS
0x27	FREQ	R	2	0x0000	Line Frequency
0x28	I1RMS	R	2	0x0000	Channel1 IRMS
0x29	I2RMS	R	2	0x0000	Channel2 IRMS
0x2A	PF1	R	2	0x0000	Channel1 power factor
0x2B	PF2	R	2	0x0000	Channel2 power factor
0x2C	EP_ACT	R	2	0x0000	active energy pulse counter
0x2D	EP_RACT	R	2	0x0000	reactive energy pulse counter
0x2E	EP_NEG_ACT	R	2	0x0000	negtive active energy pulse counter
0x2F	EP_NEG_RACT	R	2	0x0000	negtivereactive energy pulse counter

System register:

address	Name	R/W	Length(Byte)	Default	discription
0x34	SYSCONF	R&W	2	0x0004	system config register
0x35	CSGCONF	R&W	2	0x1063	CSG function config register
0x36	POWER_CONST	R&W	2	0x0640	power constant
0x37	START_CURRENT	R&W	2	0x00DC	Start power threshold
0x38	IE	R&W	2	0x0001	CSG interrupt enable
0x39	IFG	R	2	0x0000	CSG interrupt flag
0x3A	STATUS	R	2	0x0000	CSG status
0x3B	CheckSum1	R	2	0x0000	checksum for calibration registers
0x3C	WREN	R&W	2	0x0000	write enable
0x3D	SRST	W	2	--	software rest
0x3E	USI_RX	R	2	0x0000	Last SPI received value
0x3F	USI_TX	R	2	0x0000	Last SPI transmitted value

B.2.2 System Registers

System register is used to configure MSP430AFE2xx CSG firmware functions.

B.2.2.1 ADC Gain Setting

MSP430AFE2xx integrated thee independent SD24 modules, each of them has a PGA with up to 32 times gain options. CSG firmware allows you to choose different gain for every channel. The gain control is implemented through SYSCONF register

SD24 Gain setting	value	Gain	Input	unit
GAINV/GAINI1/GAINI2	000	1	±500	mVp-p
	001	2	±250	mVp-p
	010	4	±125	mVp-p
	011	8	±62	mVp-p
	100	16	±31	mVp-p
	101	32	±15	mVp-p

GAINI1, GAINI2, and GAINV denote the gain setting for channel 1, 2, and 3, respectively. They are in SYSCONF register from BIT0 to BIT8.

	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYSCONF	**RSV**	**RSV**	**RSV**	**RSV**	**RSV**	**RSV**	**RSV**	**GAINV**			**GAINI2**			**GAINI1**		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

RSV denotes reserved for future usage.

B.2.2.2 CSG Function Register

CSG function register configure CSG firmware functions.

	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
CSGCONF	**SOFF**	**QOFF**	**CSEL**		**EMOD**		**RSV**	**RSV**
default	0	0	0	1	0	0	0	0

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CSGCONF	**RSV**	**DCFILTER**		**FPEN**	**FPF**		**QPEN**	**PPEN**
default	0	0	0	0	0	0	1	1

SOFF—

1: switch off apparent power measurement. Apparent power always read 0

0: switch on apparent power measurement

QOFF—

1: switch off reactive power measurement. Apparent power always read 0

0: switch on reactive power measurement

CSEL— energy pulse selection

00: energy pulse generate from large current channel

01: energy pulse generate from channel 1

10: energy pulse generate from channel 2

EMOD— negative energy accumulate mode

00: accumulate negative energy ,

01: do not accumulate negative energy, if P<0,P=0

10: accumulate absolute value for negative energy, if P<0,P=-P

DCFILTER— DC filter selection

00: IIR filter on V channel, no filter for I channel

01: IIR filter for both V and I channel

10: average filter on V channel, no filter for I channel

11: average filter for both V and I channel

FPEN—

1: fast energy pulse enable

0: fast energy pulse disable

FPF— Fast pulse ratio. When FPEN is set, FPF decide the ratio between fast energy pulse and normal energy pulse

00:×1

01:×2

10:×4

11:×8

QPEN—

1: enable reactive energy pulse

0: disable reactive energy pulse

PPEN—

1: enable active energy pulse

0: enable active energy pulse

B.2.2.3 Power Constant

POWER_CONST register contains the number of energy pulse for 1-kWh energy. Its default value is 1600.

B.2.2.4 Start Energy

START_CURRENT register contains the threshold below which CSG firmware stops accumulate energy. It is in 10-mW steps, and the default value of 220 denotes 2.2 W.

B.2.2.5 Event and Interrupt

CSG firmware has seven event sources.

IE		WFS	ZX	QEO	PEO	QF	PF	NEWLOG
default	0	0	0	0	0	0	0	1
IFG		WFS	ZX	QEO	PEO	QF	PF	NEWLOG
default	0	0	0	0	0	0	0	0

WFS— waveform sample event is triggered every time SD24 sample ready.

ZX— cross zero event is triggered on the leading zero cross point on voltage.

QEO— reactive energy pulse overflow event is triggered every 65536 reactive energy pulses.

PEO— active energy pulse overflow event is triggered every 65536 active energy pulses.

QF— reactive energy pulse event is triggered every reactive energy pulse

PF— active energy pulse event is triggered every active energy pulse

NEWLOG— parameter register update event is triggered when parameter registers are updated by CSG firmware. It indicate the right time to read out parameter registers

Every event source has a corresponding enable mask in the IE register and a flag in the IFG register. Set mask in the IE register enables interrupt for that event. If one event is triggered and the corresponding IE mask set, CSG firmware sends out an interrupt on pin P1.1.

The event flag is always set when the corresponding event is triggered, no matter whether the corresponding IE bit is set or not. The flag remains set unless the IFG register is read by the host through SPI. The read IFG register will reset all flags.

Note: The frequency of the WFS (nominal 4 kHz) and ZX (nominal 50 Hz) events is very fast; make sure the host MCU has enough bandwidth to process them before you set those events in IE.

B.2.2.6 CSG Status

STATUS contains CSG firmware status; it is a read-only register.

	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
STATUS	**RSV**	**RSV**	**UNBAL**	**M_REV**	**RSV**	**RSV**	**CH2_USED**	**I2_REV**
default	0	0	0	0	0	0	0	0
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STATUS	**I2_OR**	**I1_REV**	**I1_OR**	**V_OR**	**EOF**	**I2POS**	**I1POS**	**VPOS**
default	0	0	0	0	0	0	0	0

UNBAL—

1: current unbalance between neutral and live

0: current balance between neutral and live

The threshold of unbalance is: If absolute active power is larger than 2000 W, 6.25% error between neutral and live If absolute active power is less than 2000 W, 25% error between neutral and live

M_REV—

1: current reversed (either live or neutral)

0: current not reversed

CH2_USED—

1: Channel 2 used to generate energy pulse

0: Channel 1 used to generate energy pulse

I2_REV—

1: Channel 2 reversed

0: Channel 2 not reversed

I2_OR—

1: Channel 2 over range

0: Channel 2 in range

I1_REV—

1: Channel 12 reversed

0: Channel 12 not reversed

I1_OR—

1: Channel 1 over range

0: Channel 1 in range

V_OR—

1: Channel V over range

0: Channel V in range

EOF—

1: Active energy pulse counter reach 65536 and reset

0: Active energy pulse counter does not reach 65536

I2POS—

1: Channel 2 on positive half

0: Channel 2 on negative half

I1POS—

1: Channel 1 on positive half

0: Channel 1 on negative half

VPOS—

1: Channel V on positive half

0: Channel V on negative half

B.2.2.7 Check Sum

The CheckSum1 register contains the checksum for all calibration registers at addresses 0x00 to 0x0C. CheckSum1 is updated by CSG firmware every time the calibration registers is modified by the host.

B.2.2.8 Write Enable

System registers at addresses 0x34 to 0x38 and all calibration registers are write protected and cannot be modified until a special code is written to the WREN register.

- Write 0x00CA to the WREN register to enable writing to the calibration registers.
- Write 0xC500 to the WREN register to enable writing to the system registers.
- Write 0xC5CA to enable writing to both the system and calibration registers.
- Write any value other than 0x00CA, 0xC500, or 0xC5CA to the WREN register to disable writing to the system and calibration registers.

NOTE: Each write to the system or calibration registers clears the corresponding write enable in the WREN register.

B.2.2.9 Software Reset

Writing 0x0099 to the SRST register will reset MSP430AFE2xx CSG firmware.

B.2.2.10 SPI Data Buffer

USI_RX and USI_TX registers store the last received data and transmitted date from SPI, respectively.

B.2.3 Metering Parameters

B.2.3.1 Active Power

The calculated active energy for the last 4096 ADC measurements (1 second) is stored in Px_ACT, where x = 1 or 2 for I1 and I2, respectively. The active power calculation formula is shown Equation 1.

$$Px\_ACT = KPx(\frac{1}{N}\sum_{k=1}^{N} v(k) \times i(k)) - Px_{offset}[10mW] \quad (1)$$

- N=4096
- KPx is the slope value for power, which is stored in the Px_GAIN calibration register.
- Px_{offset} is the active power offset, which is stored in the Px_OFFSET calibration register.
- Px_ACT is in 10-mW steps.
- The addresses of P1_ACT and P2_ACT are 0x20 and 0x21.

register	address	resolution	format	Range	step
P1_ACT	0x20	32bit signed	31.0	0x80000000~0x7FFFFFFF	10mW
P2_ACT	0x21	32bit signed	31.0	0x80000000~0x7FFFFFFF	10mW

B.2.3.2 Reactive Power

The calculated reactive energy for the last 4096 ADC measurements (1 second) is stored in Px_REACT, where x = 1 or 2 for I1 and I2, respectively. The reactive power calculation formula is shown in Equation 2:

$$Px\_REACT = KPx(\frac{1}{N}\sum_{k=1}^{N} v(k)_{\angle -\frac{\pi}{2}} \times i(k)) - Qx_{Xoffset}[10mW] \quad (2)$$

- N=4096
- KPx is the slope value for power, which is stored in the Px_GAIN calibration register.
- Qx_{offset} is the reactive power offset, which is stored in the Qx_OFFSET calibration register.
- Px_REACT is in 10-mW steps.
- The address of P1_REACT and P2_REACT are 0x22 and 0x23.

register	address	resolution	format	Range	Step
P1_REACT	0x22	32bit signed	31.0	0x80000000~0x7FFFFFFF	10mW
P2_REACT	0x23	32bit signed	31.0	0x80000000~0x7FFFFFFF	10mW

B.2.3.3 Apparent Power

The apparent power calculation formula is shown in Equation 3:

$$Px\_APP = \sqrt{P_X\_ACT^2 + P_X\_REACT^2}[10mW] \quad (3)$$

- Px_APP is in 10-mW steps.
- The addresses of P1_APP and P2_APP are 0x24 and 0x25.

register	address	resolution	format	Range	Step
P1_APP	0x24	32bit signed	31.0	0x00000000~0x7FFFFFFF	10mW
P2_APP	0x25	32bit signed	31.0	0x00000000~0x7FFFFFFF	10mW

B.2.3.4 Power Factor

The power factor calculation formula is shown in Equation 4:

$$\cos\varphi = sign(P) \times \frac{abs(P)}{abs(S)} \tag{4}$$

- The address of PF1 and PF2 are 0x2A and 0x2B.

register	address	resolution	format	range	Step
PF1	0x2A	16bit signed	15.0	0x8000~0x7FFF	NA
PF2	0x2B	16bit signed	15.0	0x8000~0x7FFF	NA

B.2.3.5 IRMS

The IRMS calculation formula is shown in Equation 5:

$$IxRMS = KIx \times \sqrt{\frac{1}{N}\sum_{k=1}^{N} i(k)^2} - Ix_{offset}[1mA] \tag{5}$$

- N=4096
- KIx is the slope value for current, which is stored in the IxRMS_GAIN calibration register.
- Ix_{offset} is the current offset, which is stored in the IxRMS_OFFSET calibration register.
- IxRMS is in 1-mA steps.
- The addresses of I1RMS and I2RMS are 0x28 and 0x29.

register	address	resolution	format	Range	step
I1RMS	0x28	32bit unsigned	32.0	0x00000000~0xFFFFFFFF	1mA
I2RMS	0x29	32bit unsigned	32.0	0x00000000~0xFFFFFFFF	1mA

B.2.3.6 VRMS

The VRMS calculation formula is shown in Equation 6:

$$V\_RMS = KV \times \sqrt{\frac{1}{N}\sum_{k=1}^{N} v(k)^2}[10mV] \tag{6}$$

- N=4096
- KVx is the slope value for voltage, which is stored in the VRMS_GAIN calibration register.
- VRMS is in 1-mV steps.
- The address of VRMS is 0x26.

register	address	resolution	format	range	step
VRMS	0x26	16bit unsigned	16.0	0~0xFFFF	10mV

B.2.3.7 Frequency

- Frequency is stored in 0x27.

register	address	resolution	format	range	step
FREQ	0x27	16bit unsigned	16.0	0~0xFFFF	0.001Hz

B.2.3.8 Energy Counter

CSG firmware provides four registers to store energy:

- EP_ACT: counter for positive active energy pulse
- EP_REACT: counter for positive reactive energy pulse
- EP_NEG_ACT: counter for negative active energy pulse
- EP_NEG_REACT: counter for negative reactive energy pulse

All energy counters overflow after reaching 65536.

register	address	resolution	format	range	step
EP_ACT	0x2C	16bit unsigned	16.0	0~0xFFFF	1 pulse
EP_REACT	0x2D	16bit unsigned	16.0	0~0xFFFF	1 pulse
EP_NEG_ACT	0x2C	16bit unsigned	16.0	0~0xFFFF	1 pulse
EP_NEG_REACT	0x2D	16bit unsigned	16.0	0~0xFFFF	1 pulse

B.2.4 Meter Calibration

B.2.4.1 Calibration Registers

B.2.4.1.1 Power Slope

register	address	resolution	range	Normal range	initiation	step
P1_GAIN	0x04	16bit signed	0~0x7FFF	0x1000~0x7000	0x3000	NA
P2_GAIN	0x05	16bit signed	0~0x7FFF	0x1000~0x7000	0x3000	NA

B.2.4.1.2 Phase Shift

register	address	resolution	range	Normal range	initiation	Step
P1_PHASE	0x04	16bit signed	0x8000~0x7FFF	0xFF8C~0x01D2	0	PRELOAD
P2_PHASE	0x05	16bit signed	0x8000~0x7FFF	0xFF8C~0x01D2	0	PRELOAD

B.2.4.1.3 Active Power Offset

register	address	resolution	range	Normal range	initiation	Step
P1_OFFSET	0x08	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	10mW
P2_OFFSET	0x09	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	10mW

B.2.4.1.4 Reactive Power Offset

register	address	resolution	range	Normal range	initiation	Step
Q1_OFFSET	0x0A	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	10mW
Q2_OFFSET	0x0B	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	10mW

B.2.4.1.5 Current Slope

register	address	resolution	range	Normal range	initiation	Step
I1RMS_GAIN	0x02	16bit signed	0~0x7FFF	0x1000~0x7000	0x2000	NA
I2RMS_GIAN	0x03	16bit signed	0~0x7FFF	0x1000~0x7000	0x2000	NA

B.2.4.1.6 Current AC Offset

register	address	resolution	range	Normal range	initiation	Step
I1RMS _OFFSET	0x00	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	1mA
I2RMS _OFFSET	0x01	16bit signed	0x8000~0x7FFF	0xFF9C~0x064	0	1mA

B.2.4.1.7 Voltage Slope

register	address	resolution	range	Normal range	initiation	step
VRMS_FACTOR	0x0C	16bit signed	0~0x7FFF	0x1000~0x7000	0x4000	NA

B.2.4.2 Calibration Approach

Calibration is done by modifying the calibration registers. A simple way to calibrate the demo meter is by calculating metering errors with the approaches described in the following sections and updating those errors to the demo e-meter through the GUI, which was introduced in Section 3. Another way is writing those errors directly to AFE253 firmware through communication between the host MCU and AFE253.

B.2.4.2.1 Slope and Offset Calibration

Single-point and dual-point meter calibration are possible using the MSP430AFE2xx CSG firmware. When single point calibration is used, the slope (P1_GAIN and P2_GAIN) is calibrated. When dual-point calibration is required, the offset is calculated in addition to the slope (P1_OFFSET and P1_OFFSET are used for active power, and (Q1_OFFSET and Q1_OFFSET are used for reactive power).

The calibration sequence for active power is (repeat for two-point calibration):

1. Configure system registers, select right ADC gain for voltage and current, chose right channel to output energy pulse
2. Set Px_OFFSET to 0, if it is modified by customer code. Read out Px_GAIN value before you modify it and recode it as Px_GAINn.
3. Set power factor to unity, read active power measurement errors E_H and E_L on two test points: 100% Ib and 5% Ib.
4. Calculate the new Px_GAIN_{n+1} according to Equation 7. Here, N_{H2L} denotes the rate between the large current and small current. N_{H2L}=100%Ib / 5%Ib = 20

$$Px\_GAIN_{n+1} = \frac{Px\_GAIN_n \times (N_{H2L} - 1)}{N_{H2L} \times (1 + E_H) - (1 + E_L)} \quad (7)$$

5. Calculate Px_OFFSET_{n+1} according to Equation 8. Here, N_{H2L} denotes the rate between the large and small current. P_{GEN} denotes the genuine active power sourced from the generator in small current points.

$$Px\_OFFSET_{n+1} = \frac{(E_H - E_L) \times N_{H2L} \times P_{GEN} \times 100}{N_{H2L} \times (1 + E_H) - (1 + E_L)} \quad (8)$$

6. Update new Px_GAIN and new Px_OFFSET to MSP430AFE253 through SPI interface.

The calibration sequence for reactive power is similar to active power calibration. Note: reactive power and active power share the same slope parameter. If active power is already calibrated, reactive power calibration should start from step 5.

For example, if single point calibration is used and E_H = 0.5%, original P1_GAIN$_n$ = 10000. Then the new P1_GAIN$_{n+1}$ =10000/(1+0.5%)=9950. To calibrate the CSG firmware, you can use either way

- Use GUI: Type 0.5 on the Active Gain edit box, and press the Update Calibration button on the meter configuration window.
- Send the calibration command to AFE253 to modify the P1_GAIN register to 9950 with packet: 0x84DE26DE26

B.2.4.2.2 Phase Calibration

Phase calibration is implemented through SD24's preload register. Setting preload on the current channel induces extra delays between current and voltage, therefore, compensating original phase shift yield from circuits.

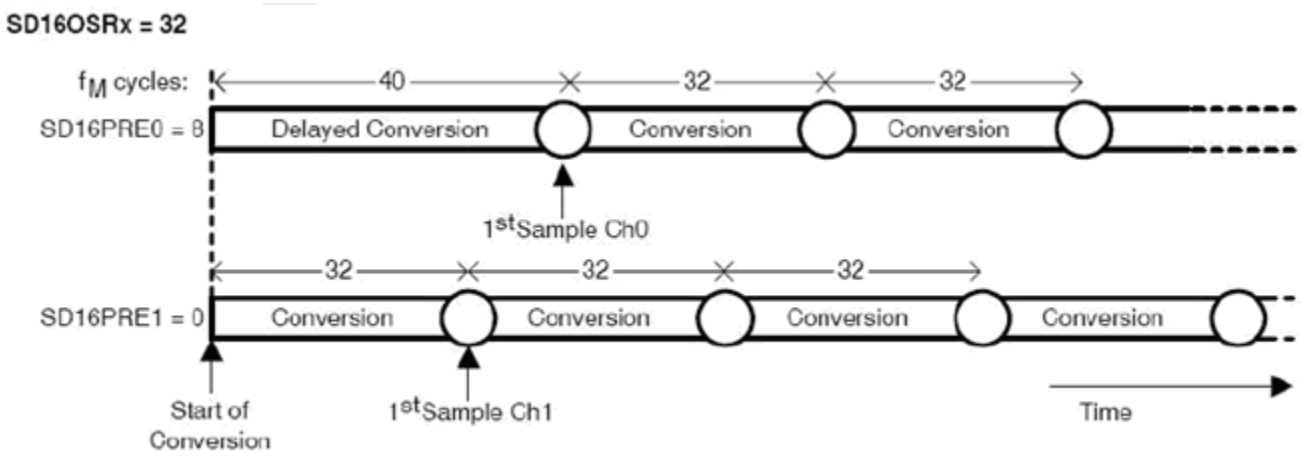

Figure 19. CSG Firmware Phase Calibration

Phase shift can be calculated using Equation 9:

$$\theta = \frac{360 \times f_{in}^{\cdot}}{OSR \times f_s} = \frac{360 \times f_{in}}{f_M} \tag{9}$$

f_m is ADC clock frequency, f_M is mains' frequency. If f_M = 50 Hz, and f_m = 256×4096 = 1 MHz, the step of phase shift is 0.017°.

Phase calibration should be done after slope and offset calibration. The calibration sequence is:

1. Configure system registers, select right ADC gain for voltage and current, chose the right channel to output energy pulse.
2. Read out old Px_PHASE value before modifying it and recode it as Px_PHASE$_n$.
3. Set generate to output 100% Ib current and set power factor to 0.5L, read active power measurement errors E.
4. Calculate the new Px_PHASE$_{n+1}$ according to Equation 10:

$$Px\_PHASE_{n+1} = Px\_PHASE_n + \frac{256 \times 4096}{2 \times \pi \times 50} \times (\arccos\frac{1+E}{2} - \frac{\pi}{3}) \tag{10}$$

5. Update the new Px_PHASE to MSP430AFE253 through SPI interface.

For example, if calculated E = 0.3%, original P1_PHASE$_n$ = 6, then the new P1_PHASE$_{n+1}$ = 10 + 6 = 16. To calibrate the CSG firmware, you can use either way:

- Use GUI: Type 6 on the Phase Shift edit box, and press the Update Calibration button on the meter configuration window.
- Send the calibration command to AFE253 to modify the P1_ PHASE register to 16 with packet: 0x8610001000

B.2.4.2.3 VRMS Calibration

VRMS calibration sequence is:

1. Configure system registers, select right ADC gain for voltage and current, chose the right channel to output energy pulse.
2. Read out old VRMS_FACTOR value before modifying it and recode it as VRMS_FACTOR$_n$.
3. Set generate to output 100% Ib current and set power factor to unity, read generator's output VRMS$_{GEN}$ and measured value VRMS$_{measure}$.
4. Calculate the new VRMS_FACTOR$_{n+1}$ according to Equation 11:

$$VRMS\_FACTOR_{N+1} = VRMS\_FACTOR_{N} \times \frac{VRMS_{GEN}}{VRMS_{measure}} \tag{11}$$

5. Update new VRMS_FACTOR to MSP430AFE253 through SPI interface.

For example, if VRMS$_{GEN}$ = 220 V and measured VRMS$_{measure}$ = 219 V, original VRMS_FACTOR$_n$ = 2000, then the error on VRMS E = 219/220-1=-0.45% and the new VRMS_FACTOR$_{n+1}$ = 2000*220/219=2009. To calibrate the CSG firmware, you can use either way:

- Use GUI: Type -0.45 on the Voltage Gain edit box, and press the Update Calibration button on the meter configuration window.
- Send the calibration command to AFE253 to modify the VRMS_FACTOR register to 2009 with packet: 0x8C097D097D.

B.2.4.2.4 IRMS Calibration

Single-point and dual-point meter calibration on IRMS are possible using the MSP430AFE2xx CSG firmware. When single point calibration is used, the slope (I1RMS_GAIN and I2RMS_GAIN) is calibrated. When dual-point calibration is required, the offset (I1RMS_OFFSET and I2RMS_OFFSET) is calculated in addition to the slope.

IRMS calibration sequence is :

1. Configure system registers, select right ADC gain for voltage and current, chose the right channel to output energy pulse.
2. Set IxRMS_OFFSET to 0 if it is modified by customer code. Read out old IxRMS_GAIN value before modifying it and recode it as IxRMS_GAIN$_n$
3. Set power factor to unity, read IxRMS measurement errors E_H and E_L on two test points: 100% Ib and 5% Ib.
4. Calculate new IxRMS_GAIN$_{n+1}$ according to Equation 12. Here, N_{H2L} denotes the rate between the large and small current, N_{H2L}=100%Ib / 5%Ib = 20.

$$IxRMS\_GAIN_{n+1} = \frac{IxRMS\_GAIN_{n} \times (N_{H2L} - 1)}{N_{H2L} \times (1 + E_H) - (1 + E_L)} \tag{12}$$

5. Calculate the new IxRMS_OFFSET$_{n+1}$ according to Equation 13. Here, N_{H2L} denotes the rate between the large and small current. I_{GEN} denotes the genuine IRMS sourced from the generator in small current points.

$$IxRMS\_OFFSET_{n+1} = \frac{(E_H - E_L) \times N_{H2L} \times I_{GEN} \times 100}{N_{H2L} \times (1 + E_H) - (1 + E_L)} \quad (13)$$

6. Update the new IxRMS_GAIN and IxRMS_OFFSET to MSP430AFE253 through SPI interface

For example, if the single point calibration is used and E_H = 0.5%, original I1RMS_GAIN$_n$ = 10000, then the new I1RMS_GAIN$_{n+1}$ =10000/(1+0.5%)=9950. To calibrate the CSG firmware, you can use either way.

- Use GUI: Type 0.5 on the Current Gain edit box, and press the Update Calibration button on the meter configuration.
- Send the calibration command to AFE253 to modify the I1RMS_FACTOR register to 9950 with packet: 0x82DE26DE26.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265