Application Report
SLAA180A–December 2003–Revised April 2018

Operating ADS1605 and ADS1606 in 2X Mode: 10 MSPS

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ABSTRACT

This application report discusses the built-in 2X mode of the ADS1605 and ADS1606 analog-to-digital converters (ADCs). In 2X mode, the data rate doubles to 10 MSPS. This report presents a brief overview, pin configuration, timing requirements, summary of key performances, and typical characteristics. In addition, this report also shows the settling time, impulse response, and frequency response of the digital decimation filter.

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1 Overview

The ADS1605 and ADS1606 (referred together here as ADS160x) are high-performance 16-bit, delta-sigma ADCs with a default oversampling ratio (OSR) of eight. The modulator uses an inherently stable 2-1-1 multistage noise-shaping (MASH) architecture incorporating proprietary circuitry that allows for very linear high-speed operation. The modulator samples the input signal at 40 MSPS (when f_{CLK} = 40 MHz). A low-ripple linear phase digital filter decimates the modulator output to provide data output at rates of 5 MSPS with a signal pass band out to 2.45 MHz.

To complement the data sheet, this application report describes the performance when the 2XMODE input pin is taken high, placing the device in 2X mode. The oversampling ratio is reduced to four, which doubles the data rate, and also reduces group delay and settling time, and decreases SNR performance. In 2X mode, the ADS160x operates at a 10-MSPS data rate with 14-bit SNR performance.

2 Pin Configuration

The 2XMODE digital input sets the decimation rate of the digital filter.

When 2XMODE = low, the decimation rate = 8.

When 2XMODE = high, the decimation rate = 4.

For the 10-MSPS performance, 2XMODE must be set high. Decreasing the decimation rate from 8 to 4 doubles the data rate. For f_{CLK} = 40 MHz, the data rate then becomes 10 MSPS with this lower decimation value.

In addition, the group delay decreases to 0.9 μs and the settling time becomes 1.3 μs or 13 DRDY cycles. With the reduced decimation rate, the noise increases. Typical SNR performance degrades by 14 dB when the decimation rate is 4 versus 8. THD remains approximately the same. There is an internal pulldown resistor of 170 kΩ on the 2XMODE; however, TI recommends this pin be forced either high or low externally. See the respective pin assignments and locations diagram and the terminal functions table in the ADS160x data sheet. Figure 1 shows the pin configuration for doubling the output data rate.

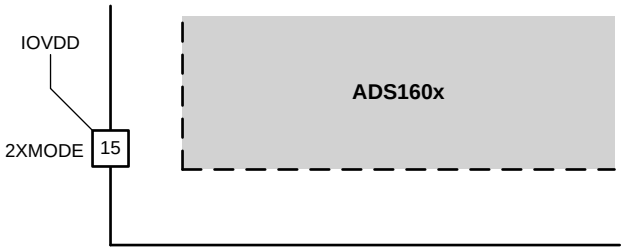

Figure 1. Pin Configuration for Doubling Output Data Rate

3 Timing Requirements

The timing requirements indicated in the ADS160x data sheet that are affected when operating at double data rate are shown in Table 1. See the ADS160x data sheet for timing diagram and timing label definition.

Table 1. Timing Requirements for Double Data Rate Mode

SYMBOL	DESCRIPTION	TYP	UNIT
t_4	$\overline{DRDY}$ pulse with high or low	8 t_1	ns
t_{12}	Delay from DOUT active to valid DOUT (settling to 0.001%)	13	$\overline{DRDY}$ Cycles

4 Summary of Key Performances

All specifications at T_A = 25°C, AVDD = 5 V, DVDD = IOVDD = 3 V, f_{CLK} = 40 MHz, External V_{REF} = 3 V, 2XMODE = high, V_{CM} = 2 V, and R_{BIAS} = 37 kΩ (unless otherwise noted).

Table 2. Typical Dynamic Performance(1)

TEST CONDITION	SNR (dB)	SINAD (dB)	THD (dB)	SFDR (dB)
f_{IN} = 100 kHz, V_{IN} = –2 dB	75	75	–95	98
f_{IN} = 100 kHz, V_{IN} = –6 dB	72	71	–98	102
f_{IN} = 100 kHz, V_{IN} = –20 dB	58	57	–97	91
f_{IN} = 500 kHz, V_{IN} = –2 dB	75	74	–98	95
f_{IN} = 500 kHz, V_{IN} = –6 dB	71	71	–98	102
f_{IN} = 500 kHz, V_{IN} = –20 dB	58	57	–84	88
f_{IN} = 2 MHz, V_{IN} = –2 dB	73	73	–90	90
f_{IN} = 2 MHz, V_{IN} = –6 dB	70	70	–92	92
f_{IN} = 2 MHz, V_{IN} = –20 dB	58	70	–79	79

(1) See the ADS160x data sheet for definition of measurement parameters.

Table 3. Digital Filter Characteristics

PARAMETER	TEST CONDITONS	MIN	TYP	MAX	UNIT
Pass band	±0.0003-dB ripple	0		$2.2\left(\frac{f_{CLK}}{40\ MHz}\right)$	MHz
Pass-band transition	–0.1-dB attenuation		$3\left(\frac{f_{CLK}}{40\ MHz}\right)$		MHz
	–3-dB attenuation		$4.5\left(\frac{f_{CLK}}{40\ MHz}\right)$		
Stop band	–40-dB attenuation	$6.9\left(\frac{f_{CLK}}{40\ MHz}\right)$		$33\left(\frac{f_{CLK}}{40\ MHz}\right)$	MHz
Group delay			$0.9\left(\frac{40\ MHz}{f_{CLK}}\right)$		µs
Settling time	±0.001%		$1.3\left(\frac{40\ MHz}{f_{CLK}}\right)$		µs

5 Typical Characteristics

All specifications at T_A = 25°C, AVDD = 5 V, DVDD = IOVDD = 3 V, f_{CLK} = 40 MHz, External V_{REF} = 3 V, 2XMODE = high, V_{CM} = 2 V, and R_{BIAS} = 37 kΩ (unless otherwise noted)

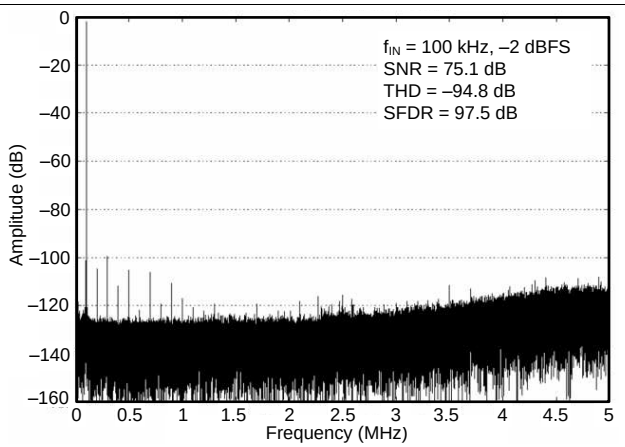

Figure 2. Spectral Response

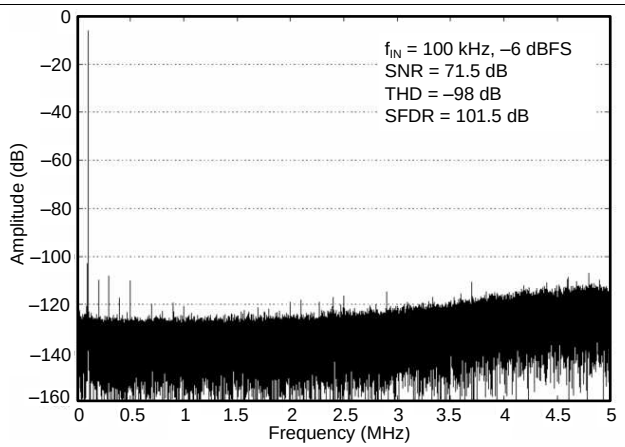

Figure 3. Spectral Response

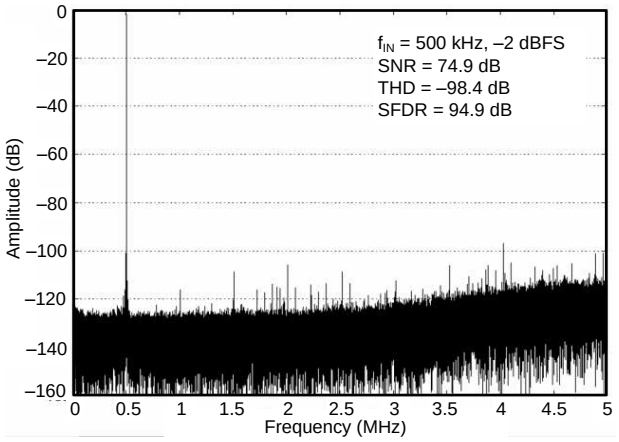

Figure 4. Spectral Response

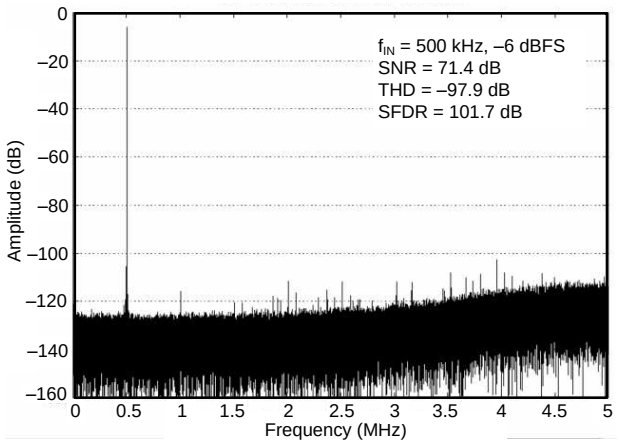

Figure 5. Spectral Response

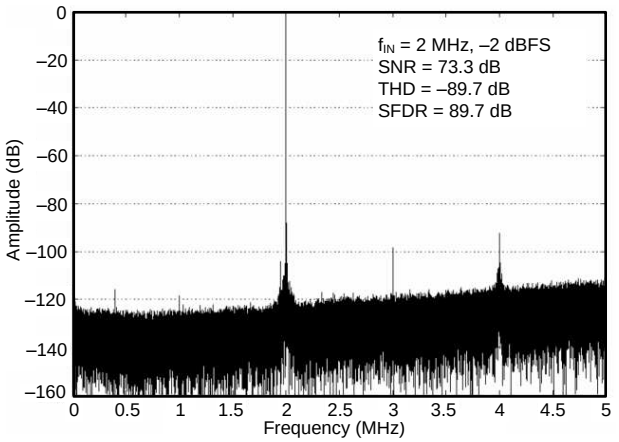

Figure 6. Spectral Response

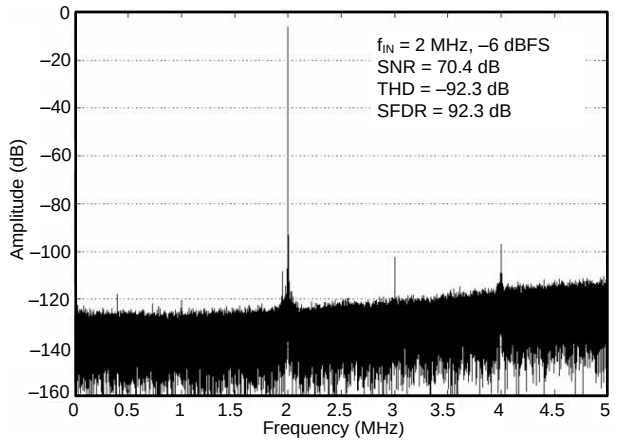

Figure 7. Spectral Response

Typical Characteristics (continued)

All specifications at T_A = 25°C, AVDD = 5 V, DVDD = IOVDD = 3 V, f_{CLK} = 40 MHz, External V_{REF} = 3 V, 2XMODE = high, V_{CM} = 2 V, and R_{BIAS} = 37 kΩ (unless otherwise noted)

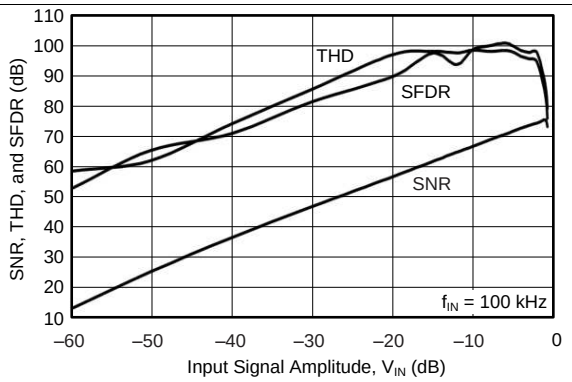

Figure 8. Signal-to-Noise Ratio, Total Harmonic Distortion, and Spurious-Free Dynamic Range vs Input Signal Amplitude

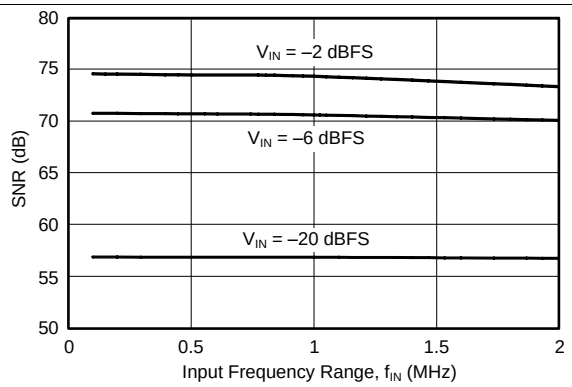

Figure 9. Signal-to-Noise Ratio vs Input Frequency

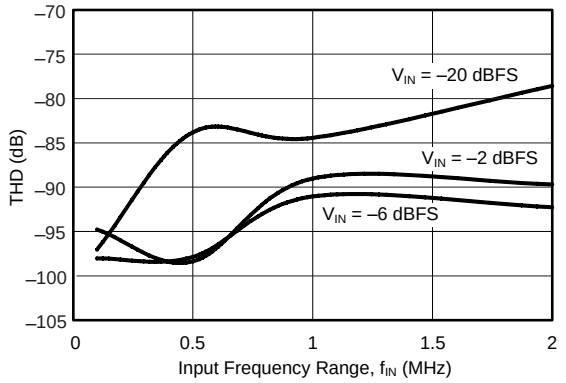

Figure 10. Total Harmonic Distortion vs Input Frequency

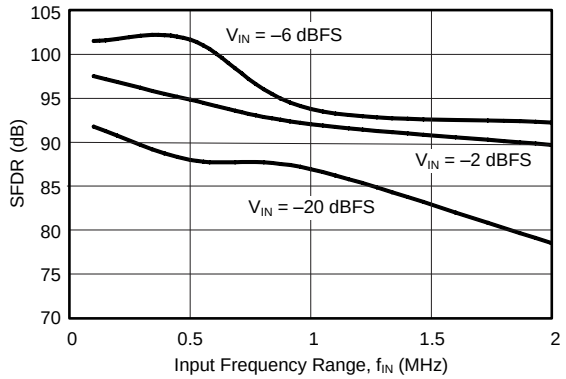

Figure 11. Spurious Free Dynamic Range vs Input Frequency

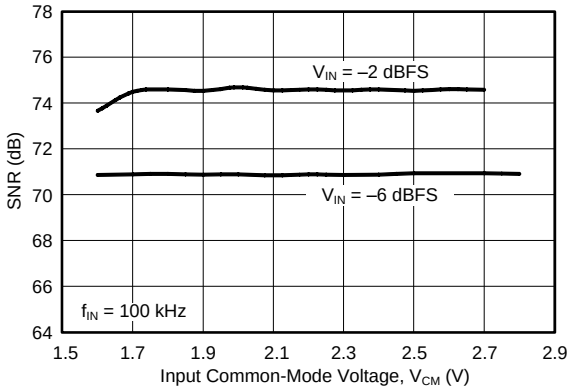

Figure 12. Signal-to-Noise Ratio vs Input Common-Mode Voltage

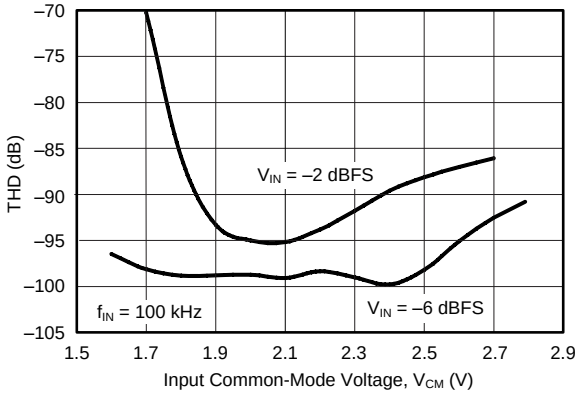

Figure 13. Total Harmonic Distortion vs Input Common-mode Voltage

Typical Characteristics (continued)

All specifications at T_A = 25°C, AVDD = 5 V, DVDD = IOVDD = 3 V, f_{CLK} = 40 MHz, External V_{REF} = 3 V, 2XMODE = high, V_{CM} = 2 V, and R_{BIAS} = 37 kΩ (unless otherwise noted)

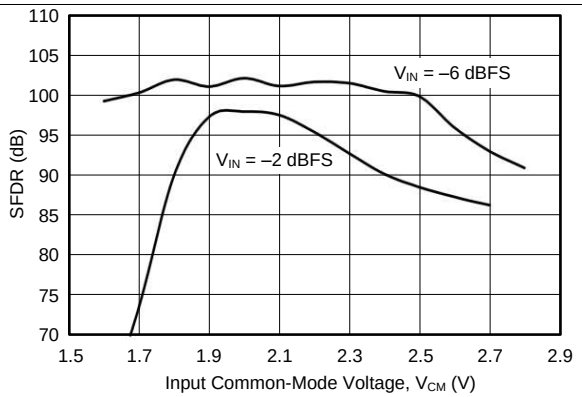

Figure 14. Spurious-Free Dynamic Range vs Input Common-Mode Voltage

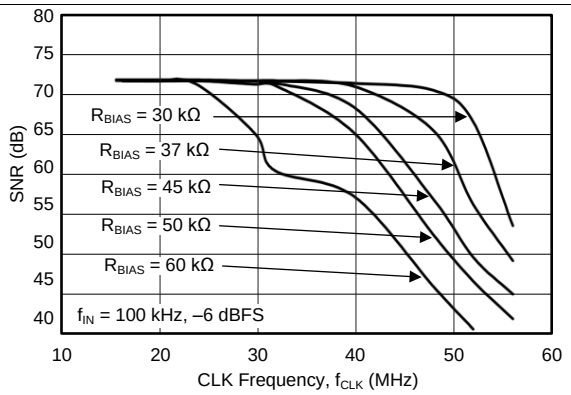

Figure 15. Signal-to-Noise Ratio vs CLK Frequency

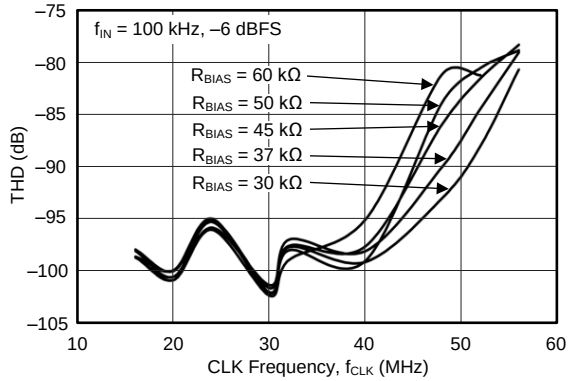

Figure 16. Total Harmonic Distortion vs CLK Frequency

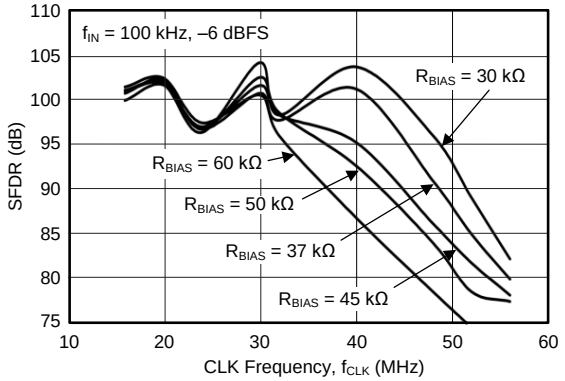

Figure 17. Spurious-Free Dynamic Range vs CLK Frequency

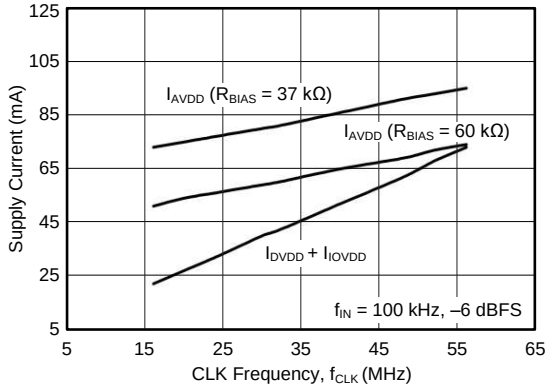

Figure 18. Supply Current vs CLK Frequency

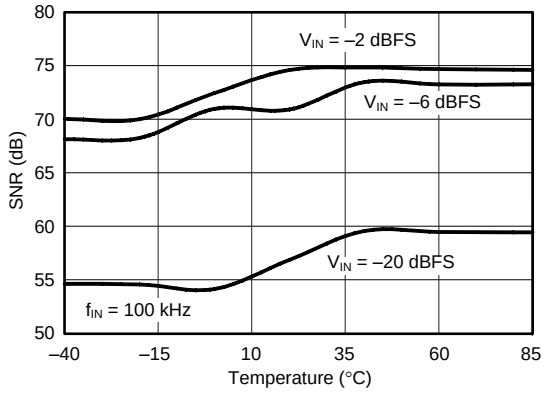

Figure 19. Signal-to-Noise Ratio vs Temperature

Typical Characteristics (continued)

All specifications at T_A = 25°C, AVDD = 5 V, DVDD = IOVDD = 3 V, f_{CLK} = 40 MHz, External V_{REF} = 3 V, 2XMODE = high, V_{CM} = 2 V, and R_{BIAS} = 37 kΩ (unless otherwise noted)

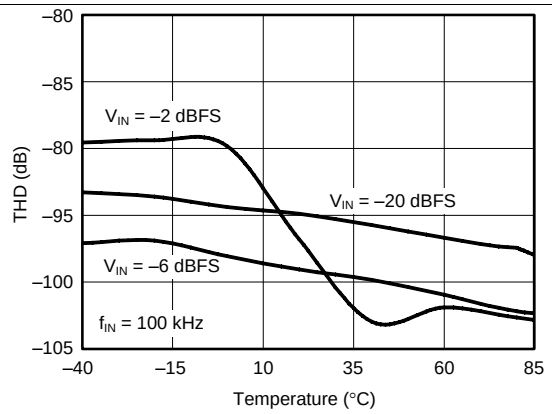

Figure 20. Total Harmonic Distortion vs Temperature

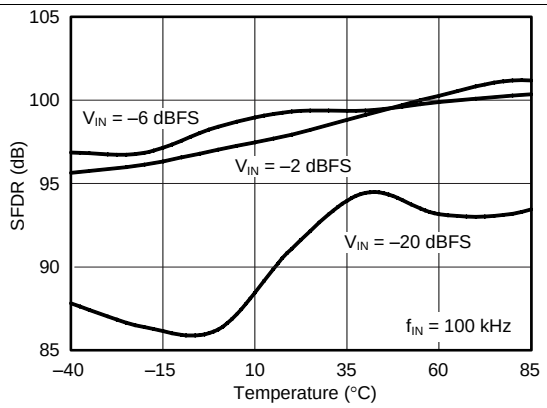

Figure 21. Spurious-Free Dynamic Range vs Temperature

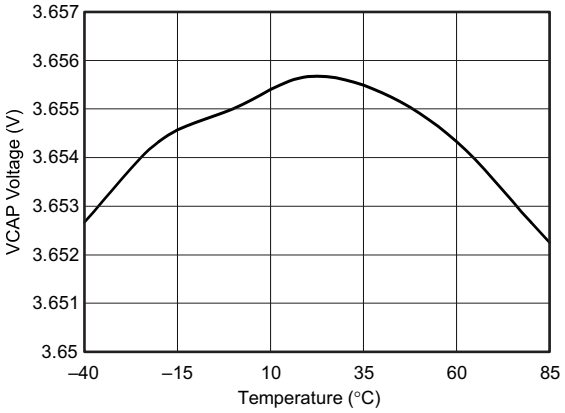

Figure 22. VCAP Voltage vs Temperature

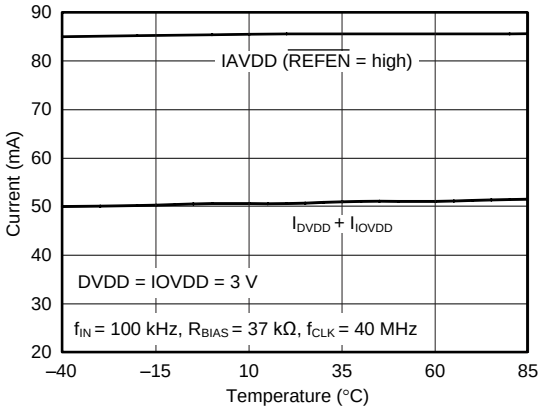

Figure 23. Power-Supply Current vs Temperature

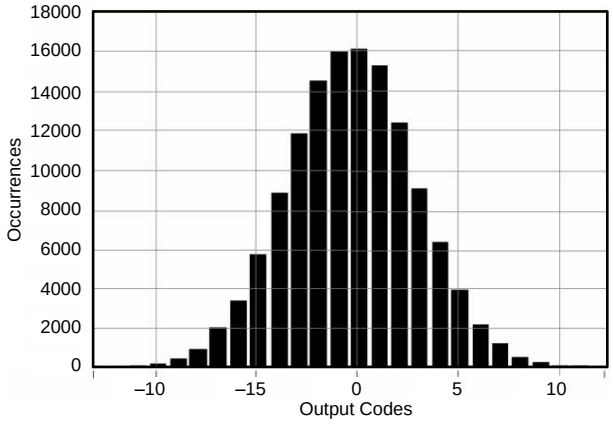

Figure 24. Number of Occurences for Output Codes With Inputs Shorted to V_{CM}

6 Digital Decimation Filter

6.1 Settling Time

The settling time is an important consideration when measuring signals with large steps or when using a multiplexer in front of the analog inputs. The ADS160x digital filter requires time for an instantaneous change in signal level to propagate to the output. Make sure to allow the filter time to settle after applying a large step in the input signal, switching the channel on a multiplexer placed in front of the inputs, resetting the ADS160x, or when exiting the power-down mode. Figure 25 shows the settling error as a function of time for a full-scale signal step applied at t = 0 with 2XMODE = high. Figure 25 uses DRDY cycles for the time scale (X-axis). After 13 DRDY cycles, the settling error drops below 0.001%. For f_{CLK} = 40 MHz, this corresponds to a settling time of 1.3 μs.

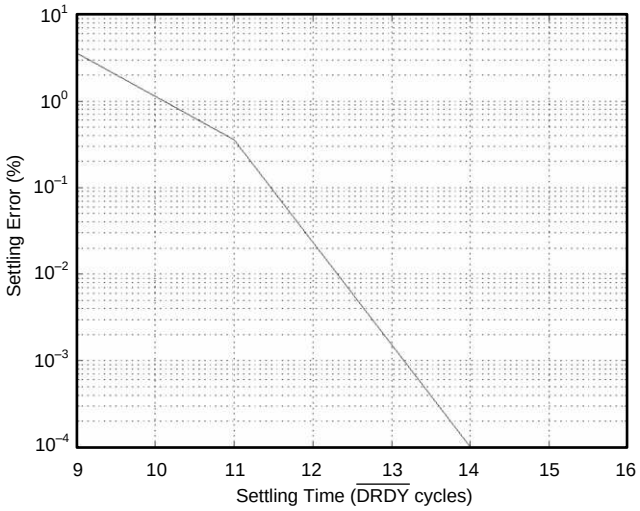

Figure 25. Settling Time

6.2 Impulse Response

Figure 26 plots the normalized response for an input applied at t = 0 with 2XMODE = high. The X-axis units of time are DRDY cycles. As shown in Figure 26, the peak of the impulse takes nine DRDY cycles to propagate to the output. For f_{CLK} = 40 MHz, a DRDY cycle is 0.1 μs in duration, and the propagation time (or group delay) is 9 × 0.1 μs = 0.9 μs.

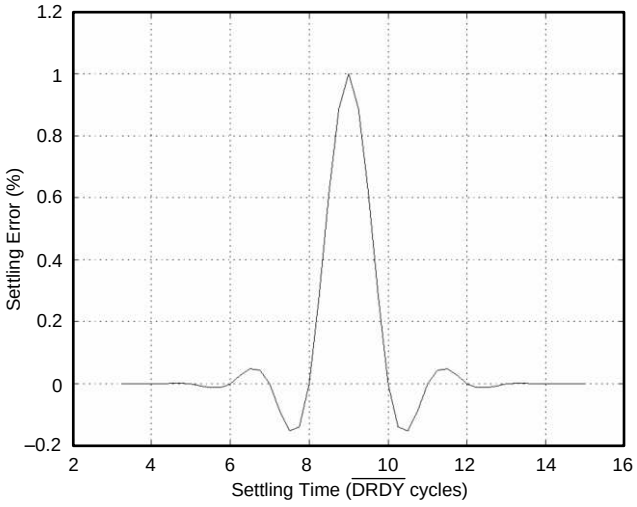

Figure 26. Impulse Response

6.3 Frequency Response

The linear phase FIR digital filter sets the overall frequency response. The decimation rate is set to 4 (2XMODE = high) for all the figures shown in this section. Figure 27 shows the frequency response from dc to 20 MHz for f_{CLK} = 40 MHz. The frequency response of the ADS160x filter scales directly with CLK frequency. For example, if the CLK frequency is decreased by half (to 20 MHz), the values on the X-axis in Figure 27 must to be scaled by half, with the span becoming dc to 10 MHz. Figure 28 shows the pass-band ripple from dc to 2.2 MHz (f_{CLK} = 40 MHz). Figure 29 shows a closer view of the pass-band transition by plotting the response from 2 MHz to 5 MHz (f_{CLK} = 40 MHz). The overall frequency response repeats at multiples of the CLK frequency. To help illustrate this, Figure 30 shows the response out to 120 MHz (f_{CLK} = 40 MHz). Notice how the pass-band response repeats at 40 MHz, 80 MHz, and 120 MHz; important to consider, when there is high-frequency noise present with the signal. The modulator bandwidth extends to 100 MHz. High-frequency noises around 40 MHz and 80 MHz are not attenuated by either the modulator or the digital filter. This noise aliases back in-band, and reduces the overall SNR performance unless the noise is filtered out prior to the ADS1605. To prevent this, place an antialias filter in front of the ADS160x.

Within the 2.2-MHz pass band for f_{CLK} = 40 MHz, the pass-band ripple decreased to ±0.0003 (when 2XMODE = high) compared to ±0.0025 (when 2XMODE = low). The –0.1-dB pass-band transition increases up to 3 MHz, while the –3-dB pass-band transition increases up to 4.5 MHz for f_{CLK} = 40 MHz when 2XMODE = high.

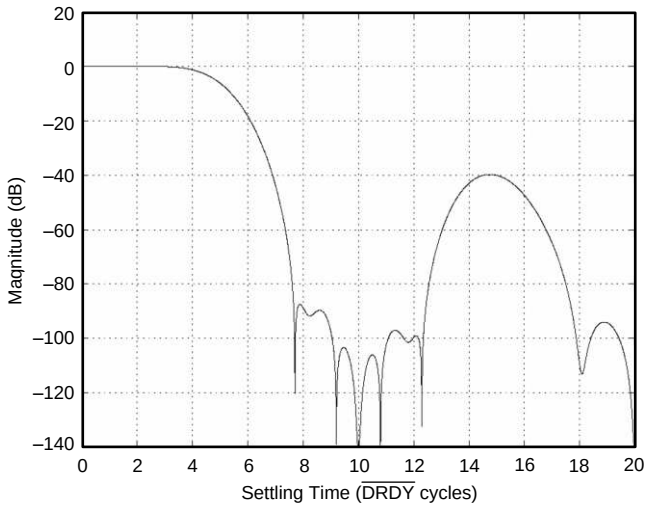

Figure 27. Frequency Response

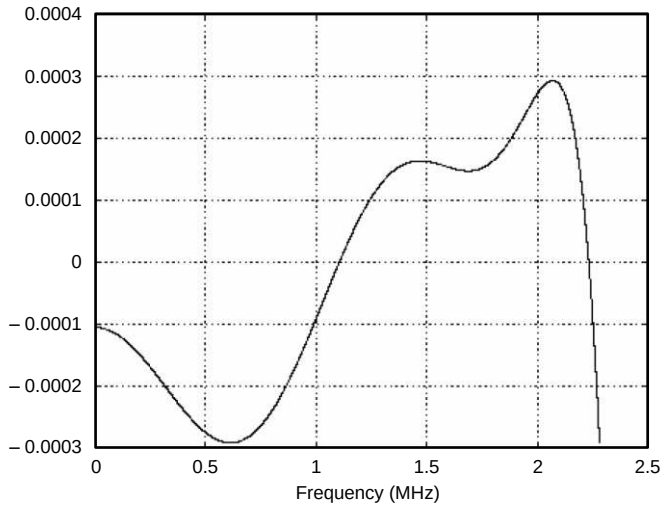

Figure 28. Pass-Band Ripple

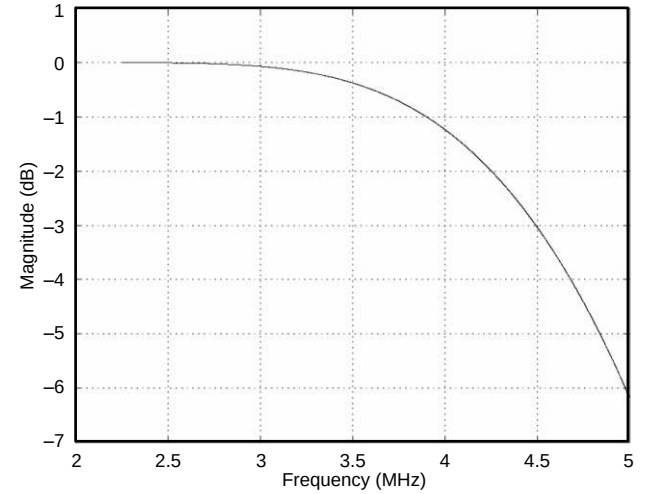

Figure 29. Pass-Band Transition

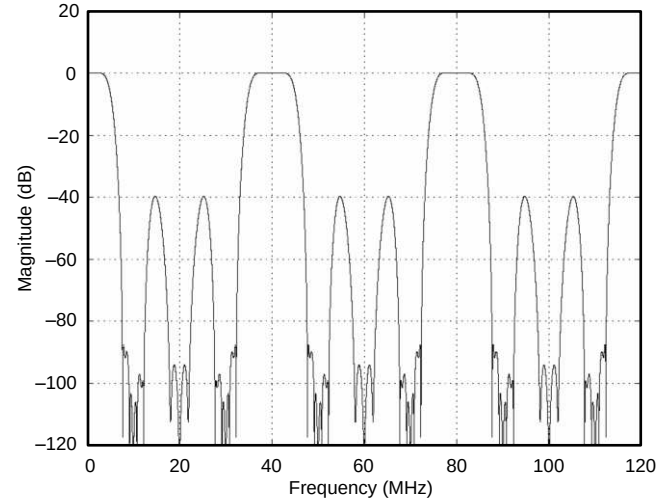

Figure 30. Frequency Response Out to 120 MHz

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2003) to A Revision	Page
• Changed document to meet Texas Instruments formatting standards	3

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