



P.O. Box 84  
 Sherman, TX 75090  
 6412 Hwy 75 South  
 Sherman, TX 75090

(903) 868-7111

## Texas Instruments Extended Temperature Products Reliability Report

(Subject To Attached Disclaimers)

Device Type/Device Family: OMAPL137PTPH  
 Package Type: 176/PTP  
 Wafer Fabrication Facility: TSMC-F14  
 Assembly/Test Facility: PHI (TIPI)  
 Compiled: 04/12

### Biased Life Test

Test Method: JESD22-A108  
 Test Condition: 175C/1000 hours or equivalent 45/0 Minimum Sample  
 Sample Size: 45  
 Rejects: 0

### Package Sequence Test

<u>Description</u>	<u>Condition</u>	<u>Referenced Method</u>	<u>Lot/Sample</u>	<u>Rejects</u>
Preconditioning		QSS009-142 JEDEC Std. 22 Method A112/A113	3/45	0
CSAM/TSAM Exposed pad devices only	No Delamination		3/45	0
Storage Bake	2000hr @ Data Sheet Operating Temperature		3/45	N/A
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles or equivalent	JESD22-A104-A	3/45	N/A
Electrical Test	Per Data Sheet with Additional Pin to Pin Leakage Testing		3/45	0
CSAM	No Delamination on Lead or Die		3/5	0
TSAM Exposed pad devices only	50% Maximum Mount Pad Delamination		3/5	0
Decap/Bond Pull	Wirebond Packages Only		3/5-15 Wires	0
Decap/Bond Shear	Wirebond Packages Only	ASTM F-459	3/5-15 Wires	0
Cross Section	Through ball bond or flip chip bump	Examine for bond Integrity	3/1	0

### Additional Qualification Testing

The subject Enhanced Plastic device, device family, and/or package family have passed Texas Instruments product qualification as follows:

<u>Description</u>	<u>Condition</u>	<u>Referenced Method</u>	<u>Sample Size</u>	
Electrical Characterization	TI Data Sheet	N/A	30 Units	
Electrostatic Discharge Sensitivity	HBM	EIA/JESD22-A114	3 Units/voltage	
	MM	EIA/JESD22-A115	3 Units/voltage	
	CDM	JESD22-C101	3 Units/voltage	
Latch-up	Per Technology	EIA/JESD78	6/0	
Physical Dimensions	TI Data Sheet	EIA/JESD22- B100	15/0	
Thermal Impedance	Theta-JA on board	EIA/JESD51	Per Pin-Package	
Bias Life Test	125°C / 1000 hours or equivalent	JESD22-A108	77/0	
Biased Humidity or HAST	85°C / 85% / 1000 hours	JESD22-A101	77/0	*
	130°C / 85% / 96 hours	JESD22-A110		
Autoclave or Unbiased HAST	121°C @ 2 atm / 96 hours	JESD22-A102	77/0	*
	130°C / 85% / 96 hours	JESD22-A110		
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles or equivalent	JESD22-A104	77/0	*
Solderability	Condition A (steam age for 8 hours)	ANSI/J-STD-002-92	22/0	
Bond Strength	-	ASTM F-459	30/0	
Moisture Sensitivity	Surface Mount Only	J-STD-020-A	12/0	

\* Preconditioning per JEDEC Std. 22, Method A112/A113

### Supplemental Device Characteristics

Master Die: YF771673A  
 Wafer Fab: TSMC-F14  
 Fab Process: 1218C021.M6NAW  
 Fab Technology: CMOS  
 Die Revision: TSMC-F14  
 Passivation: Oxy Nitride  
 Metal 1: Cu  
 Metal 2: Cu

Assembly Site: 4209748-0002 (roughened LF)  
 Pin/Package Type: Cu  
 Lead Composition: 7.311 X 5.734  
 Lead Finish: NiPdAu  
 Packaged Die Thickness: 3A991A2  
 MSL Level: MSL4/260C  
 Metal 3: Cu  
 Metal 4: Cu

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