Functional Safety Information

SN4599-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN4599-Q1 (SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

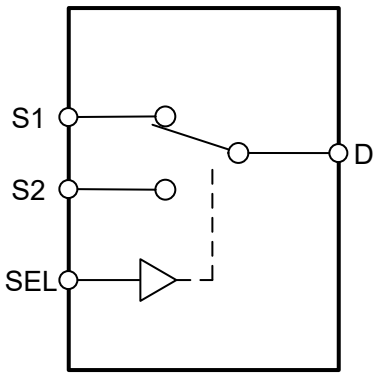

Figure 1-1. Functional Block Diagram

SN4599-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the SN4599-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	9
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 300 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS ASICs Analog and Mixed = < 50V supply	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN4599-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
MUX no output (HIZ)	5%
MUX channel stuck on	5%
MUX channel stuck off	45%
MUX functional out of specification voltage or timing	45%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN4599-Q1 (SOT-23 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the SN4599-Q1 data sheet.

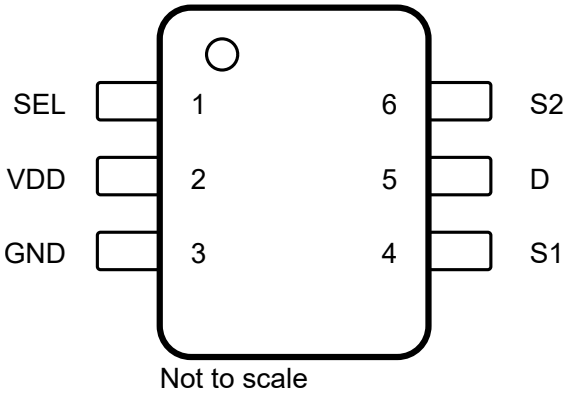

Figure 4-1. Pin Diagram (SOT-23 Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	SEL stuck low. Cannot control switch states	B
VDD	2	Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
GND	3	No effect, normal operation	D
S1	4	Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path device damage possible Device unpowered.	A
D	5	Corruption of signal passed onto the S1/S2 pins. If there is no limiting resistor in the switch path device damage possible	A
S2	6	Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path device damage possible	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	Loss of control of SEL pin. Cannot control switch.	B
VDD	2	Device unpowered. Device not functional.	B
GND	3	Device unpowered. Device not functional.	B
S1	4	Corruption of signal passed onto the D pin.	B
D	5	Corruption of signal passed onto the S1/S2 pins.	B
S2	6	Corruption of signal passed onto the D pin.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted To	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	VDD	SEL stuck high. Can no longer switch signal path of the device	B
VDD	2	GND	Device is unpowered. Device is not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
GND	3	S2	Not considered. This is a corner pin.	D
S2	4	D	Corruption of signal passed onto the D pin.	B
D	5	S1	Corruption of signal passed onto the S1/S2 and D pins.	A
S1	6	VDD	Not considered. This is a corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SEL	1	SEL stuck high. Cannot control switch states	B
VDD	2	No effect; normal operation	D
GND	3	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met. Otherwise, device damage may be plausible.	A
S2	4	Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path device damage is possible.	A
D	5	Corruption of signal passed onto the S1/S2 pins. If there is no limiting resistor in the switch path device damage is possible.	A
S1	6	Corruption of signal passed onto the D pin. If there is no limiting resistor in the switch path device damage is possible.	A

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