Functional Safety Information

RES11A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the RES11A-Q1 (SOT-23-THIN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the device estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

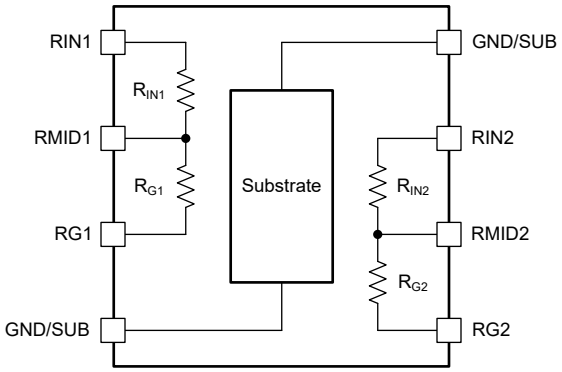

Figure 1-1. Functional Block Diagram

The RES11A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

The RES11A-Q1 is a pair of resistor dividers implemented in a semiconductor process. The device has no active elements such as transistors or ESD cells, which complicates the calculation of effective FIT rates. As the tools conventionally used for this task are unable to parse a chip that contains zero active elements, the limit as the active element count goes to zero is used for all calculations reported in this document.

The *Recommended Operating Conditions* section of the RES11A-Q1 data sheet specifies a maximum sustained current through each R_{IN} and R_G resistor for long-term operation. For a given RES11A-Q1 device, the lesser of these two values defines the maximum sustained divider current. The maximum divider impedance occurs in the event that the absolute tolerance of each resistor is +12% from the nominal value, and results in the highest possible values for R_G and R_{IN}. The square of the maximum sustained divider current, multiplied by the maximum divider impedance, thus defines the maximum power dissipation of the divider. As the RES11A-Q1 contains two dividers per package, multiplying this result by two gives the maximum recommended power dissipation of the device.

The maximum allowed power dissipation does also depend on environmental conditions. In cases where the ambient temperature combined with the self-heating associated with a given power dissipation (given $R_{\theta JA}$ = 156.2°C/W) leads the expected junction temperature to exceed the absolute maximum of 150°C, the power dissipation must be reduced accordingly.

As the effective FIT rate is highly dependent on the power dissipation of the device, a different FIT rate table is presented for each of the RES11A-Q1 ratios available. Estimated FIT rates are provided for cases where 100%, 80%, 60%, 40%, and 20% of the maximum allowed power dissipation is utilized.

2.1 SOT-23-THIN Package: RES11A10-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A10-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	16	13	10	7	6
Die FIT rate	13	10	7	5	4
Package FIT rate	3	3	3	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 357 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT-23-THIN Package: RES11A15-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A15-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	9	7	6	6	5
Die FIT rate	6	5	4	4	3
Package FIT rate	3	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 198 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 SOT-23-THIN Package: RES11A16-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A16-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	8	7	6	6	5
Die FIT rate	6	5	4	4	3
Package FIT rate	2	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 172 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.4 SOT-23-THIN Package: RES11A20-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A20-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-7. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	7	6	6	6	5
Die FIT rate	5	4	4	4	3
Package FIT rate	2	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 134 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-8. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.5 SOT-23-THIN Package: RES11A25-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A25-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-9. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	12	10	8	6	5
Die FIT rate	9	7	6	4	3
Package FIT rate	3	3	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 278 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-10. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.6 SOT-23-THIN Package: RES11A30-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A30-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-11. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	14	11	9	7	5
Die FIT rate	11	8	6	5	3
Package FIT rate	3	3	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 317 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-12. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.7 SOT-23-THIN Package: RES11A40-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A40-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-13. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	10	8	7	6	5
Die FIT rate	7	6	5	4	3
Package FIT rate	3	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 224 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-14. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.8 SOT-23-THIN Package: RES11A50-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A50-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-15. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	8	7	6	6	5
Die FIT rate	6	5	4	4	3
Package FIT rate	2	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 171 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-16. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.9 SOT-23-THIN Package: RES11A90-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A90-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-17. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	10	7	6	6	5
Die FIT rate	7	5	4	4	3
Package FIT rate	3	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 199 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-18. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.10 SOT-23-THIN Package: RES11A00-Q1

This section provides functional safety failure in time (FIT) rates for the SOT-23-THIN package of the RES11A00-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-19. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)				
	100% of Rated Power	80%	60%	40%	20%
Total component FIT rate	10	8	7	6	5
Die FIT rate	7	6	5	4	3
Package FIT rate	3	2	2	2	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 219 mW (100% of maximum rated power)
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-20. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the RES11A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	10%
Output short to RGx or RINx	30%
Output short to GND/SUB	30%
Output functional, not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the RES11A-Q1 (SOT-23-THIN). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the RES11A-Q1 pin diagram for the SOT-23-THIN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the RES11A-Q1 data sheet.

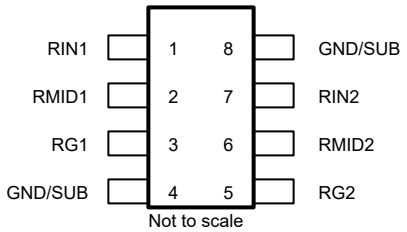

Figure 4-1. Pin Diagram for SOT-23-THIN Package

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- 'Short circuit to VEE or Ground' means short to GND/SUB
- 'Short circuit to Supply or VCC' means shorted to a source of power at a different potential than GND/SUB
- 'Divider 1' means the circuit of RIN1, RMID1, and RG1
- 'Divider 2' means the circuit of RIN2, RMID2, and RG2

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (VEE)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RIN1	1	RIN1 is set to VEE. Device functions as intended if VEE–VRG1 does not exceed maximum rating.	A
RMID1	2	RMID1 is set to VEE. Device functions as intended if VEE–VRIN1 and VEE–VRG1 do not exceed maximum ratings.	A
RG1	3	RG1 is set to VEE. Device functions as intended if VEE–VRIN1 does not exceed maximum rating.	A
GND	4	If GND2 is left floating, the device substrate is biased to VEE and functions as intended. If GND2 is also biased, then voltage can develop across the substrate, potentially damaging the device. If both GND1 and GND2 are short circuited, a current path can form through the substrate, potentially damaging the device.	A
GND	5	If GND1 is left floating, the device substrate is biased to VEE and functions as intended. If GND1 is also biased then voltage can develop across the substrate, potentially damaging the device. If both GND1 and GND2 are short circuited, a current path can form through the substrate, potentially damaging the device.	A
RIN2	6	RIN2 is set to VEE. Device functions as intended if VEE–VRG2 does not exceed maximum rating.	A
RMID2	7	RMID2 is set to VEE. Device functions as intended if VEE–VRIN2 and VEE–VRG2 do not exceed maximum rating.	A
RG2	8	RG2 is set to VEE. Device functions as intended if VEE–VRIN2 does not exceed maximum rating.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RIN1	1	No impact on performance, resistor is left floating. Device remains functional. Divider 1 midpoint voltage is unreliable	B
RMID1	2	No impact on device functionality. Divider 2 midpoint is unable to be read by external circuitry	D
RG1	3	No impact on performance, resistor is left floating. Device remains functional. Divider 1 midpoint voltage is unreliable	B
GND1	4	Depending on circuit configuration, circuit noise is increased and device bandwidth is increased.	C
GND2	5	Depending on circuit configuration, circuit noise is increased and device bandwidth is increased.	C
RIN2	6	No impact on performance, resistor is left floating. Device remains functional. Divider 2 midpoint voltage is unreliable	B
RMID2	7	No impact on device functionality. Divider 2 midpoint is unable to be read by external circuitry	D
RG2	8	No impact on performance, resistor is left floating. Device remains functional. Divider 2 midpoint voltage is unreliable	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RIN1	1	RMID1	RIN1 resistance is forced into short circuit condition with VMID1 voltage ultimately forced to VRIN1 voltage. The voltage between VRIN1 and VRG1 must not exceed maximum voltage rating or device damage will occur.	B
RMID1	2	RG1	RG1 resistance is forced into short circuit condition with VMID1 voltage ultimately forced to VRG1 voltage. The voltage between VRIN1 and VRG1 must not exceed maximum voltage rating or device damage will occur.	B
RG1	3	GND1	If GND2 is floating then the substrate is biased to VRG1 and functions as intended. If GND2 is also biased then voltage can develop across the substrate potentially damaging the device.	A
GND1	4	GND2	GND1 and GND2 are short circuited and a current return path forms through the substrate potentially damaging the device.	A
GND2	5	RIN2	If GND1 is floating then the substrate is biased to VRIN2 and functions as intended. If GND1 is also biased then voltage can develop across the substrate potentially damaging the device.	A
RIN2	6	RMID2	RIN2 resistance is forced into short circuit condition with VMID2 voltage ultimately forced to VRIN2 voltage. The voltage between VRIN2 and VRG2 must not exceed maximum voltage rating or device damage will occur.	B
RMID2	7	RG2	RG2 resistance is forced into short circuit condition with VMID2 voltage ultimately forced to VRG2 voltage. The voltage between VRIN2 and VRG2 must not exceed maximum voltage rating or device damage will occur.	B
RG2	8	RIN1	Device inputs are shorted together leaving the RG2 pin and RIN1 pin at some voltage between VRG1 and VRIN2. The device functions as intended if VRG2–VMID2 and VRIN1–VMID1 do not exceed maximum rating.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (VCC)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RIN1	1	RIN1 is set to VCC. Device functions as intended if VCC–VRG1 does not exceed maximum rating.	A
RMID1	2	RMID1 is set to VCC. Device functions as intended if VCC–VRIN1 and VCC–VRG1 do not exceed maximum rating.	A
RG1	3	RG1 is set to VCC. Device functions as intended if VCC–VRIN1 does not exceed maximum rating.	A
GND1	4	If GND2 is left floating, the device substrate is biased to VCC and functions as intended. If GND2 is also biased then voltage can develop across the substrate, potentially damaging the device. If both GND1 and GND2 are short circuited, a current path can form through the substrate, potentially damaging the device.	A
GND2	5	If GND1 is left floating, the device substrate is biased to VCC and functions as intended. If GND1 is also biased then voltage can develop across the substrate, potentially damaging the device. If both GND1 and GND2 are short circuited, a current path can form through the substrate, potentially damaging the device.	A
RIN2	6	RIN2 is set to VCC. Device functions as intended if VCC–VRG2 does not exceed maximum rating.	A
RMID2	7	RMID2 is set to VCC. Device functions as intended if VCC–VRIN2 and VCC–VRG2 do not exceed maximum rating.	A
RG2	8	RG2 is set to VCC. Device functions as intended if VCC–VRIN2 does not exceed maximum rating.	A

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