Functional Safety Information

TXV0106-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TXV0106-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

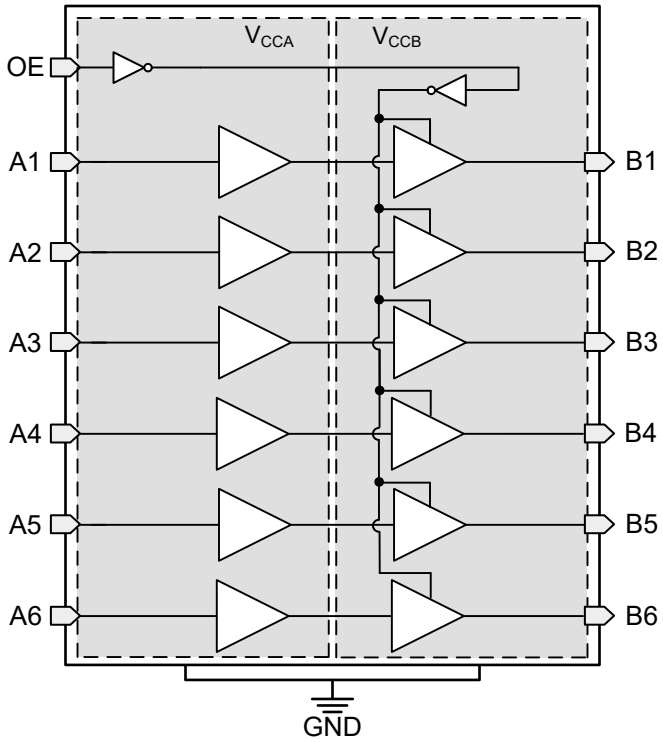

Figure 1-1. Functional Block Diagram

TXV0106-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on Siemens Norm SN 29500-2

This section provides Functional Safety Failure In Time (FIT) rates for WQFN package of TXV0106-Q1 based on industry-wide used reliability standards:

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	2
Package FIT Rate	5

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 24 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS Analog switch, Bus Interface	5 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TXV0106-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Driver HIZ no output	31%
Functional fail (voltage, timing; out of specification)	33%
Driver stuck at fault high	14%
Driver stuck at fault low	14%
Driver stuck at undetermined state	8%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TXV0106-Q1 (WQFN package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Figure 4-1 shows the TXV0106-Q1 pin diagram for the WQFN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TXV0106-Q1 data sheet.

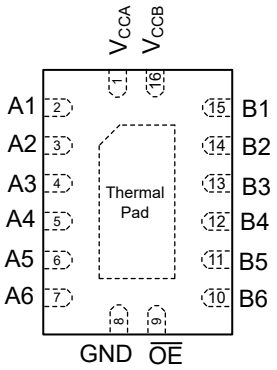

Figure 4-1. Pin Diagram (WQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	GND short to VCC, device will be bypassed . This may cause system damage, but not device damage	B
A1 - A6	2 to 7	Ax will be LOW, if corresponding Bx is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Bx is LOW, then nothing will occur, no damage.	B
GND	8	Normal operation.	D
OE (active low)	9	Outputs will remain enabled	B
B6 - B1	10 to 15	Bx will be LOW, if corresponding Ax is HIGH, there will be potential damage to the device if the current is not limited. If corresponding Ax is LOW, then nothing will occur, no damage.	B
VCCB	16	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device will not be powered.	B
A1 - A6	2 to 7	Ax input pins will be floating, there will be potential damage to the device if the current is not limited.	A
GND	8	Device will not be powered.	B
OE (active low)	9	OE input pin will be floating, there will be potential damage to the device causing outputs to switch between enabled and disabled, if the current is not limited.	B
B6 - B1	10 to 15	Bx output pins will be in HiZ if device is disabled. If device is enabled, it will be HIGH or LOW depending on the input.	D
VCCB	16	Device will not be powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	A1	A1 will be HIGH, if corresponding B1 is LOW, there will be potential damage to the device if the current is not limited. If corresponding B1 is HIGH, then nothing will occur, no damage.	B
A(n)	2 to 6	A(n+1)	Two inputs shorted together will not cause damage unless there is external bus contention that drives the input such that VIL < Input Voltage < VIH in which case excessive supply current to GND may cause damage.	B
A6	7	GND	A6 will be LOW, if corresponding B6 is HIGH, there will be potential damage to the device if the current is not limited. If corresponding B6 is LOW, then nothing will occur, no damage.	B
GND	8	OE (active low)	Outputs will remain enabled.	B
OE (active low)	9	B6	If B6 is HIGH, OE will be LOW and the outputs will remain enabled. If corresponding B6 is LOW, then outputs will be disabled.	B
B(n)	10 to 15	B(n+1)	Two outputs shorted together may cause damage if there is external bus contention that drives one LOW while driving the other HIGH.	D
B1	15	VCCB	B1 will be HIGH, if corresponding A1 is LOW, there will be potential damage to the device if the current is not limited. If corresponding A1 is HIGH, then nothing will occur, no damage.	B
VCCB	16	VCCA	GND short to VCC, device will be bypassed . This may cause system damage, but not device damage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply VCCA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Normal operation.	D
A1 - A6	2 to 7	Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur, no damage.	B
GND	8	GND short to VCC, device will be bypassed. This may cause system damage, but not device damage.	B
OE (active low)	9	Outputs will remain disabled.	B
B6 - B1	10 to 15	Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage.	B
VCCB	16	VCCB short to VCCA, device will be bypassed. This may cause system damage, but not device damage.	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to supply VCCB

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	VCCB short to VCCA, device will be bypassed . This may cause system damage, but not device damage	B
A1 - A6	2 to 7	Ax will be HIGH, if corresponding Bx is LOW, there will be potential damage to the device if the current is not limited. If corresponding Bx is HIGH, then nothing will occur; no damage.	B
GND	8	GND short to VCC, device will be bypassed. This may cause system damage, but not damage to the device.	B
OE (active low)	9	Outputs will remain disabled.	B
B6 - B1	10 to 15	Bx will be HIGH, if corresponding Ax is LOW, there will be potential damage to the device if the current is not limited. If corresponding Ax is HIGH, then nothing will occur, no damage.	B
VCCB	16	Normal operation.	D

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