Functional Safety Information

TPS2663
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

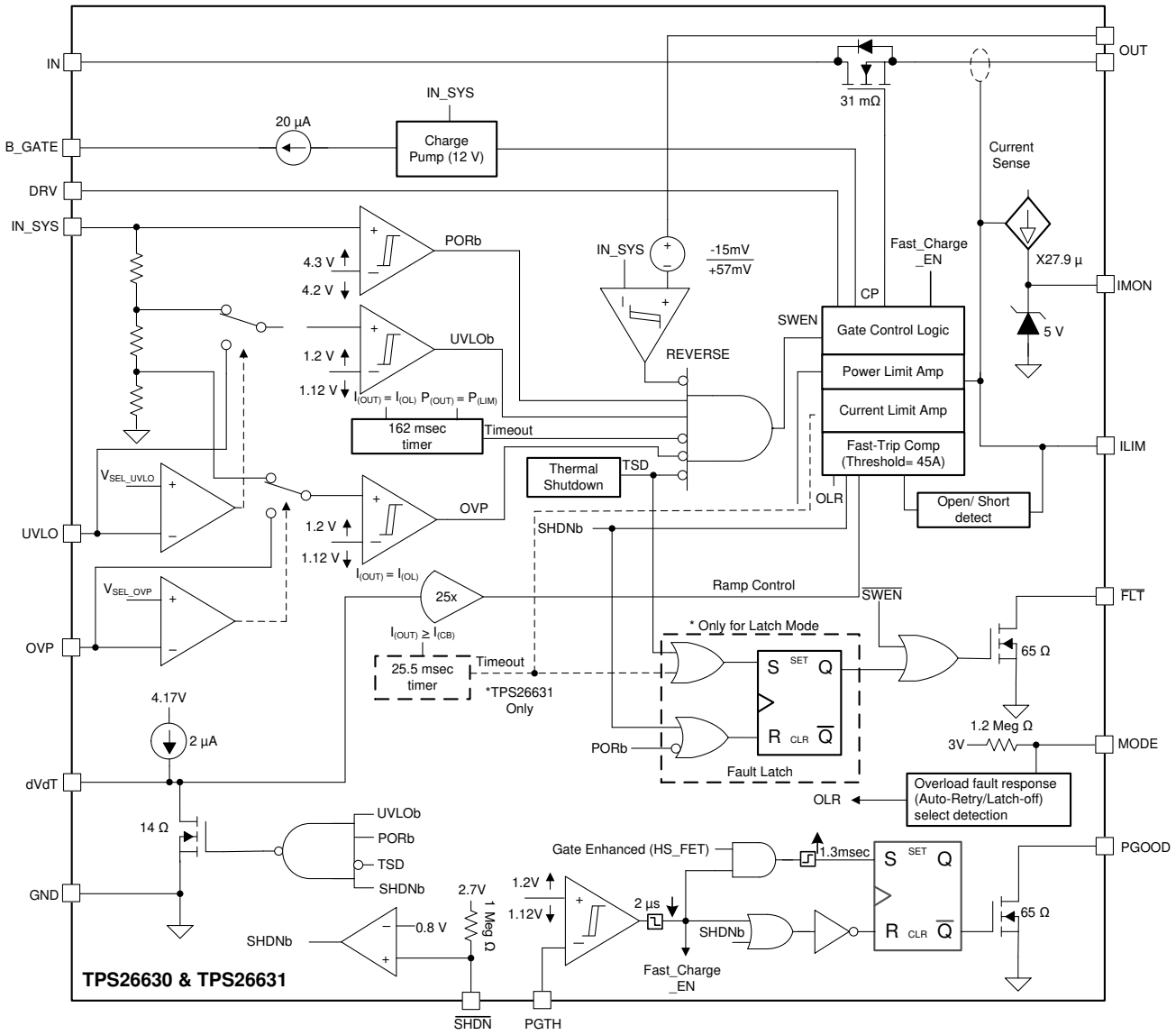
Trademarks

1 Overview

This document contains information for TPS2663 (VQFN and HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.



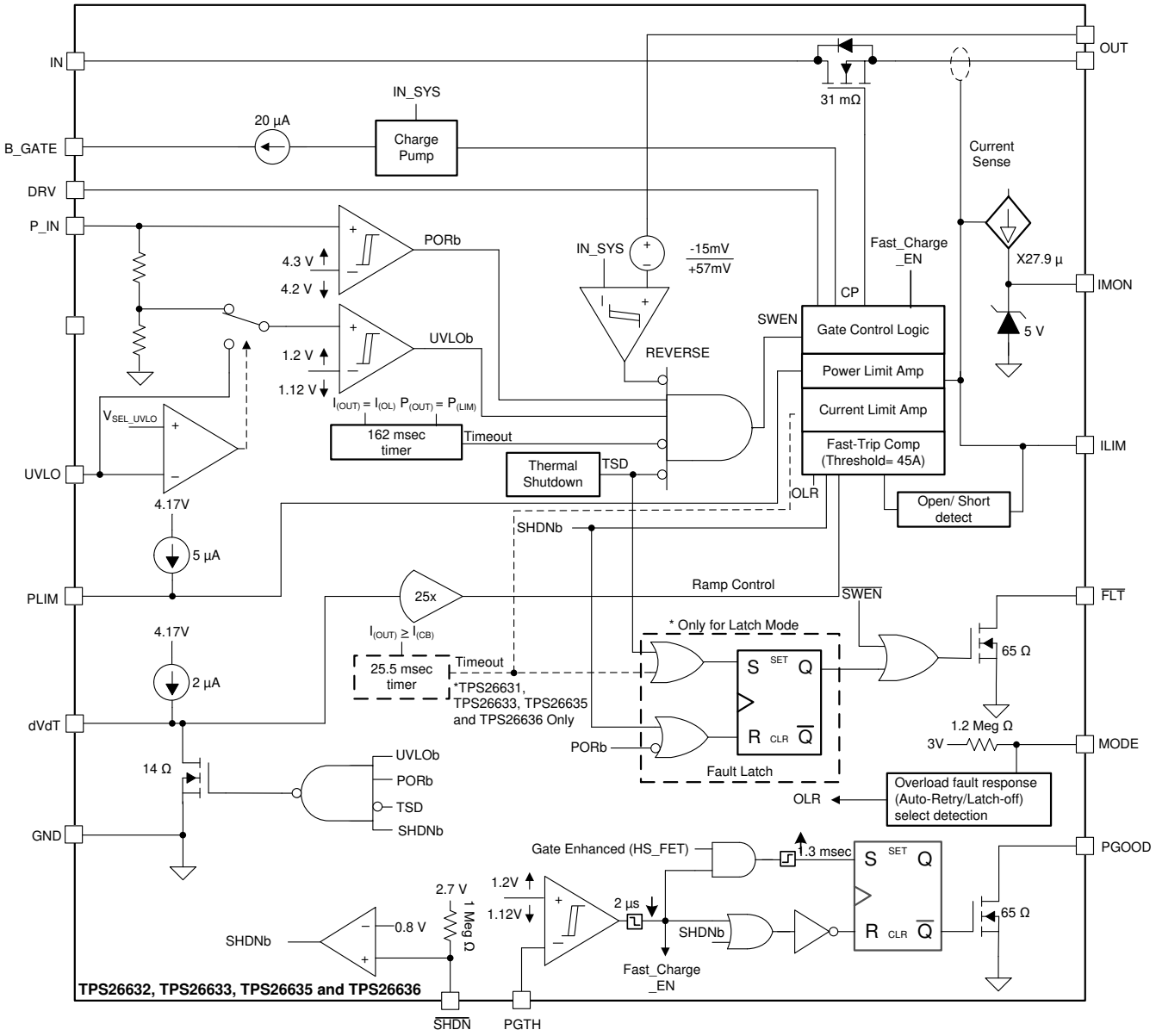


Figure 1-1. Functional Block Diagram

TPS2663 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VQFN Package

This section provides Functional Safety Failure In Time (FIT) rates for VQFN package of TPS2663 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	6
Package FIT Rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 700 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 HTSSOP Package

This section provides Functional Safety Failure In Time (FIT) rates for the HTSSOP package of TPS2663 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	18
Die FIT Rate	6
Package FIT Rate	12

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 700 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS2663 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT HIZ or no output	35%
OUT not in specification – voltage or timing	40%
IMON not in specification – current or timing	5%
PLIM not in specification – power or timing	5%
PGOOD/FLT fails to trip or false trip	5%
OUT stuck on	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS2663 (VQFN and HTSSOP package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Capacitors are installed on IN and OUT pins.
- Resistor is installed on ILIM pin.
- Resistors are installed on UVLO and OVP pin to set the UVLO and OVP set-points.

4.1 VQFN Package

Figure 4-1 shows the TPS2663 pin diagram for the VQFN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2663 data sheet.

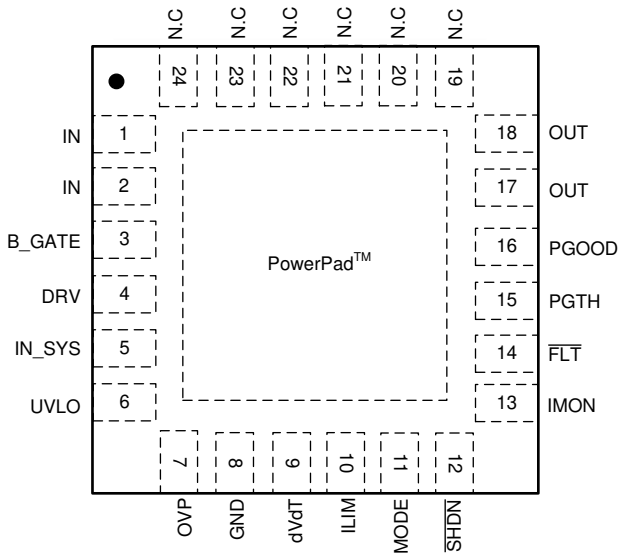


Figure 4-1. TPS26630, TPS26631 Pin Diagram (VQFN) Package

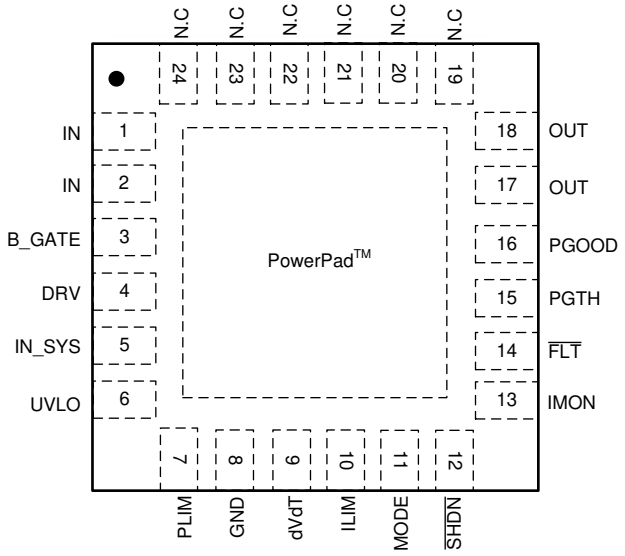


Figure 4-2. TPS26632, TPS26633, TPS26635 Pin Diagram (VQFN) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1,2	Device unpowered. Device not functional.	B
B_GATE	3	Potential device damage	A
DRV	4	Potential device damage	A
IN_SYS	5	Device unpowered. Device not functional.	B
UVLO	6	UVLO protection is triggered. Device turns off the internal FET.	B
OVP or PLIM	7	Over-voltage protection or power limiting does not function.	B
GND	8	No effect. Normal operation.	D
dVdT	9	Device does not power up.	B
ILIM	10	Device does not power up.	B
MODE	11	Device provides auto-retry behavior for over-current events as per device functional modes in data sheet.	D
$\overline{\text{SHDN}}$	12	Device is disabled.	B
IMON	13	Current monitor function is not available.	B
$\overline{\text{FLT}}$	14	Fault function is not available.	B
PGTH	15	PGOOD function is not available.	B
PGOOD	16	PGOOD function is not available.	B
OUT	17, 18	Device enters into current limiting operation.	B
NC	19, 20, 21, 22, 23, 24	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1,2	Device unpowered. Device is not functional.	B
B_GATE	3	Reverse current blocking and Reverse polarity protection are not functional.	B
DRV	4	Reverse current blocking and Reverse polarity protection are not functional.	B
IN_SYS	5	Device unpowered. Device is not functional.	B
UVLO	6	Device functionality undetermined. Device may turn off / power down.	B
OVP or PLIM	7	TPS26630, TPS26631: over-voltage protection function is not determined. Device may turn off the internal FET. TPS26632, TPS26633, TPS26635: output power limit is set to power more than 400 W.	B
GND	8	Device unpowered. Device is not functional.	B
dVdT	9	Device provides slew rate 24 V/500 µs on output.	D
ILIM	10	Internal FET is turned off. Output is not powered up.	B
MODE	11	Device provides latch-off behavior for over-current events as per device functional modes in data sheet.	D
$\overline{\text{SHDN}}$	12	No effect. Normal operation.	D
IMON	13	No effect. Normal operation.	D
$\overline{\text{FLT}}$	14	No effect. Normal operation.	D
PGTH	15	PGOOD might not function.	B
PGOOD	16	No effect. Normal operation.	D
OUT	17, 18	No power or current provided to load.	D
NC	19, 20, 21, 22, 23, 24	No effect. Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1,2	IN to B_GATE: Potential device damage	A
B_GATE	3	B_GATE to DRV : Potential device damage	A
DRV	4	DRV to IN_SYS : Potential device damage	A
IN_SYS	5	IN_SYS to UVLO: under-voltage protection does not function.	B
UVLO	6	UVLO to OVP/PLIM: potential device damage if UVLO voltage is more than 5.5 V.	A
OVP or PLIM	7	OVP/PLIM to GND: over-voltage protection or Power limiting does not function.	B
GND	8	GND to dVdT: device unpowered. Device not functional.	B
dVdT	9	dVdT to ILIM: device can go into current limit operation.	B
ILIM	10	ILIM to MODE: device can go into current limit operation or Latch-off mode.	B
MODE	11	MODE to $\overline{\text{SHDN}}$: device can go into shutdown.	B
$\overline{\text{SHDN}}$	12	$\overline{\text{SHDN}}$ to IMON: device can go into shutdown.	B
IMON	13	IMON to $\overline{\text{FLT}}$: potential Device damage if $\overline{\text{FLT}}$ pin voltage is more than 5.5 V.	A
$\overline{\text{FLT}}$	14	$\overline{\text{FLT}}$ to PGTH : PGOOD does not function if $\overline{\text{FLT}}$ is low.	B
PGTH	15	PGTH to PGOOD : PGOOD does not function	B
PGOOD	16	PGOOD to OUT: Potential device damage when PGOOD is low and output is powered up.	A
OUT	17, 18	OUT to N.C: no effect. Normal operation.	D
NC	19, 20, 21, 22, 23, 24	NC to IN short or NC to NC short : No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to IN or IN_SYS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1,2	No effect. Normal operation.	D
B_GATE	3	Potential device damage	A
DRV	4	Potential device damage	A
IN_SYS	5	No effect. Normal operation.	D
UVLO	6	Under-voltage protection does not function.	B
OVP or PLIM	7	Potential device damage if supply voltage is more than 5.5 V.	A
GND	8	Short circuit of input supply.	B
dVdT	9	Potential device damage if supply voltage is more than 5.5 V.	A
ILIM	10	Potential device damage if supply voltage is more than 5.5 V.	A
MODE	11	Potential device damage if supply voltage is more than 5.5 V.	A
$\overline{\text{SHDN}}$	12	Potential device damage if supply voltage is more than 5.5 V.	A
IMON	13	Potential device damage if supply voltage is more than 5.5 V.	A
$\overline{\text{FLT}}$	14	Potential device damage if $\overline{\text{FLT}}$ pin is low.	A
PGTH	15	PGOOD does not function.	B
PGOOD	16	Potential device damage if PGOOD pin is low.	A
OUT	17, 18	Device does not limit power or current into load.	B
NC	19, 20, 21, 22, 23, 24	No effect. Normal operation.	D

4.2 HTSSOP Package

Figure 4-3 shows the TPS2663 pin diagram for the HTSSOP package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2663 data sheet.

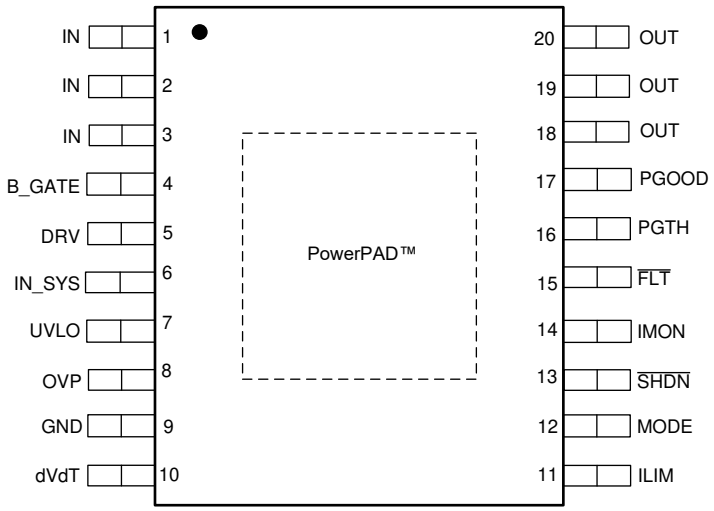


Figure 4-3. TPS26631 Pin Diagram (HTSSOP Package)

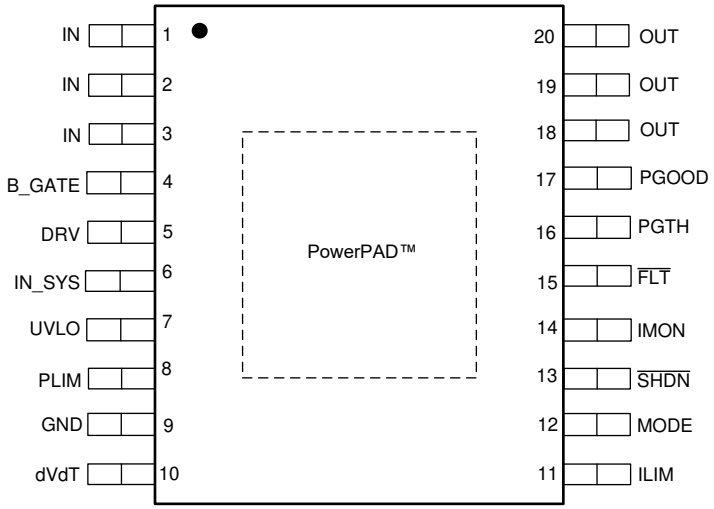


Figure 4-4. TPS26633, TPS26636 Pin Diagram (HTSSOP Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1, 2, 3	Device unpowered. Device not functional.	B
B_GATE	4	Potential device damage.	A
DRV	5	Potential device damage.	A
IN_SYS	6	Device unpowered. Device not functional.	B
UVLO	7	UVLO protection is triggered. Device turns off the internal FET.	B
OVP or PLIM	8	Over-voltage protection or Power limit does not function.	B
GND	9	No effect. Normal operation.	D
dVdT	10	Device does not power up.	B
ILIM	11	Device does not power up.	B
MODE	12	Device provides auto-retry behavior for over-current events as per device functional modes in data sheet.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
$\overline{\text{SHDN}}$	13	Device is disabled.	B
IMON	14	Current monitor function is not available.	B
$\overline{\text{FLT}}$	15	Fault function not available.	B
PGTH	16	PGOOD does not function.	B
PGOOD	17	PGOOD does not function.	B
OUT	18, 19, 20	Device enters into current limiting operation.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1, 2, 3	Device unpowered. Device not functional.	B
B_GATE	4	Reverse current blocking and Reverse polarity protection are not functional.	B
DRV	5	Reverse current blocking and Reverse polarity protection are not functional.	B
IN_SYS	6	Device unpowered. Device not functional.	B
UVLO	7	Device functionality undetermined. Device may turn off / power down.	B
OVP or PLIM	8	TPS26631: over-voltage protection function is not determined. Device may turn off the internal FET. TPS26633, TPS26636 : Output power limit is set to power more than 400 W.	B
GND	9	Device unpowered. Device not functional.	B
dVdT	10	Device provides slew rate 24 V/500 µs on output at power up.	D
ILIM	11	Internal FET is turned off. Output is not powered up.	B
MODE	12	Device provides latch-off behavior for over-current events as per device functional modes in data sheet.	D
$\overline{\text{SHDN}}$	13	No effect. Normal operation.	D
IMON	14	No effect. Normal operation.	D
$\overline{\text{FLT}}$	15	No effect. Normal operation.	D
PGTH	16	PGOOD might not function.	B
PGOOD	17	No effect. Normal operation.	D
OUT	18, 19, 20	No power or current provided to load.	D

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1, 2, 3	IN to B_GATE : Potential device damage.	A
B_GATE	4	B_GATE to DRV : Potential device damage.	A
DRV	5	DRV to IN_SYS : Potential device damage	A
IN_SYS	6	IN_SYS to UVLO: under-voltage protection does not function.	B
UVLO	7	UVLO to OVP: potential device damage if UVLO voltage is more than 5.5 V.	B
OVP or PLIM	8	OVP or PLIM to GND: over-voltage protection does not function.	B
GND	9	GND to dVdT: device unpowered. Device not functional.	B
dVdT	10	dVdT to ILIM: device can go into current limit operation.	B
ILIM	11	ILIM to MODE: device can go into current limit operation or Latch-off mode.	B
MODE	12	MODE to $\overline{\text{SHDN}}$: device can go into shutdown.	B
$\overline{\text{SHDN}}$	13	$\overline{\text{SHDN}}$ to IMON: device can go into shutdown.	B
IMON	14	IMON to $\overline{\text{FLT}}$: potential Device damage if $\overline{\text{FLT}}$ pin voltage is more than 5.5 V.	A
$\overline{\text{FLT}}$	15	PGTH to $\overline{\text{FLT}}$: PGOOD does not function if $\overline{\text{FLT}}$ is low.	B
PGTH	16	PGTH to PGOOD : PGOOD does not function.	B
PGOOD	17	PGOOD to OUT: Potential device damage when PGOOD is low and output is powered up.	A
OUT	18, 19, 20	OUT to OUT: No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to IN or IN_SYS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1,2, 3	No effect. Normal operation.	D
B_GATE	4	Potential device damage	B
DRV	5	Potential device damage	B
IN_SYS	6	No effect. Normal operation.	D
UVLO	7	Under-voltage protection does not function.	B
OVP or PLIM	8	Potential device damage if supply voltage is more than 5.5 V	D
GND	9	Short circuit of input supply.	B
dVdT	10	Potential device damage if supply voltage is more than 5.5 V.	A
ILIM	11	Potential device damage if supply voltage is more than 5.5 V.	A
MODE	12	Potential device damage if supply voltage is more than 5.5 V.	A
$\overline{\text{SHDN}}$	13	Potential device damage if supply voltage is more than 5.5 V.	A
IMON	14	Potential device damage if supply voltage is more than 5.5 V.	A
$\overline{\text{FLT}}$	15	Potential device damage if $\overline{\text{FLT}}$ pin is low.	A
PGTH	16	PGOOD does not function.	B
PGOOD	17	Potential device damage if PGOOD pin is low.	A
OUT	18, 19, 20	Device does not limit power or current into load.	B

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