Functional Safety Information

TPS784-Q1
Functional Safety FIT Rate, FMD and Pin FMEA

Table of Contents

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1 Overview

This document contains information for the TPS784-Q1 (VSON and SOT-23 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the adjustable-version functional block diagram for reference.

Figure 1-2 shows the fixed-version functional block diagram for reference.

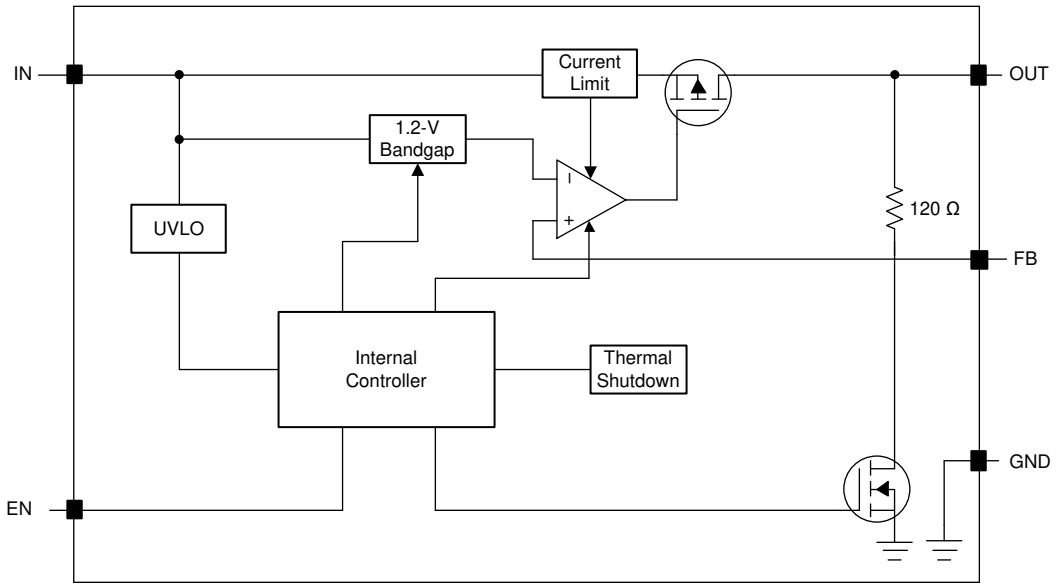

Figure 1-1. Functional Block Diagram (Adjustable Version)

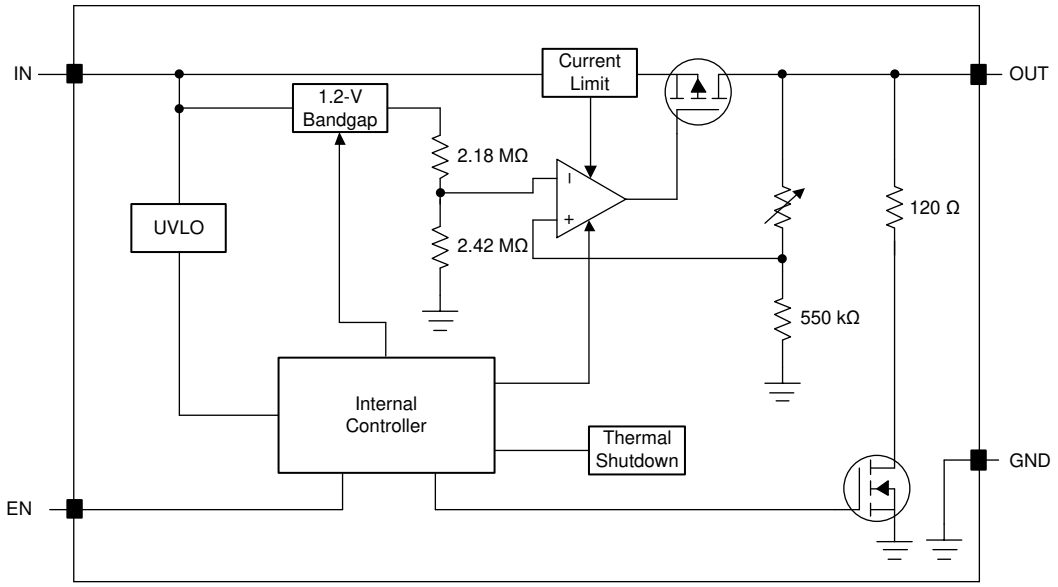

Figure 1-2. Functional Block Diagram (Fixed Version)

The TPS784-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS784-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	3
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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2.2 SOT-23 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 package of the TPS784-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	7
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS784-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output (output low)	50
Output high (following input)	10
Output not in specification	35
Short circuit, any two pins	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS784-Q1 (VSON and SOT-23 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, and Table 4-10)
- Pin open-circuited (see Table 4-3, Table 4-7, and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, and Table 4-12)
- Pin short-circuited to supply (see Table 4-5, Table 4-9, and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 VSON Package

Figure 4-1 shows the TPS784-Q1 pin diagram for the VSON package with a fixed output, and Figure 4-2 shows the TPS784-Q1 pin diagram for the VSON with an adjustable output. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS784-Q1 data sheet.

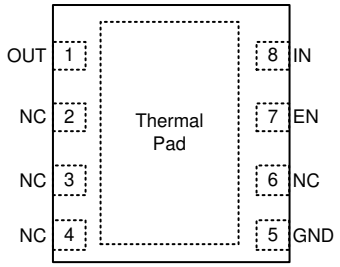

Figure 4-1. Pin Diagram (VSON Package), Fixed Version

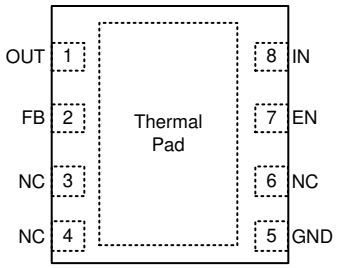

Figure 4-2. Pin Diagram (VSON Package), Adjustable Version

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC/FB	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	D/B
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
NC	6	No effect. Normal operation.	D
EN	7	The device is disabled, resulting in no output voltage.	B
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC/FB	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	D/B
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
NC	6	No effect. Normal operation.	D
EN	7	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC/FB (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) The output voltage is set to the internal reference voltage.	D/B
FB	2	NC (pin 3)	No effect. Normal operation.	D
NC	3	NC (pin 4)	No effect. Normal operation.	D
GND	5	NC (pin 6)	No effect. Normal operation.	D
NC	6	EN (pin 7)	No effect. Normal operation.	D
EN	7	IN (pin 8)	The device is always enabled. Peripherals connected to EN can be at risk of EOS.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device does not regulate.	B
NC/FB	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The absolute maximum rating for the FB pin (2 V max) can be violated, resulting in the device being destroyed. If the absolute maximum rating is not violated, the error amplifier closes the channel and there is no output voltage.	D/A
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	No output voltage. System performance depends on upstream overcurrent protection.	B
NC	6	No effect. Normal operation.	D
EN	7	The device is always enabled.	B
IN	8	No effect. Normal operation.	D

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4.2 VSON Package B Version

Figure 4-3 shows the TPS784-Q1 pin diagram for the VSON package with a fixed output, and Figure 4-4 shows the TPS784-Q1 pin diagram for the VSON with an adjustable output. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS784-Q1 data sheet.

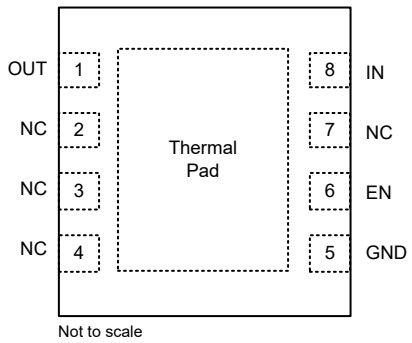

Figure 4-3. Pin Diagram (VSON Package B Version), Fixed Version

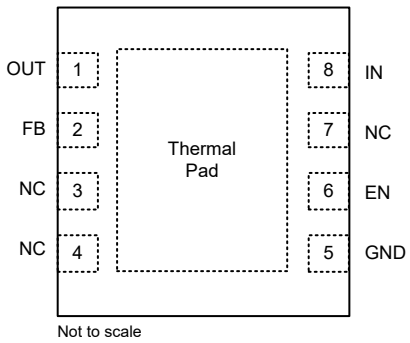

Figure 4-4. Pin Diagram (VSON Package B Version), Adjustable Version

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B
NC/FB	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	D/B
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	No effect. Normal operation.	D
EN	6	The device is disabled, resulting in no output voltage.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device output is disconnected from the load.	B
NC/FB	2	(Adjustable output.) No effect. Normal operation. (Fixed output.) The error amplifier input is not connected. The output voltage is indeterminate.	D/B
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
EN	6	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
NC	7	No effect. Normal operation.	D
IN	8	Power is not supplied to the device, resulting in no output voltage.	B

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Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	NC/FB (pin 2)	(Fixed output.) No effect. Normal operation. (Adjustable output.) The output voltage is set to the internal reference voltage.	D/B
NC/FB	2	NC (pin 3)	No effect. Normal operation.	D
NC	3	NC (pin 4)	No effect. Normal operation.	D
GND	5	EN (pin 6)	The device is always disabled, resulting in no output.	B
EN	6	NC (pin 7)	No effect. Normal operation.	D
NC	7	IN (pin 8)	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	The device does not regulate.	B
NC/FB	2	(Fixed output.) No effect. Normal operation. (Adjustable output.) The absolute maximum rating for the FB pin (2 V max) can be violated, resulting in the device being destroyed. If the absolute maximum rating is not violated, the error amplifier closes the channel and there is no output voltage.	D/A
NC	3	No effect. Normal operation.	D
NC	4	No effect. Normal operation.	D
GND	5	No output voltage. Either input supply is at 0 V, or an input fuse is blown.	B
EN	6	The device is always enabled.	B
NC	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

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4.3 SOT-23 Package

Figure 4-5 shows the TPS784-Q1 pin diagram for the SOT-23 package with a fixed output, and Figure 4-6 shows the TPS784-Q1 pin diagram for the SOT-23 with an adjustable output. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS784-Q1 data sheet.

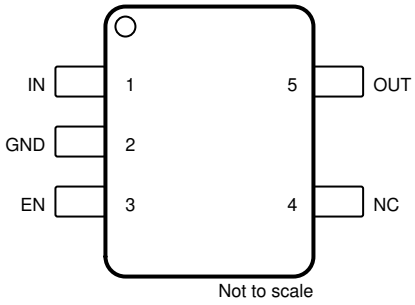

Figure 4-5. Pin Diagram (SOT-23 Package), Fixed Version

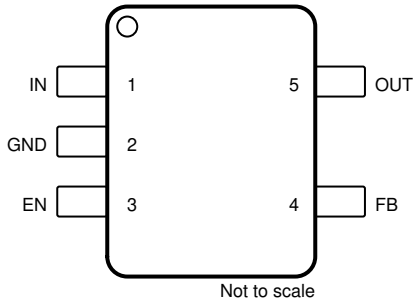

Figure 4-6. Pin Diagram (SOT-23 Package), Adjustable Version

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
GND	2	No effect. Normal operation.	D
EN	3	The device is disabled, resulting in no output voltage.	B
NC/FB	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) Output voltage is input voltage minus dropout voltage because the error amplifier drives the pass transistor gate to the rail.	D/B
OUT	5	Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Power is not supplied to the device, resulting in no output voltage.	B
GND	2	There is no current loop for the supply voltage. The device is not operational and does not regulate.	B
EN	3	The enable circuit is in an unknown state. The device can be enabled or disabled.	B
NC/FB	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) The error amplifier input is not connected. The output voltage is indeterminate.	D/B
OUT	5	The device output is disconnected from the load.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	GND (pin 2)	No output voltage. Either input supply is at 0 V, or an input fuse is blown.	B
GND	2	EN (pin 3)	The device is disabled, resulting in no output voltage.	B
NC/FB	4	OUT (pin 5)	(Fixed output.) No effect. Normal operation. (Adjustable output.) The output voltage is set to the internal reference voltage.	D/B

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Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No effect. Normal operation.	D
GND	2	No output voltage. System performance depends on upstream overcurrent protection.	B
EN	3	The device is always enabled.	B
NC/FB	4	(Fixed output.) No effect. Normal operation. (Adjustable output.) The absolute maximum rating for the FB pin (2 V max) can be violated, resulting in the device being destroyed. If the absolute maximum rating is not violated, the error amplifier closes the channel and there is no output voltage.	D/A
OUT	5	The device does not regulate.	B

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