Functional Safety Information

TCA9517-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TCA9517-Q1 (VSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

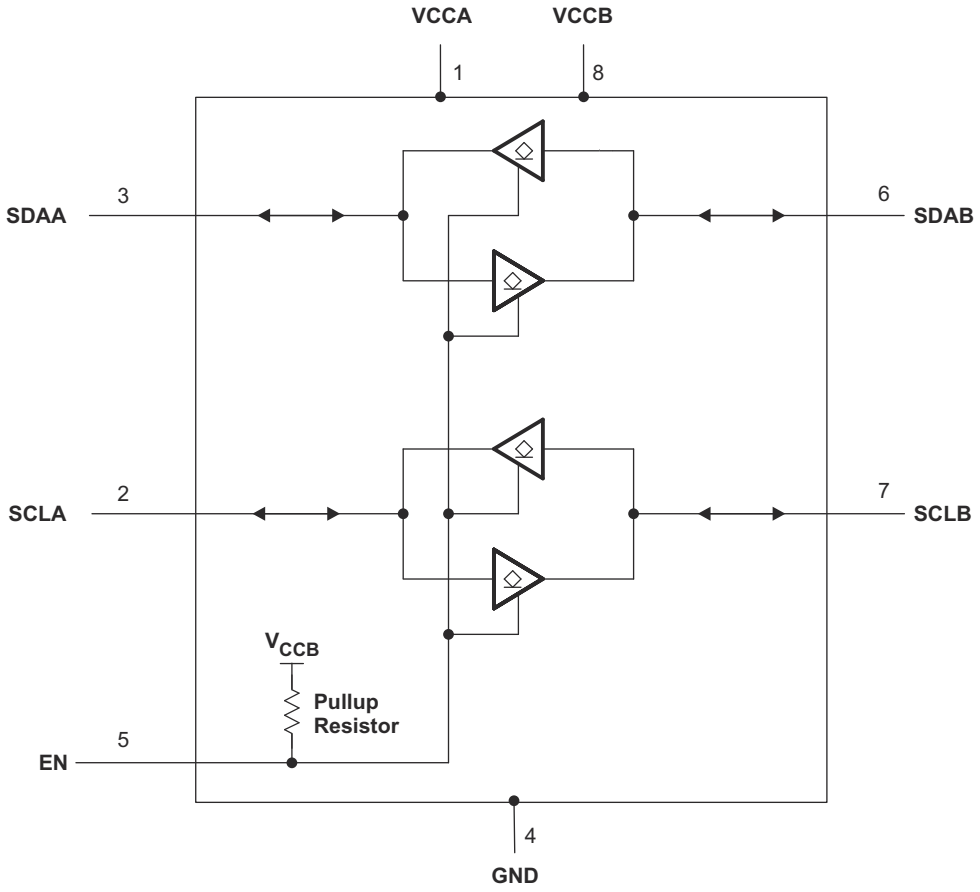

Figure 1-1. Functional Block Diagram

TCA9517-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCA9517-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCA9517-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
I2C control / communication error	25%
I/O configuration error	10%
I/O data bit error	65%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCA9517-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TCA9517-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCA9517-Q1 data sheet.

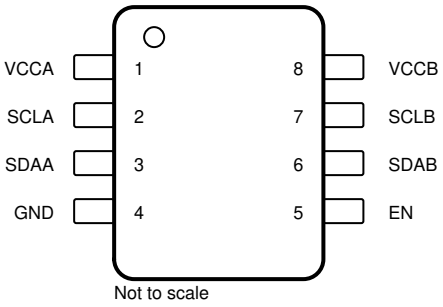

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption x
- Assumption y
- etc.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device may be held at RESET if VCCA does not power up above 0.8 V Concern due to this short is V_{CC} to GND from a system level, device is not expected to be damaged from this kind of short.	B
SCLA	2	SCL short to GND cause an I2C stuck bus. From a system level, the I2C bus is not functional. From device level, the device is not expected to be damaged from this short but functionality is lost.	B
SDA	3	SDA short to GND caused an I2C stuck bus. From a system level, the I2C bus is not functional. From device level, the device is not expected to be damaged from this short but functionality is lost.	B
GND	4	No expected concerns	D
EN	5	The device is disabled and be high impedance. Device funtionality is lost.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SDAB	6	SDA short to GND causes an I2C stuck bus. From a system level, the I2C bus is not functional. From device level, the device is not expected to be damaged from this short but functionality is lost.	B
SCLB	7	SCL short to GND causes an I2C stuck bus. From a system level, the I2C is not functional. From device level, the device is not expected to be damaged from this short but functionality is lost.	B
VCCB	8	Device may be held at RESET if VCCA does not poer up above 2.5 V Concern due to this short is V_{CC} to GND from a system level, device is not expected to be damaged from this kind of short.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device remains in a RESET or disabled state because VCCA is not above the under voltage lock out (UVLO). Device is high impedance between A and B sides. the device loses functionality, but should not be damaged.	B
SCLA	2	The device loses functionality, and may see an increase in supply current. Logic lows on SCL do not pass through this device.	B
SDAA	3	The device loses functionality, and may see an increase in supply current. Logic lows on SDA do not pass through this device.	B
GND	4	Device functionality is lost.	B
EN	5	Device may interrmittently become disabled as the Enable floats. Increased supply current may occur. Device should not be damaged, but functionality is lost.	B
SDAB	6	Device loses functionality, and may see an increase in supply current. Logic lows on SDA do not pass through the device.	B
SCLB	7	Device loses functionality, and may see an increase in supply current. Logic lows on SCL do not pass through the device.	B
VCCB		Device remains in a RESET or disabled state because VCCB is not above the under voltage lock out (UVLO). The device is high impedance between A and B sides. The device functionality is lost, but should not be damaged.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	SCLA	Potential damage to any device on this net that tries to pull the pin low.	B
SCL	2	SDA	I2C signal integrity becomes corrupted. Oscillations may occur on the I2C bus. Device does not function as intended.	B
SDAA	3	GND	I2C bus is stuck due to SDA being held at GND. I2C bus is not able to recover. The device does not function as intended.	B
EN	5	SDAB	The device is disabled intermittently as SDAB is driven low. The device may oscillate, and does not function as intended.	B
SDAB	6	SCLB	I2C signal integrity becomes corrupted. Oscillations may occur on the I2C bus. The device does not function as intended.	B
SCLB	7	VCCB	Potential damage to any device on this net that tries to pull the pin low.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	No affect.	D
SCLA	2	Potential harm to the I2C controller or any I2C target device that supports clock stretching. Voltage out low (VoL) likely to shift higher and create signal integrity issues on the I2C system.	B
SDAA	3	Potential harm to the I2C controller or any I2C target device on the net. Voltage out low (VoL) likely to shift higher and create signal integrity issues on the I2C system.	B
GND	4	Short to GND. No damage expected to device, but may cause GND shift or damage to supply.	B
EN	5	No damage expected to device, but device is held in an enabled state. Device may not be able to be disabled so device functionality is lost.	B
SDAB	6	Potential harm to the I2C controller or any I2C target device that supports clock stretching. Voltage out low (VoL) likely to shift higher and create signal integrity issues on the I2C system.	B
SCLB	7	Potential harm to the I2C controller or any I2C target device that supports clock stretching. Voltage out low (VoL) likely to shift higher and create signal integrity issues on the I2C system.	B
VCCB	8	No affect.	B

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