Functional Safety Information

UCC5350-Q1 UCC5390-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for UCC5350-Q1 (DWV SOIC-8 and D SOIC-8 package) and UCC5390-Q1 (DWV SOIC-8) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figures show the device functional block diagram for reference.

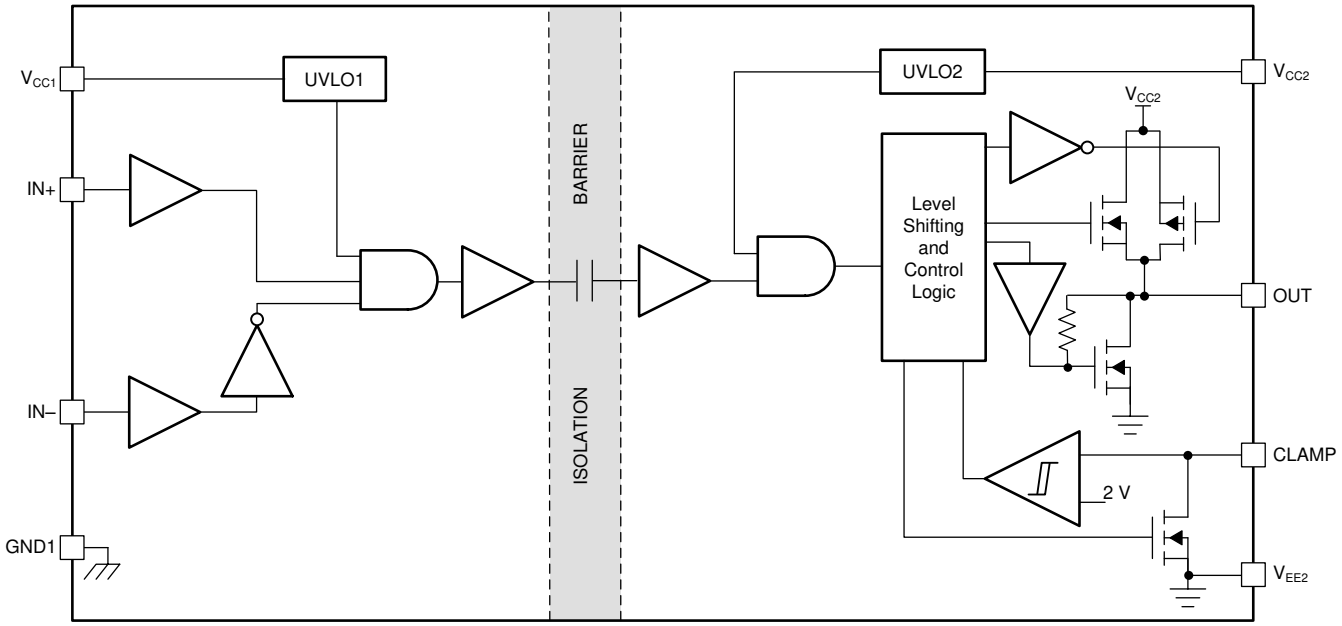

Figure 1-1. Functional Block Diagram of UCC5350-Q1

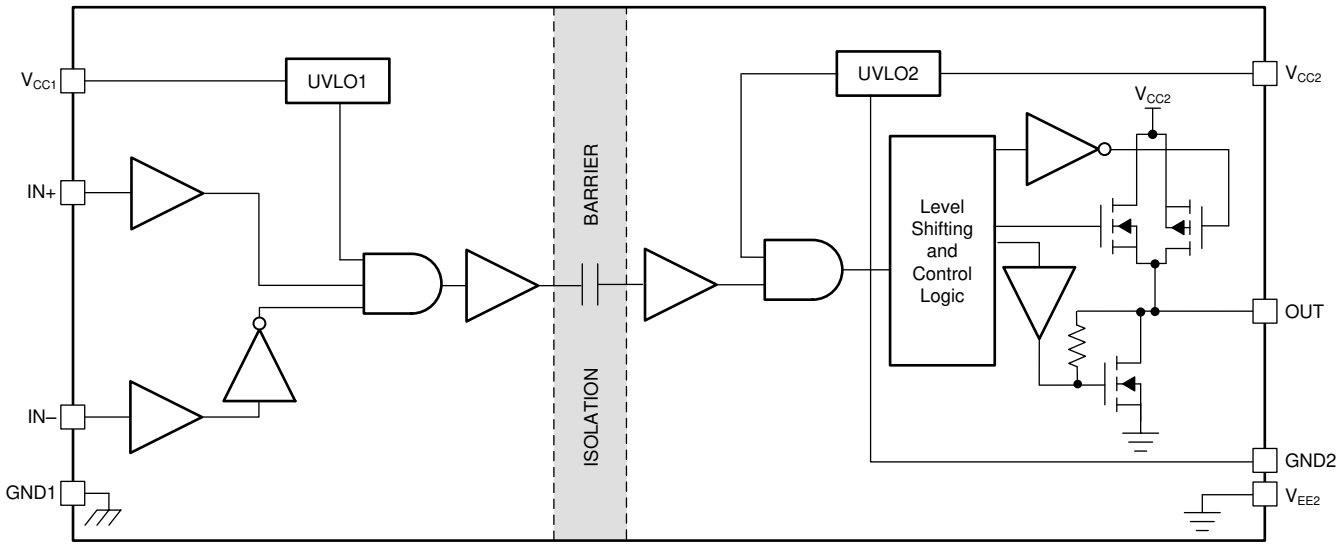

Figure 1-2. Functional Block Diagram of UCC5390-Q1

UCC5350-Q1 and UCC5390-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for UCC5350-Q1 and UCC5390-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11. Power dissipation: 100 mW
- Table 2-2 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11. Power dissipation: 300 mW
- Table 2-3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 Power dissipation: 100 mW

FIT IEC TR 62380 / ISO 26262 Power	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8.UCC5390-Q1 - DWV SOIC-8)	12,19,19
Die FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8.UCC5390-Q1 - DWV SOIC-8)	5,4,4
Package FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8.UCC5390-Q1 - DWV SOIC-8)	7,15,15

Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 Power dissipation: 300 mW

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8,UCC5390-Q1 - DWV SOIC-8)	15,24,24
Die FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8,UCC5390-Q1 - DWV SOIC-8)	7,8,8
Package FIT Rate (UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8,UCC5390-Q1 - DWV SOIC-8)	8,16,16

The failure rate and mission profile information in Table 2-1 and Table 2-2 come from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW, 300 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2 of UCC5350-Q1 - D SOIC-8, UCC5350-Q1 - DWV SOIC-8,UCC5390-Q1 - DWV SOIC-8

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	22 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for UCC5350-Q1 in Table 3-1 and UCC5390-Q1 in Table 3-2come from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution of UCC5350-Q1

Die Failure Modes	Failure Mode Distribution (%)
OUT stuck low	29%
OUT stuck high	29%
OUT level is outside of specified value	29%
UVLO not working	1%
CLAMP not working	12%

Table 3-2. Die Failure Modes and Distribution of UCC5390-Q1

Die Failure Modes	Failure Mode Distribution (%)
OUT stuck low	33%
OUT stuck high	33%
OUT level is outside of specified value	33%
UVLO not working	1%

The FMD excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the UCC5350-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the UCC5350-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC5350-Q1 data sheet.

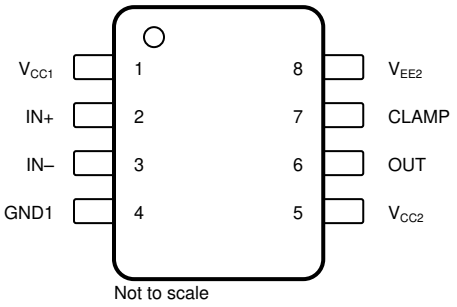

Figure 4-1. Pin Diagram

Figure 4-2 shows the UCC5390-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the UCC5390-Q1 data sheet.

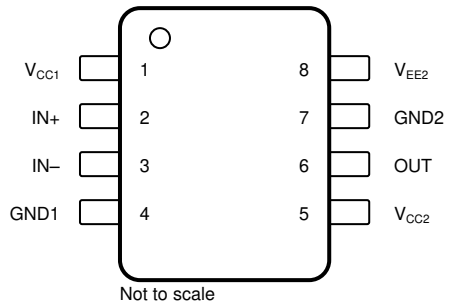

Figure 4-2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Primary side short to positive potential is short to Vcc1 and Vcc2 for the seondary.
- Pin short from #1 to #8 and #4 to #5 are not considered.
- Pin short that result in system supply fault cases are considered no effect to the driver.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Vcc1	1	Device is not powered.	D
IN+	2	OUT stuck low.	B
IN-	3	Cross conduction prevention does not work..	B
GND1	4	Short to same potential. No effect.	D
Vcc2	5	Seondary side unpowered.	D
OUT	6	OUT stuck low. Potential damage to OUT driver.	A
CLAMP(UCC5350-Q1)	7	CLAMP stuck low. Potentail damage to OUT and CLAMP driver.	A
GND2 (UCC5390-Q1)	7	Short to same potentail. No effect.	D
VEE2	8	Short to same potential. No effect.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Vcc1	1	Device is unpowered.	D
IN+	2	OUT stuck low.	B
IN-	3	OUT stuck low	B
GND1	4	Device is unpowered.	D
Vcc2	5	Device is unpowered.	D
OUT	6	OUT is disconnected from the power stage gate.	B
CLAMP(UCC5350-Q1)	7	Miller Clamp function is not available.	B
GND2 (UCC5390-Q1)	7	Device is unpowered. OUT stuck high.	B
VEE2	8	Device is unpowered. OUT stuck high.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
Vcc1	1	IN+	OUT follows IN- command.	B
IN+	2	IN-	OUT depends on IN+ and IN- driving capability.	B
IN-	3	GND1	Cross conduction prevention does not work..	B
Vcc2	5	OUT	OUT stcuk high. Potantail damage to OUT driver.	A
OUT(UCC5390-Q1)	6	GND2	OUT stcuk low. Potantail damage to OUT driver.	A
OUT(UCC5350-Q1)	6	CLAMP	No effect on the driver. The external gate resistor may be shorted out.	D
GND2(UCC5390-Q1)	7	VEE2	System supply short. No effect to the driver.	D
CLAMP (UCC5350-Q1)	7	VEE2	CLAMP stuck low. Potential damage to OUT driver.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Vcc1	1	No effect. Short to same potentail.	D
IN+	2	OUT follows IN- command.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	3	OUT stuck low.	B
GND1	4	Device is unpowered.	D
Vcc2	5	No effect. Short to same potentail.	D
OUT	6	OUT stuck high. Potential damage to OUT driver.	A
CLAMP(UCC5350-Q1)	7	CLAMP stuck high. Potential damage to OUT and CLAMP driver.	A
GND2 (UCC5390-Q1)	7	Device is unpowered.	D
VEE2	8	Device is unpowered.	D

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