SN74LV8T574-EP Enhanced Product Qualification and Reliability Report



ABSTRACT

TI Device: SN74LV8T574-EP

DLA VID: V62/25615

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication processes and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers. TI Enhanced Products are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures. Texas Instruments Enhanced Products are certified to meet GEIA-STD-0002-1 Aerospace Qualified Electronic Components.

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Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified devices through *Qualification by Similarity* (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests are eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameters or package define which attributes are required to remain fixed for the QBS rules to apply. The attributes which are expected and allowed to vary are reviewed and a QBS plan is developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device is reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.



JESD22-A110⁽¹⁾

JESD22-A.118(1)

JESD22-A104⁽¹⁾

ANSI/J-STD-002

UL 94V-0 IEC standard 695-2-2

UL 1694

JESD22-B116

ASTM F-459 or TM2011

TM 2019

JESD22-A103(1)

J-STD-020(1)

Table 1-1. Enhanced Products New Device Qualification Matrix

Enhanced Products New Device Qualification Matrix (Note that qualification by similarity (qualification family) per JEDEC JESD47 is allowed) Sample Size Lots Description Condition (Allowed **Test Method** Required Rejects) N/A Per TI Design Rules Electromigration Maximum Recommended Operating Conditions N/A Maximum Recommended Operating Conditions N/A N/A Per TI Design Rules Wire Bond Life **Electrical Characterization** TI Data Sheet 10 3 N/A EIA/JESD22-A114 or HBM per TI Data sheet ANSI/ESDA/JEDEC JS-001 Electrostatic Discharge 3 units/voltage N/A Sensitivity EIA/JESD22-C101 or CDM per TI Data sheet ANSI/ESDA/JEDEC JS-002 Latch-up Per Technology 3(0) 1 EIA/JESD78 **Physical Dimensions** TI Data Sheet 5(0) 1 EIA/JESD22-B100 Thermal Impedance Theta-JA on board Per Pin-Package N/A EIA/JESD51 Bias Life Test 125°C / 1000 hours or equivalent 3 JESD22-A108(1) 45(0) Biased Humidity or 85°C / 85% / 1000 hours JESD22-A101(1) 77(0) 3 130°C / 85% / 96 hours or 110°C / 85% / 264 Biased HAST JESD22-A110⁽¹⁾ hours Extended Biased Humidity(2) 85°C / 85% / 2000 hours JESD22-A101(1)

130°C / 85% / 192 hours or 110°C / 85% / 528

130°C / 85% / 96 hours or 110°C / 85% / 264

-65°C to +150°C non-biased for 500 cycles or

or Method B - IEC standard 695-2-2

77(-)

77(0)

77(0)

22(0)

5(0)

5 units x 30(0)

bonds
5 units x 30(0)

bonds

5(0)

15(0)

12

1

3

3

1

1

3

3

3

3

1

hours

equivalent

Per wire size

Per wire size

Per die size

150 °C / 1000 hours

Surface Mount Only

Bake Preconditioning

Method A - UL 94V-0

or Method C - UL 1694

Extended Biased HAST(2)

Unbiased HAST

Solderability

Flammability

Bond Shear

Die Shear

Bond Pull Strength

High Temp Storage

Moisture Sensitivity

Temperature Cycle

⁽¹⁾ Precondition performed per JEDEC Std. 22, Method A112/A113.

⁽²⁾ For information only.

Technology Family FIT / MTBF Data

Mean Time Between Fails (MTBF) and Failures in Time (FIT) rates are device reliability statistics calculated based on data collected from Tl's internal reliability testing (life test).

TI's DPPM/FIT/MTBF Estimator Search Tool reports the generic data based on technology groupings and shows conditions under which the rates were derived. All terms used in the tool and definitions can be found on the TI reliability terminology page. Failure rates are summarized by technology and mapped to the associated material part numbers. The failure rates are highly dependent on the number of units tested, therefore, it is not recommended to compare failure rates.

TI DPPM/FIT/MTBF Estimator Search Tool webpage link:

www.ti.com/quality/docs/estimator.tsp

Device Family Qualification Data

TI's Qualification Summary Search Tool reports generic qualification data representative of the material sets, processes, and manufacturing sites used by the device family and may not include all of the testing performed for a specific EP device. Please see the Enhanced Products New Device Qualification Matrix above for the full suite of qualification testing performed to release Enhanced Product devices.

TI Qualification Summary Search webpage link:

www.ti.com/qualificationsummary/qualsumm/home

Ongoing Reliability Monitoring

TI periodically monitors the reliability of its products, wafer fab processes, and package technologies, through its Ongoing Reliability Monitor (ORM) program. The ORM program involves collecting environmental reliability stress data on representative sets of devices, processes and packages. The results from the ORM program are updated quarterly in this report.

TI Ongoing Reliability Monitoring Search webpage link:

www.ti.com/orm/home?actionId=2801.html

For additional information or technical support please contact the Texas Instruments Customer Support Center. For more information on TI Enhanced Products, click here.

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