User's Guide

TXU-EVM Evaluation Module User's Guide

ABSTRACT

The characteristics, operation, and use of the TXU-EVM Evaluation Module (EVM) is described in this user's guide. A complete printed-circuit board layout, schematic diagrams, and bill of materials are included in this document.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TXU-EVM is specifically designed to support the evaluation of the TXU family. This evaluation module (EVM) supports the customizable evaluation of TXU0104, TXU0204 and TXU0304 devices in the 12-pin VQFN package with a footprints to be optionally fitted with a 14-pin TSSOP package of the same device. Figure 1-1 shows how the PCB can be broken down into three sections with each section supporting one of the three TXU variations.

Each TXU variation is designed to support specific applicatoins. While all three variations are suited for GPIO translation, TXU0104 is best suited for GPIO translation where all data is traveling in the same direction. TXU0204 is best suited for UART and JTAG. While TXU0304 is best suited for SPI and I**2**S used to translate PCM data. Table 1-1 shows the comparison between the three TXU variations.

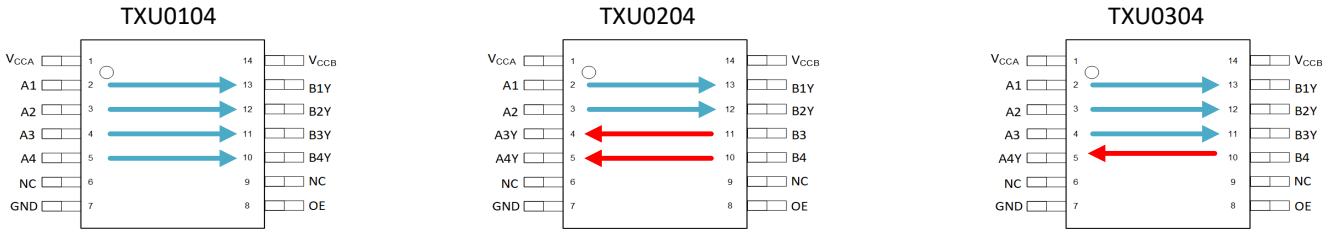

Figure 1-1. TXU Variations

Table 1-1. TXU Family Specializations

Part Number	GPIO	UART	JTAG	SPI	I^2S
TXU0104 (TXU0104-Q1*)(1)	✓				
TXU0204 (TXU0204-Q1*)(1)	✓	✓	✓		
TXU0304 (TXU0304-Q1*)(1)	✓			✓	✓

(1) -Q1 devices are not populated but can be supported.

1.1 Features

The TXU-EVM has the following feature:

- SMT footprints for configurable input and output loading
- Supports all three variants of the TXU family
- Fitted with bypass capacitors on both supply rails for more robust usage
- Individual ground pins on inputs and outpus for ease of use for differential probes
- OE headers with pullup resistors to either power supply
- Fitted with VQFN package of TXU family of devices
- Supports TSSOP packages of TXU family of devices

2 Hardware

2.1 PCB Overview

Figure 2-1 shws TXU-EVM. Table 2-1 shows the packages supported by the TXU-EVM.

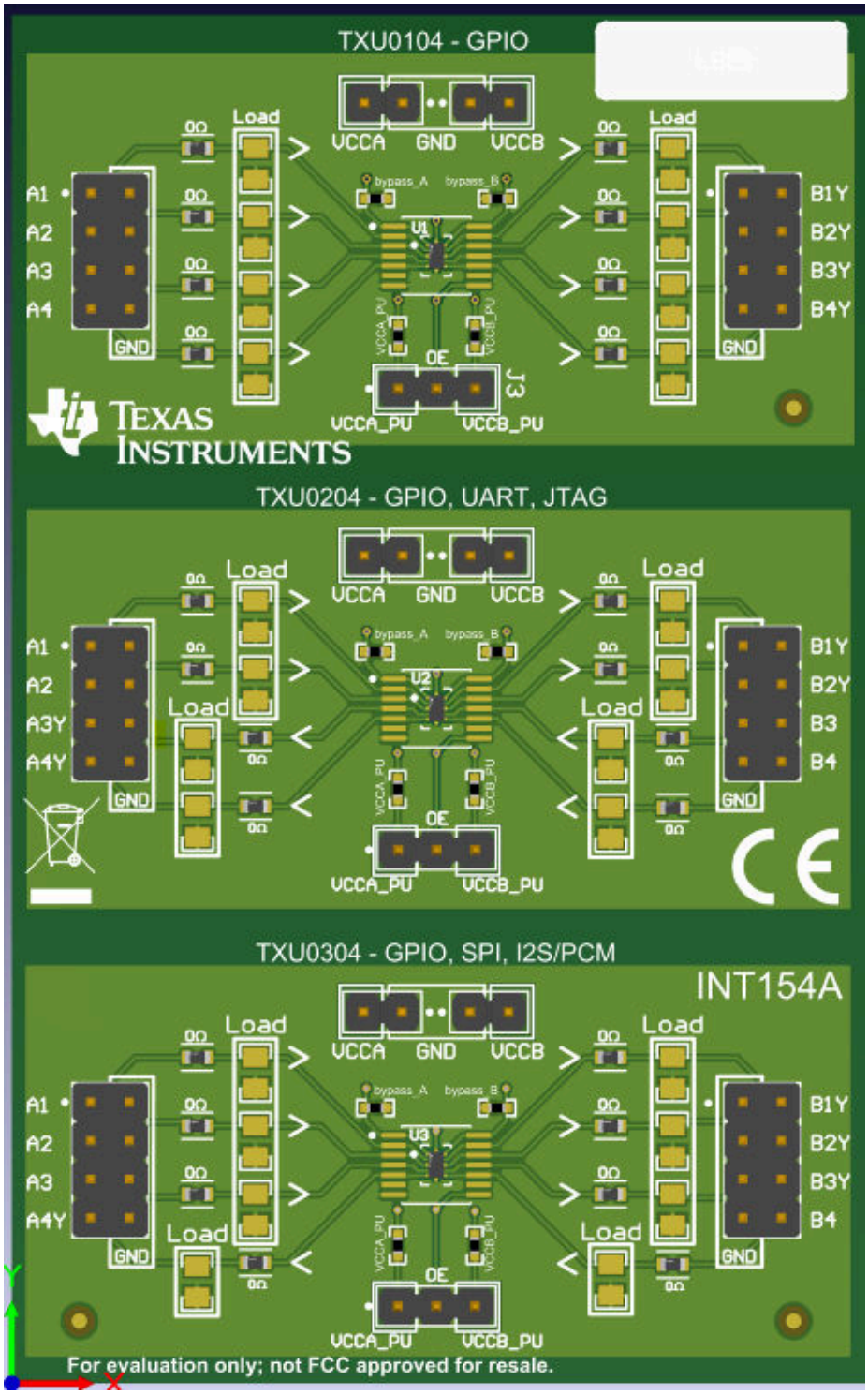

Figure 2-1. TXU-EVM

Table 2-1. TXU-EVM Packages and Devices Supported

Device	Package	Pins	Device Populated
TXU0104 (TXU0104-Q1*)(1)	DTR (X2QFN)	12	Yes
	PW (TSSOP)	14	No
TXU0204 (TXU0204-Q1*)(1)	DTR (X2QFN)	12	Yes
	PW (TSSOP)	14	No
TXU0304 (TXU0304-Q1*)(1)	DTR (X2QFN)	12	Yes
	PW (TSSOP)	14	No

(1) -Q1 devices are not populated but can be supported.

2.2 Headers

Each EVM board has header arrays for connection to the A and B side data pins, with ground oriented towards the device and the data headers closer to the board edges. Data pins inputs are marked *Ax* or *Bx* where x = 1, 2, 3 or 4. While outputs are marked *AxY* or *BxY* where x = 1, 2, 3 or 4 with the *Y* appended to indicate the pin as an output. Arrows are located in the middle section of the board which indicate the directionality of the pins from either A-side to B-side or vice versa.

All ground pins on their respective sections of the board are at the same ground potential and are boxed and labeled *GND* in the silkscreen of the EVM. All data I/O's in each TXU device have weak pulldowns integrated which allow for these headers to be left disconnected with a known state.

2.3 Voltage Supply

Supply headers are located at the top of each EVM for V_{CCA} and V_{CCB}. Table 2-2 denotes the operational voltage ranges for TXU devices. Figure 1-3. shows the location of the pin headers.

Table 2-2. TXU Device Voltage Supply Ranges

Devices	V_{CCA} range	V_{CCB} range
TXU0104(-Q1), TXU0204(-Q1), and TXU0304(-Q1)	1.1 – 5.5 V	1.1 – 5.5 V

2.4 Bypass Capacitors

0.1 µF Surface-Mount Technology (SMT) capacitors are populated near V_{CCA} and V_{CCB} device pins on each board (C1, C2, C11, C12, C13, and C14) and are labeled *bypass_A* and *bypass_B* respectively in association with each power rail. These are in place to smooth transient voltage supply spikes during start up and normal device operation.

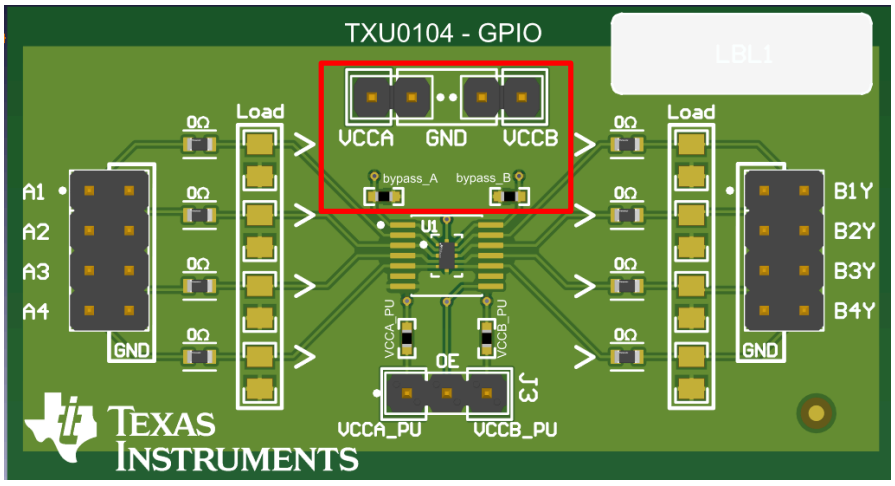

Figure 2-2. Supply Pin Headers with Bypass Capacitors

2.5 OE Select

A 3x1 100 mil header provides access to the Output Enable (OE) pins on the device. The 100 mil jumper is available for selecting a known state for the OE pin. The outer header pins access V_{CCA} or V_{CCAB} through a 10 kΩ resistor (0402). Because of $V_{CC(MIN)}$ circuitry, the OE pin on TXU device will defer to the lowest of the two supply voltages as reference for OE operation. The $V_{CC(MIN)}$ circuitry in conjunction with the over-voltage tolerant inputs allow the enable pin to be referenced to either V_{CCA} or V_{CCAB}.

An internal pull down resistor is present within the OE pin, allowing for the header to be disconnected without concern of the consequences of a floating CMOS input. Not pulling the OE to either V_{CCA} or V_{CCAB} will cause the OE pin to be pulled low and isolate your inputs from your outputs.

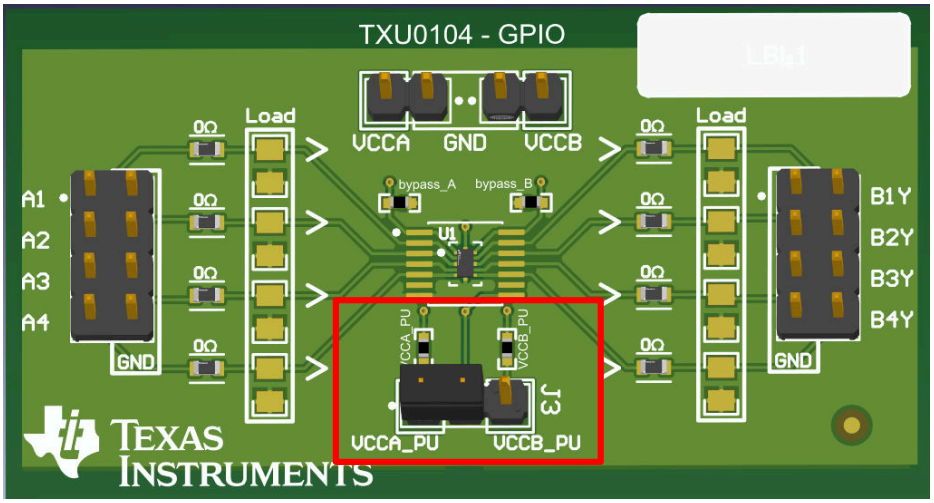

Figure 2-3. OE Pin Selection Jumper with Pullup Resistors

2.6 RC Loading

Each data I/O trace connects to an 0805 SMT pad with access to GND for a customizable load. Large pads were chosen for ease of access and the option to compose a load out of multiple, smaller, SMT components if desired. A 0 Ω resistor is located in series with each I/O line. Both the SMT pad and resistor can be used and modified for RC load tests, propagation delay, rise or fall time adjustments, input filtering, and so forth. Figure 2-4 shows the SMT pad and 0 Ω resistor locations. Pull down pads are boxed and labeled *Load* with the bottom pad being referenced to GND. Each input and output is fitted with individual GND pins for ease of use with differential probes.

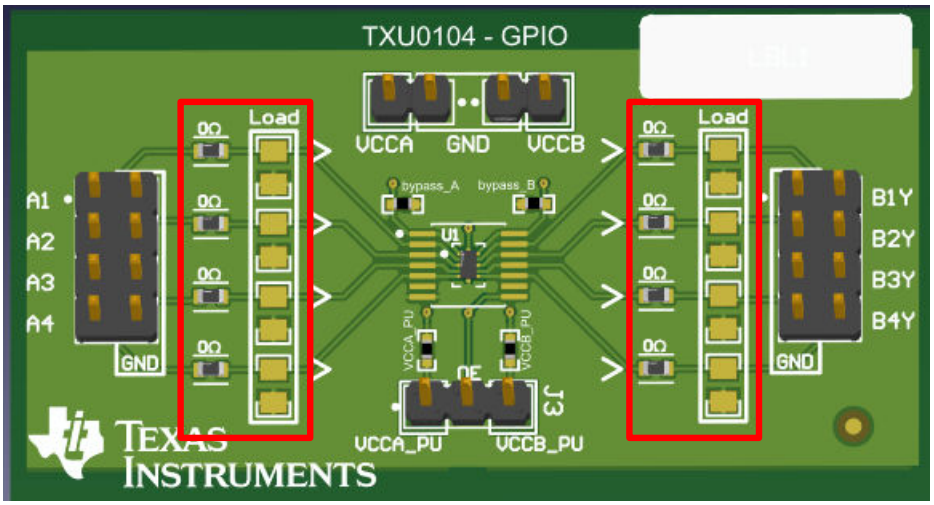

Figure 2-4. RC Loading

3 Board Layout

Figure 3-1 illustrates the TXU-EVM layout.

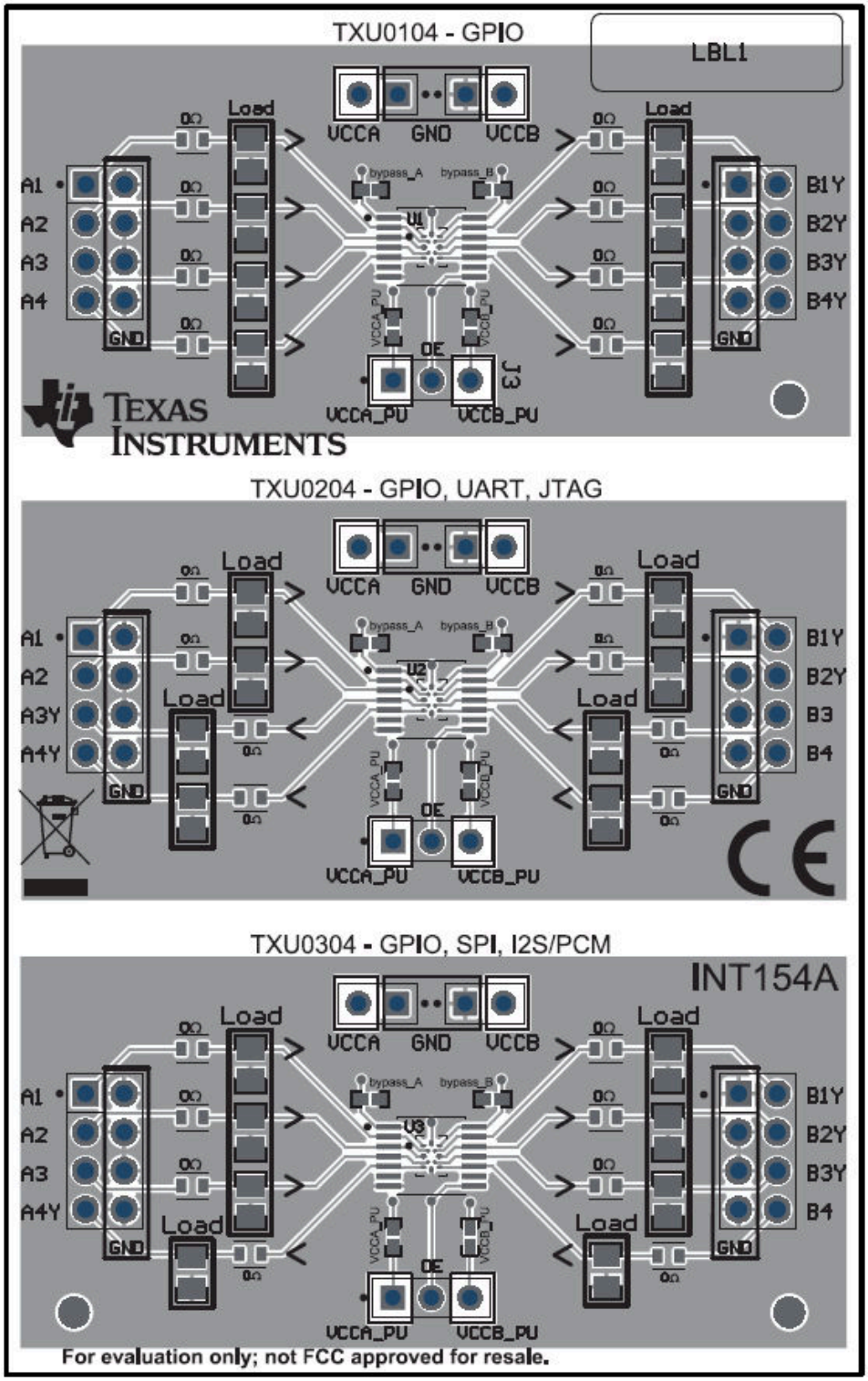

Figure 3-1. TXU-EVM Layout

4 Schematic and Bill of Materials

4.1 Schematic

Figure 4-1, Figure 4-2, and Figure 4-3 illustrate the TXU-EVM schematic.

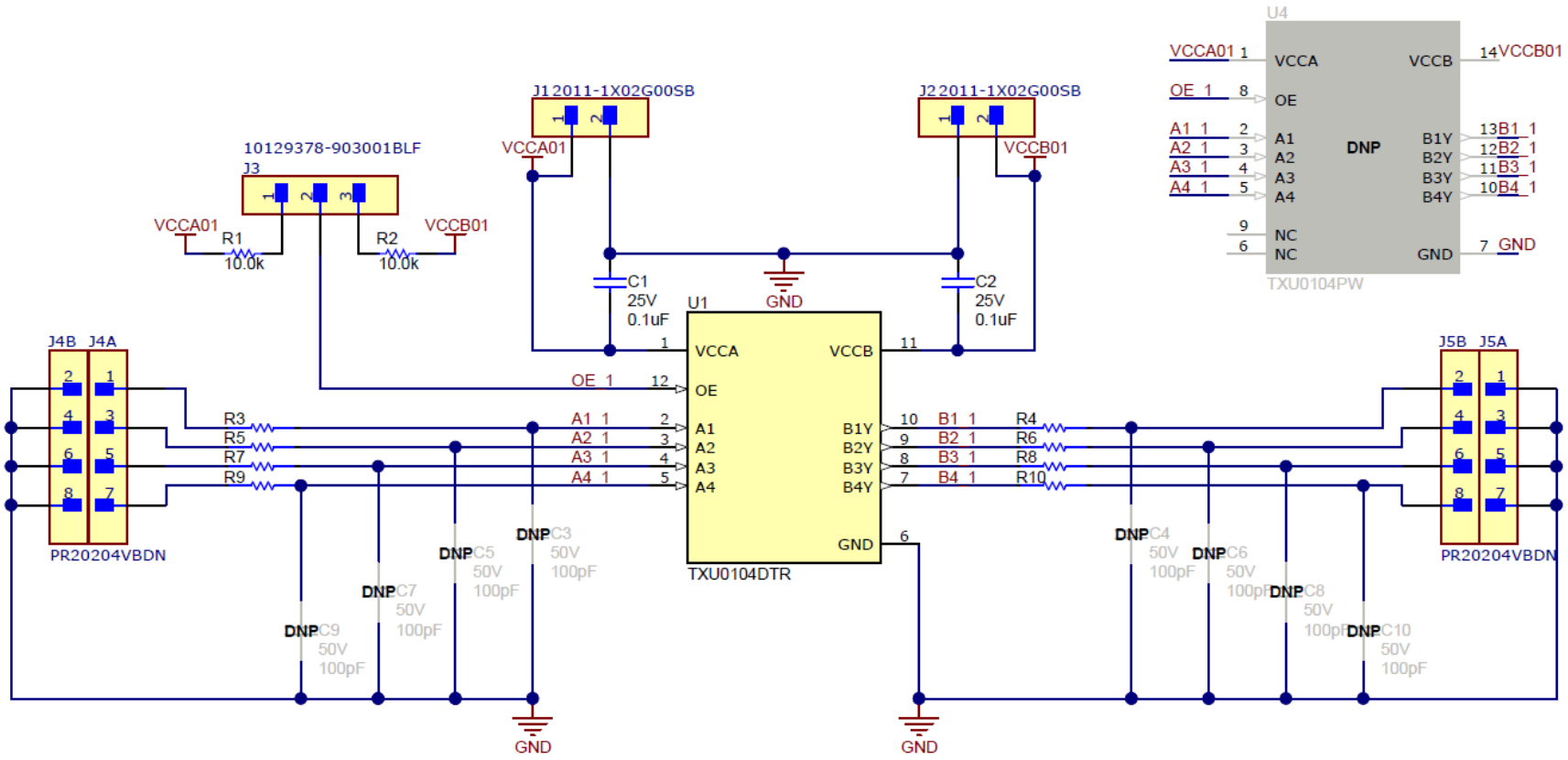

Figure 4-1. TXU0104

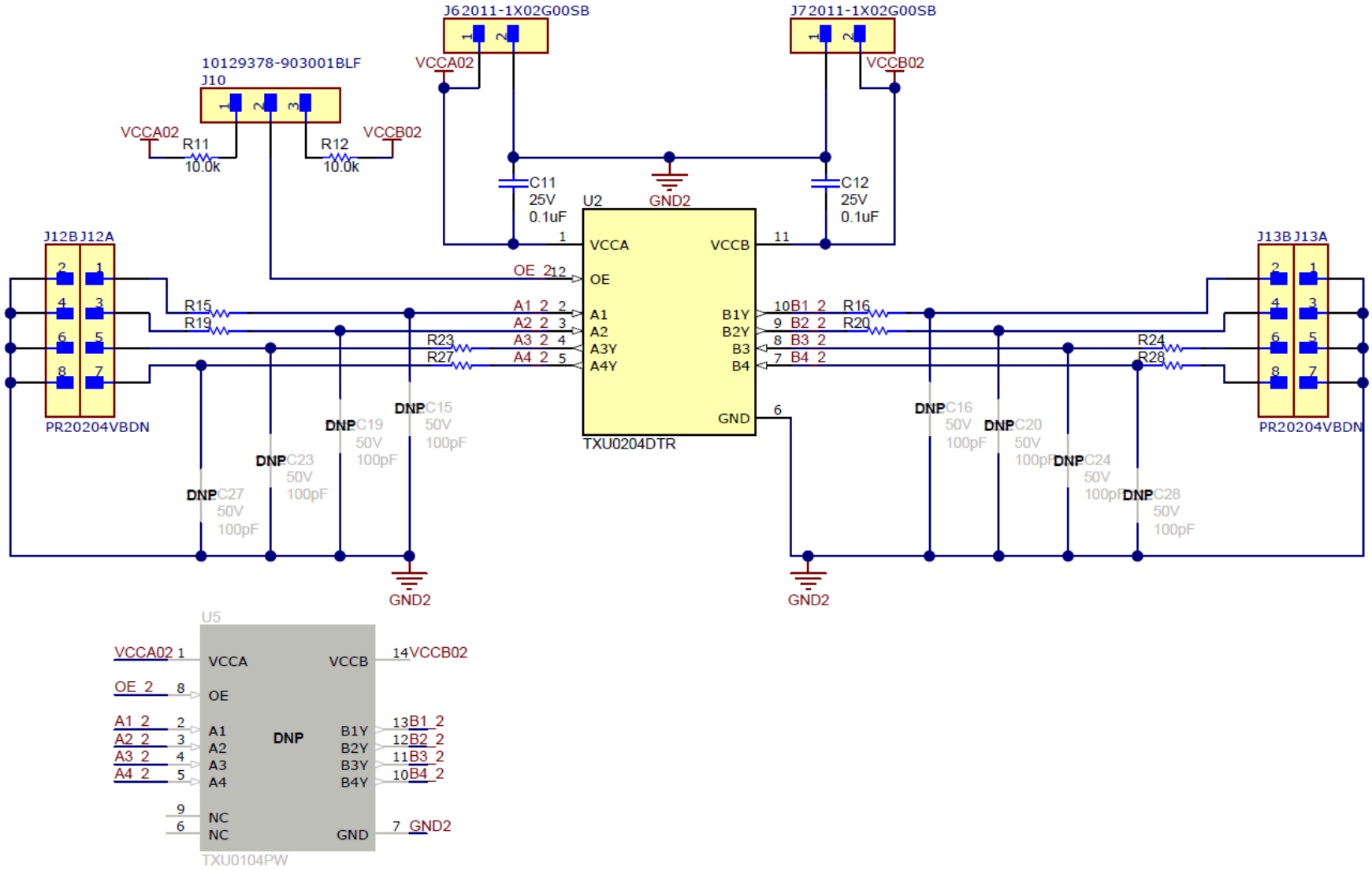

Figure 4-2. TXU0204

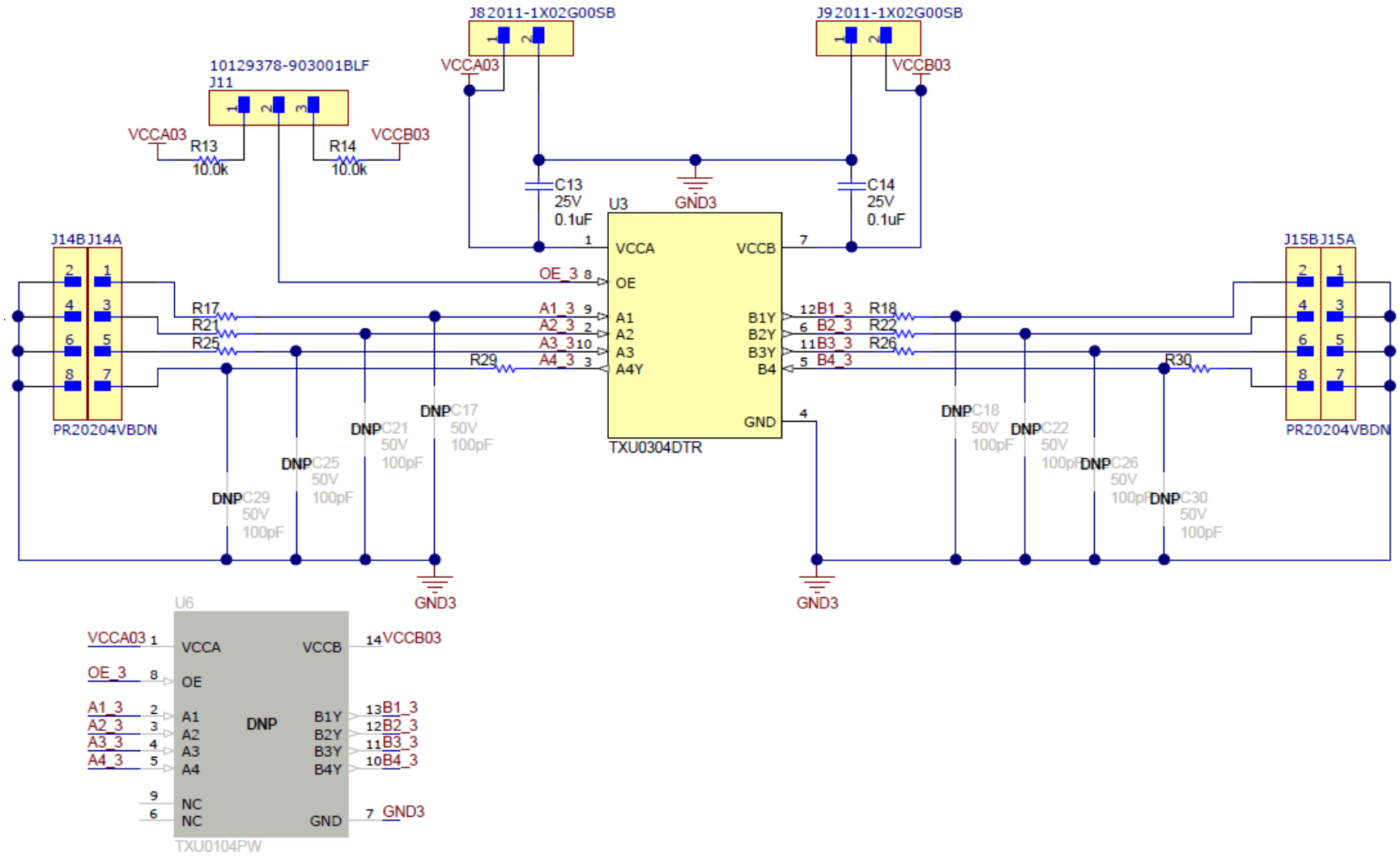

Figure 4-3. TXU0304

4.2 Bill of Materials

Table 4-1 lists the TXU-EVM bill of materials.

Table 4-1. TXU-EVM Bill of Materials

Designator	Quantity	Description	Part Number	Manufacturer
'C1, C2, C11, C12, C13, C14	6	'CAP, CERM, 0.1 µF, 25 V, ± 10%, X7R, 0402	'GRM155R71E104KE14D	'MuRata
'J1, J2, J6, J7, J8, J9	6	Header, 100mil, 2x1, Gold, TH	'2011-1X02G00SB	'Oupiin
'J3, J10, J11	3	Header, 100mil, 3x1, Gold, TH	'10129378-903001BLF	'Amphenol ICC
'J4, J5, J12, J13, J14, J15	6	Header, 100mil, 4x2, Gold, TH	'PR20204VBDN	'METZ CONNECT
'R1, R2, R11, R12, R13, R14	6	'RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	'RMCF0402FT10K0	'Stackpole Electronics Inc
'R3, R4, R5, R6, R7, R8, R9, R10, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30	24	'0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	'ERJ-3GEY0R00V	'Panasonic
U1	1	4-Bit Fixed Direction Voltage-Level Translator with SchmittTrigger Inputs, and Tri-State Outputs	'TXU0104DTR	Texas Instruments
U2	1	4-Bit Fixed Direction Voltage-Level Translator with SchmittTrigger Inputs, and Tri-State Outputs	TXU0204DTR	Texas Instruments
U3	1	4-Bit Fixed Direction Voltage-Level Translator with SchmittTrigger Inputs, and Tri-State Outputs	'TXU0304DTR	Texas Instruments

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