High-Performance Backplane Design With GTL+

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Abstract

Results from a system that demonstrates the performance of GTL+ devices in a backplane are provided. The Texas Instruments (TI™) GTL16622A is the example used in the design of the physical backplane. The TI backplane demonstration system is a useful tool for designers in understanding issues related to loading effects, termination, signal integrity, and data-transfer rate in a high-performance backplane environment. Simulation results are compared to laboratory measurements to validate the performance of TI GTL+ devices, and simulation results for the new TI GTL16612A in a very high-performance backplane are provided.

Introduction

High-performance backplane is becoming common terminology in the rapidly evolving data-communications market. Designers are developing innovative methods for multiplexing data to achieve higher throughput on the system bus or backplanes. High-speed backplanes that can handle large amounts of data are extremely important to high-performance systems.

The backplane is a physical and electrical interconnection between various modules in a system. Each module in the backplane communicates with other modules through the backplane bus. The backplane traces and the load capacitance affect signal integrity.

The discussion of the backplane demonstration system in this application report describes the various issues that should be considered while designing a backplane. The type of termination, backplane topology and layout, connector capacitance and stub lengths, along with the effect of the number of loads, all are investigated in this report. This report explains a demonstration backplane and its elements, followed by results that have been obtained using the TI GTL+ devices. HSPICE, a simulation tool, is used to model the performance of the system and to compare it to the hardware.

Background

In the past, increased throughput was achieved by increasing the frequency, or clock rate, or by increasing the bit width of the bus. Logic families that were used as backplane drivers included Advanced BiCMOS Technology (ABT), Fast CMOS Technology (FCT), Advanced CMOS Technology (ACT) and Backplane Transceiver Logic (BTL). These backplane drivers do not perform well in backplanes operating at frequencies over 33 MHz, but are sufficient for lower throughput requirements. With the trend toward higher system bandwidth requirements, into the hundreds of multimegabits per second, using a technology that supports these higher performance requirements is essential.

These increased speeds and performance requirements in designs created a need for higher-speed devices. Newer technologies developed by TI have helped to create devices that can drive these high-performance backplanes.

GTL/GTL+

Gunning Transceiver Logic (GTL), a technology invented by William Gunning at Xerox Corporation and standardized by JEDEC, was a low-swing input/output (I/O) driver technology that helped address these high-performance requirements. This technology was further modified by Intel™ and TI by increasing the voltage swing to create the GTL+ switching standard (see Figure 1). Subsequently, the standard was used by TI and Fairchild to create stand-alone devices to drive backplanes.

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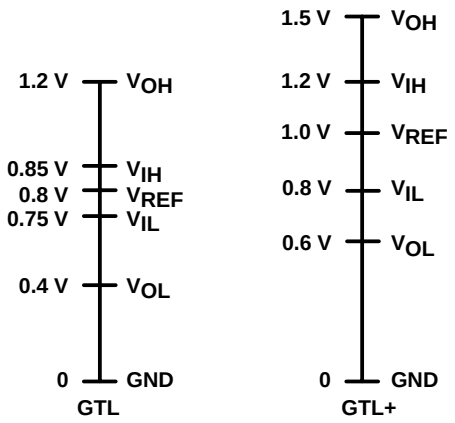

Figure 1. GTL/GTL+ Switching Levels

GTL+ achieves high performance with the help of the low signal voltage swing.[1] The typical swing for GTL+ is from 0.6-V low (V_{OL}) to 1.5-V high (V_{OH}) maximum. TI uses tighter threshold regions, V_{IH} at 1.05 V, V_{IL} at 0.95 V, and V_{OL} at 0.55 V, to provide better signal integrity in its stand-alone devices. This report demonstrates the performance of the newest TI GTL+ devices operating at clock rates of 100 MHz, providing bit rates of up to 10 Gbit/s in a 100-bit-wide backplane bus.

The TI GTL family offers edge control, which reduces signal noise and electromagnetic interference (EMI). The basic GTL output structure is an open-drain transistor, whereas the input is a differential receiver.[2] Also, the GTL I/Os have been designed to minimize their capacitance, an extremely important factor for distributed-load high-performance backplanes.

Backplane Design Considerations

This section covers the electrical elements of the backplane. The backplane bus connects the different modules in a backplane. The wires and traces on the bus and the traces on the modules are electrical elements that are a connection point for the various electrical modules. It is necessary to understand these electrical elements (such as impedance, capacitance, inductance, termination, connectors, stub lengths, vias, and driver and receiver characteristics) to design a successful backplane.

All of the above parameters contribute to the performance of the backplane. Backplanes can be categorized as low performance, medium performance, or high performance. A low-performance backplane can be modeled as a lumped load; medium- and high-performance backplanes must be viewed as a distributed load, by applying transmission-line theory.

With a low-performance backplane, the backplane driver sees the load as a lumped capacitance. The capacitive load in many cases is still distributed; however, it is modeled as a lumped load. This lumped model is used where the rise time of the signal is small compared to the transition time along the backplane. Here, only the final state matters, and bus performance is not the highest concern. The lumped capacitance is charged or discharged by the driver (see Figure 2) and is controlled by the RC time constant. The low-to-high signal transition is indicated by $1 - e^{-t/RC}$ and the high-to-low signal transition is of the form $e^{-t/RC}$. This lumped capacitance is referred to in the industry as a lumped load.

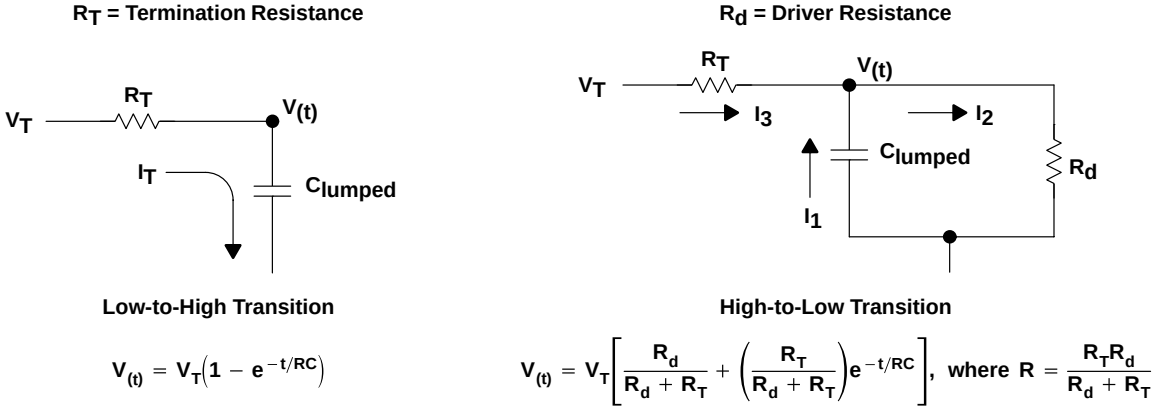

Figure 2. Lumped-Load Effects

Medium- and high-performance backplanes can be modeled as a distributed load. This is because performance drives a multidrop architecture, where the capacitance is distributed over the length of the backplane. To design an optimized medium- or high-performance backplane, a few concepts must be understood. These include the characteristic impedance of the backplane, (Z_o), the characteristic delay per unit length (τ_o), and the reflection coefficient (ρ), defined as the ratio of the amplitude of the reflected wave to the incident wave.

Figure 3 shows the transmission line as a distributed inductance and capacitance. The backplane driver charges the capacitance and is delayed by the inductance along the line. The signal sees the line as a characteristic impedance, given as:

$$Z_o = \sqrt{(L_o/C_o)} \quad \textbf{(1)}$$

Where:

L_o, C_o = distributed inductance and capacitance per unit length

The current flowing into the transmission line is of the form:

$$I = V_{in}/Z_o \quad \textbf{(2)}$$

The transition time or the time it takes for the signal to travel along the transmission line is:

$$\tau_o = \sqrt{(L_o/C_o)} \quad \textbf{(3)}$$

The intrinsic per-unit delay along the line is multiplied by the distance to give the overall delay across the line.

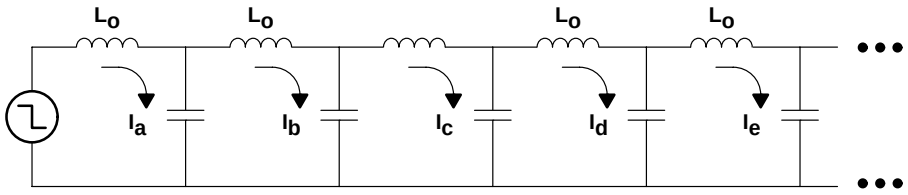

Figure 3. Transmission Line

The connectors on the backplane connect the backplane traces to branch transmission lines called stubs. These stubs are the communication ports between the backplane and the plug-in modules. These stubs, which have inductance and capacitance, change the overall impedance of the transmission line, and affect the signals that feed into the plug-in modules. This lumped capacitance changes the impedance and delay constants along the line by the following relationships:

$$Z_L = Z_o/\sqrt{(1 + C_d/C_o)} \quad \textbf{(4)}$$

$$\tau_d = \tau_o\sqrt{(1 + C_dC_o)} \quad \textbf{(5)}$$

Where:

C_d = added capacitance per unit length
C_o = intrinsic capacitance (as defined previously)

A point on the backplane where the impedance changes is called a discontinuity. A discontinuity on a backplane can occur if the drivers are placed too far from the backplane, there is improper termination, or the driver and receiver characteristics are not properly matched. At each point where a voltage wave that travels down the backplane meets a discontinuity, some of the signal is reflected, while the rest is transmitted along the backplane. The reflection coefficient determines the amount of signal that is reflected and is defined as the ratio of the reflected wave to the incident wave.

Figures 4 and 5 show the effects described above by using the GTL16622A to drive lumped and distributed loads, respectively. The lumped load consists of 25 Ω to 1.5 V, 30 pF to GND, whereas, the backplane (distributed load) consists of 16 slots separated by 0.875 in. Each load is approximately 14 pF.

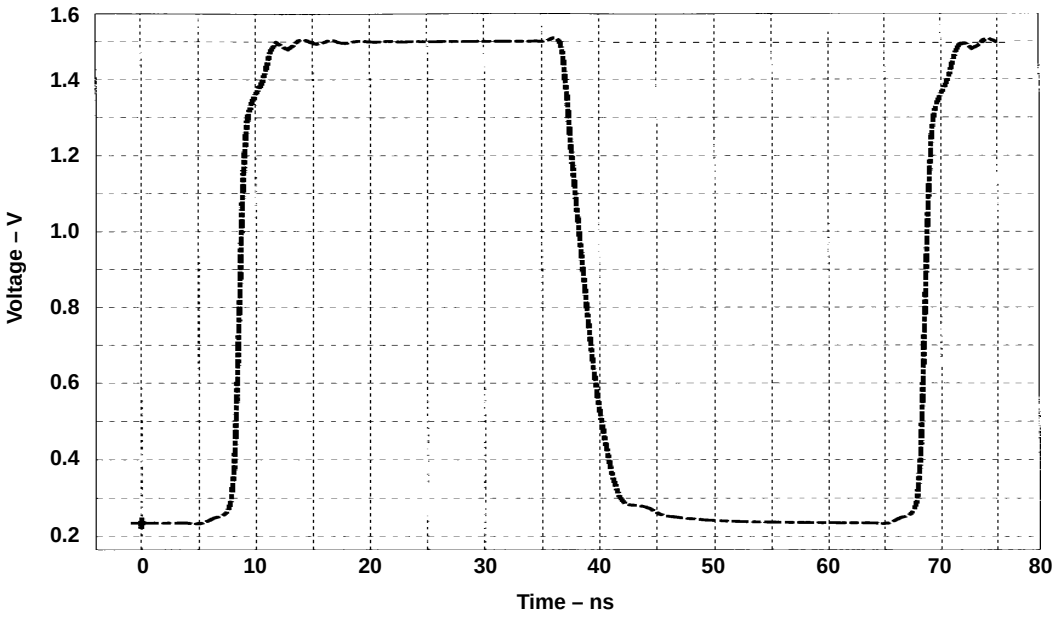

Figure 4. GTL16622A H-SPICE Simulation (Lumped Load, 33 MHz)

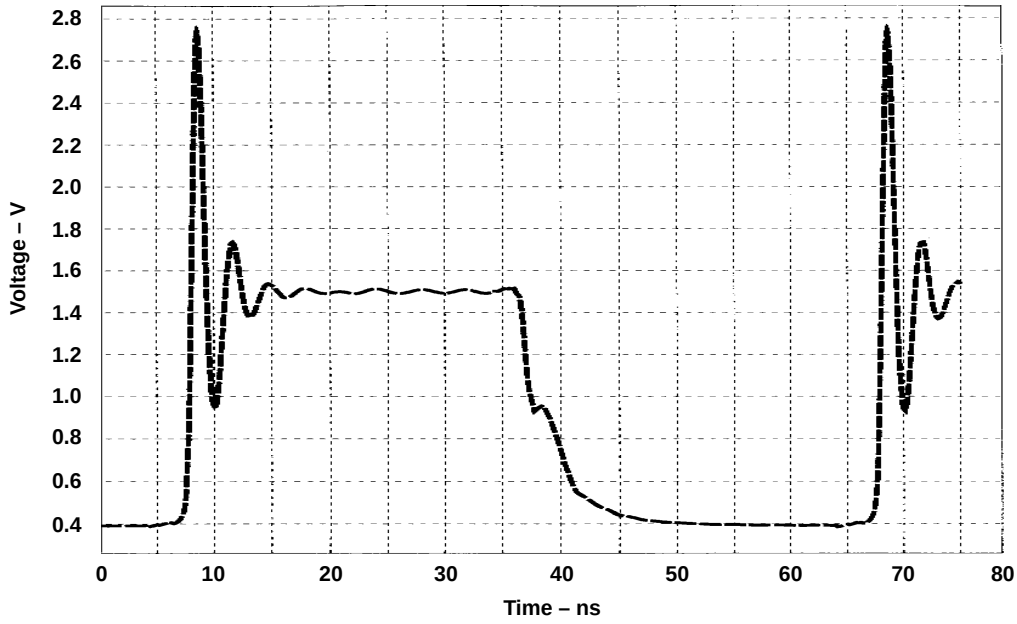

Figure 5. GTL16622A H-SPICE Simulation of a Backplane (Distributed Load, 33 MHz)

The added capacitance and inductance in the distributed load cause reflections that result in problems that include reduced noise margins.[3] In this case, the signal on the bus must settle before being sampled, hence, the bus settling time is required before valid data can obtained. Table 1 shows the comparison for the noise margins obtained for GTL and GTL+. GTL+ provides a wider noise margin than GTL, an important factor for designing signal-integrity-critical applications. In high-performance backplane designs, termination voltage, bus impedance, termination resistance, stub lengths, and driver and receiver characteristics must be controlled carefully to achieve good signal integrity, so that valid data can be presumed at the incident wave of the signal.

Table 1. Noise-Margin Comparison

DEVICE TYPE	NOISE MARGIN (mV)	
	UPPER	LOWER
GTL	350	350
GTL+	450	400

Another issue to consider in backplane design is crosstalk. Crosstalk, an effect of capacitive coupling in backplanes, can also result in false switching. Crosstalk between signal lines can be approximated as being inversely proportional to the distance between the signal lines and directly proportional to the distance between the signal lines and the ground plane. The most popular technique used to avoid crosstalk is fine-line technology that increases the distance between the signal lines while decreasing the distance between the signal line and the reference plane.

Backplane Demonstration System

The TI backplane demonstration board represents a typical industry backplane. The following section explains the elements of the demonstration backplane.

Architecture

Backplane Driver/Receiver (GTL16622A)

The GTL16622A 18-bit LVTTL-to-GTL/GTL+ bus transceiver translates between GTL/GTL+ signal levels and LVTTL or 5-V TTL signal levels. The device supports mixed-mode signal operation (3.3-V and 5-V signal) on the A port and control pins and is hot insertable with an output drive capability of 50 mA.[4] The device is used as both the driver and the receiver on the individual plug-in modules in the backplane.

Backplane Motherboard

The TI backplane demonstration board was constructed after studying various backplane loads. The 36-bit backplane consists of 14-in. traces with 16 slots separated by 0.875-in. pitch. Figure 6 shows the physical layout of the backplane board and its elements. The power supplies are represented as PS1 (5 V) and PS2 (3 V) and connectors by points P1 to P16. The connectors host the driver/receiver cards.

The clock drivers are U1, U2, and U3. U1 and U2 each distribute the clock to eight loads, while U3 is configured to supply the data at one-half the clock rate. The crystal oscillator (X1) supplies the clock and the data to the backplane board. The crystal oscillator can be changed to configure the clock rates at any frequency. The frequencies that have been used to test the demonstration board are 50 MHz, 66 MHz, 80 MHz, and 100 MHz. One of the plug-in cards is a driver, while the remaining cards are receivers. The GTL16622A is used as both driver and receiver. The position of the driver card on the backplane can be varied to study the loading effects and signal integrity on the backplane.

The 1.5-V termination voltage (V_{TT}) for GTL+ is from a 5-V regulated power supply. The 3.3-V power supply provides power to the GTL device on board. The voltage reference, V_{REF}, is generated from V_{TT}, using a simple voltage-divider circuit with an appropriate bypass capacitor (0.1 μF) placed as close as possible to the V_{REF} pin.[2] TI recommends placing the voltage-divider circuitry on each daughter card, because this eliminates the noise introduced by the backplane trace.

The intrinsic, unloaded, backplane trace impedance is 50 Ω and has a loaded impedance of 25 Ω with 16 loaded slots. The backplane is dc terminated using a 25-Ω resistor to V_{TT} to match the loaded impedance of the backplane. The 36-bit backplane is used to transmit data from the driver to each receiver card at the frequency of the crystal oscillator.

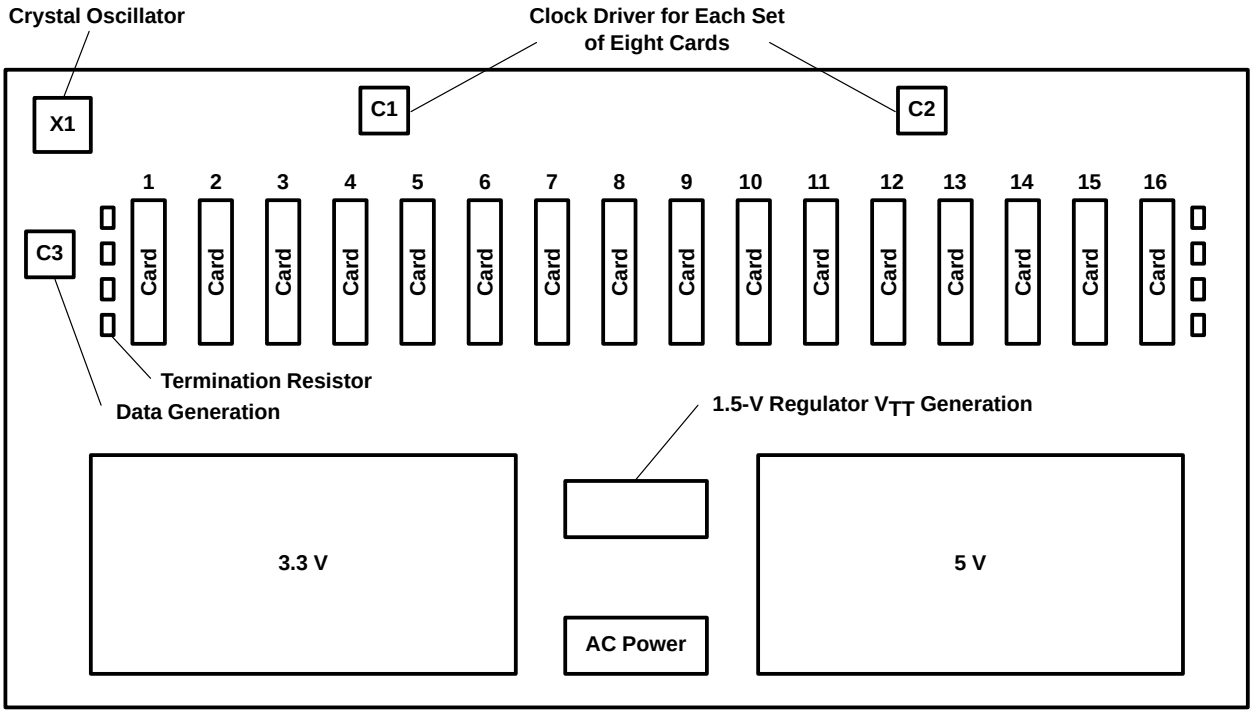

Figure 6. Backplane Demonstration Board Physical Layout

Interconnect and Impedance Calculations

Figure 7 is a graphical summary of the network that provides the physical dimensions of the backplane. Each element introduces additional capacitance on the board, which increases the loading on the backplane, eventually affecting signal integrity. The physical representation of the demonstration backplane shows the slots separated by 0.875 in. of backplane trace (B). There is a 0.0625-in. stub between the backplane trace and the connector (C), followed by approximately 1 in. of microstripline card stubs (D), and a total stub length of 1.0625 in. (as shown in the impedance calculator in Figure 8).

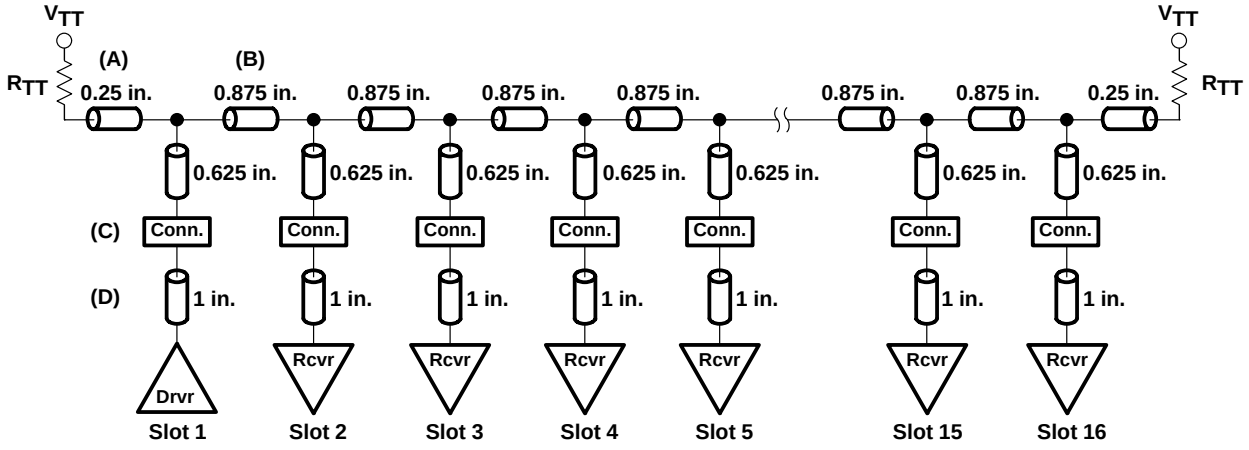

Figure 7. Backplane Physical Representation

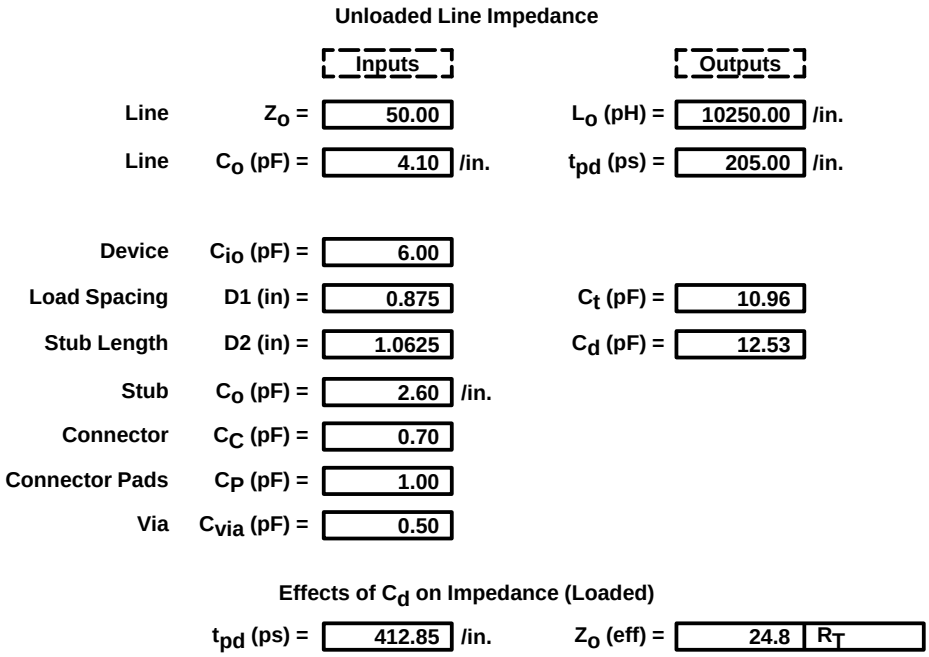

Figure 8. Impedance Calculator

The impedance calculator is a spreadsheet that is created using the previous equations to show the effects of distributed capacitance. The spreadsheet shows that the initial impedance of the 50-Ω backplane trace introduces a delay of 205 ps/in. (see equation 3) and has a C_o of 4.1 pF/in. The introduction of backplane loads increases the distributed capacitance (C_d) to 12.53 pF/in., which increases the propagation delay (t_{pd}) to 412.85 ps/in. and reduces the backplane impedance to 24.83 Ω (see equation 4). The backplane loading is a factor of the input/output capacitance of the driver or receiver (C_{io}), stub capacitance, via capacitance, and connector capacitance. Both ends of the backplane trace are terminated by a stub (A), using a 25-Ω pullup resistor to the termination voltage (V_{TT} = 1.5 V).[5]

Results

Laboratory data were taken using the demonstration backplane and compared to HSPICE simulation results to validate the performance of the GTL16622A on the backplane. Figure 7 is the reference to give the position of driver and receiver cards in the backplane. Results for TI's newest addition, the GTL16612A, demonstrate the throughput capability in a very high-performance backplane.

Laboratory

Figure 9 shows the laboratory results for the GTL16622A, with all 36 bits switching on the fully loaded backplane board with the driver card in slot 1. The worst-case signal was observed in the receiver card closest to the driver card (slot 2), while the best-case signal was seen in the receiver card farthest from the driver (slot 16). The throughput obtained at 50 MHz is 1.8 Gbit/s.

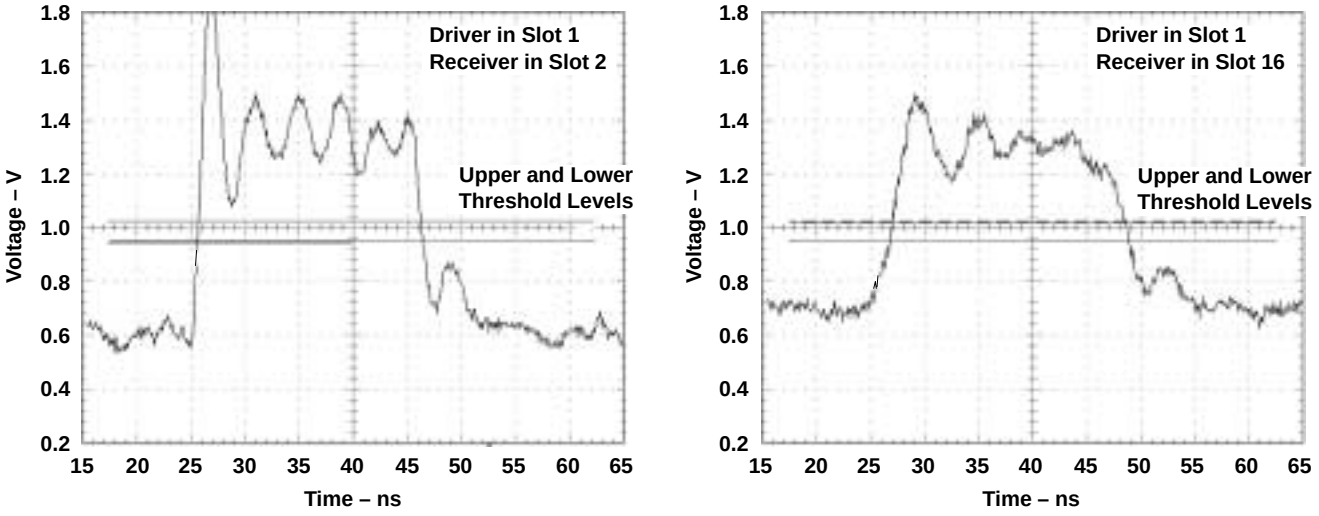

Figure 9. GTL16622A Signal Integrity (Laboratory Results)

Simulation

Figure 10 shows the HSPICE simulation results for the GTL16622A, which correlate closely with results observed in the laboratory with the demonstration hardware. The simulation results are observed after modeling the backplane using HSPICE for single-bit switching.

Figure 10. GTL16622A Signal Integrity (HSPICE Simulation Results)

The slot closest to the driver (slot 2) shows the worst-case ringing because it sees the fastest rise time of the IC driver compared to the slots that are farther away from the driver. The worst-case signal at slot 2 also is due to the effect of reflected energy that is maximum in the receiver closest to the driver.[3]

Correlation

Figure 11 shows laboratory versus simulation results for the GTL16622A on the demonstration board. The results shown are for the receiver at slot 2 (closest to the driver card). Here, as the frequency is increased, the time available for the data to be sampled decreases, making good signal integrity necessary at these high frequencies.

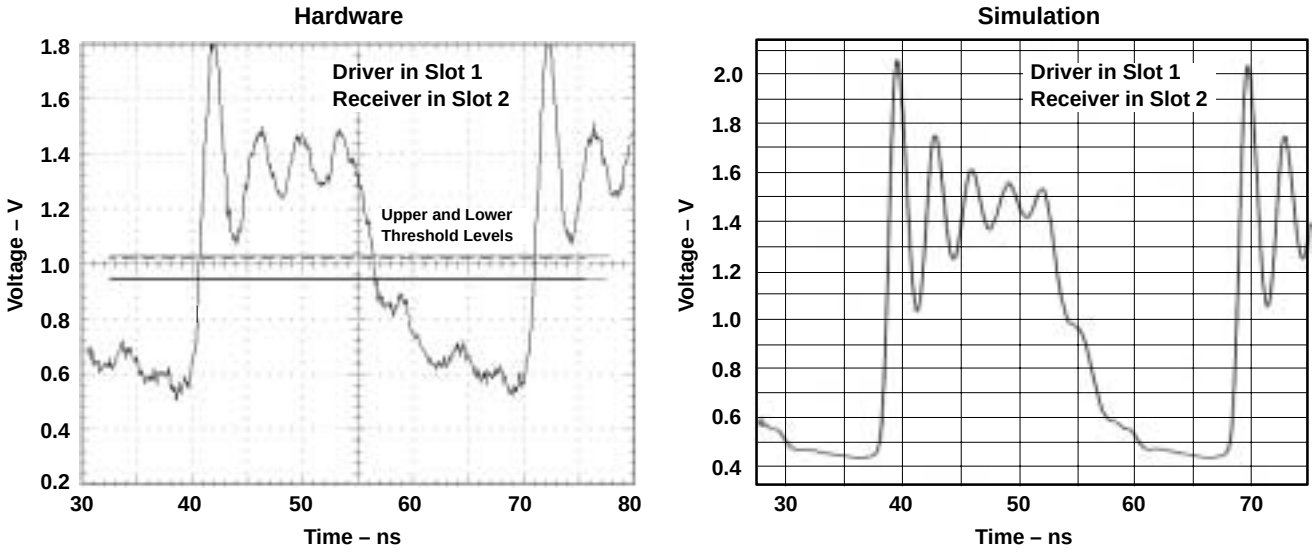

Figure 11. GTL16622A Signal Integrity (Hardware vs Simulation at 66 MHz)

Moving Forward With the GTL16612A

TI has continued to improve the characteristics and features of the GTL family to provide higher throughput rates at backplane frequencies up to 80 MHz. These higher frequencies allow designers to transmit increased amounts of data on their board, achieving high bit rates in their systems. The newest device in the GTL family, the GTL16612A, an improved version of the GTL16612, is capable of operating at frequencies as high as 80 MHz. The features of this device include output edge control (OEC™) on the rising and the falling edge, and optimization for high-performance distributed-load applications. Simulation results that provide a comparison between the GTL16622A and the GTL16612A are shown in Figures 12 and 13 at 50 MHz and 66 MHz, respectively.

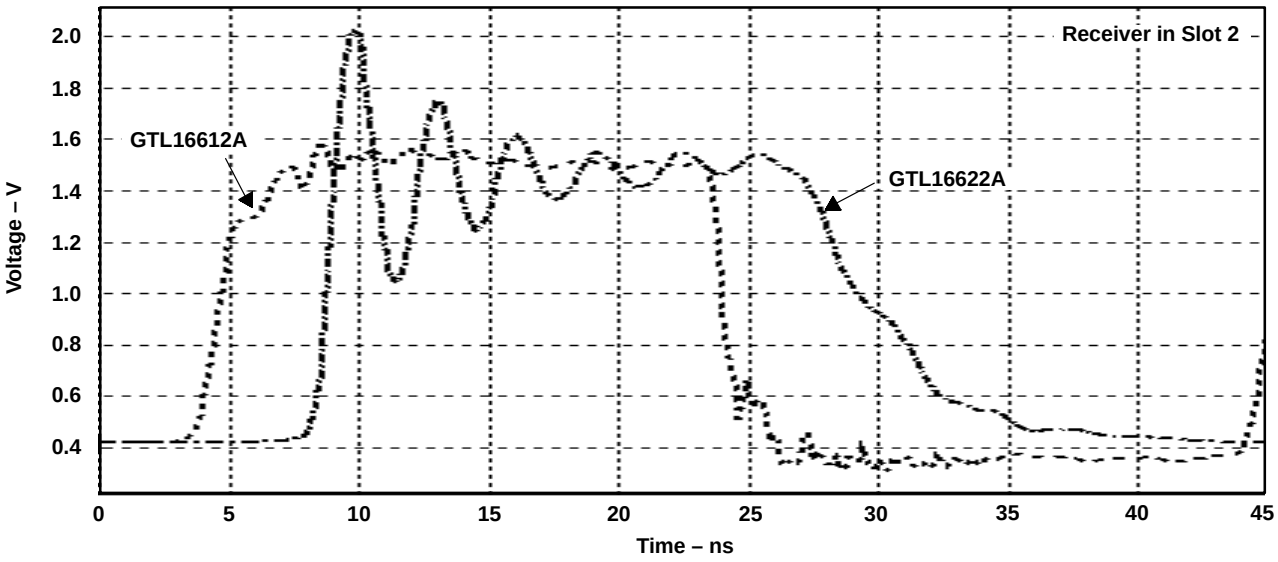

Figure 12. GTL16622A vs GTL16612A (50 MHz)

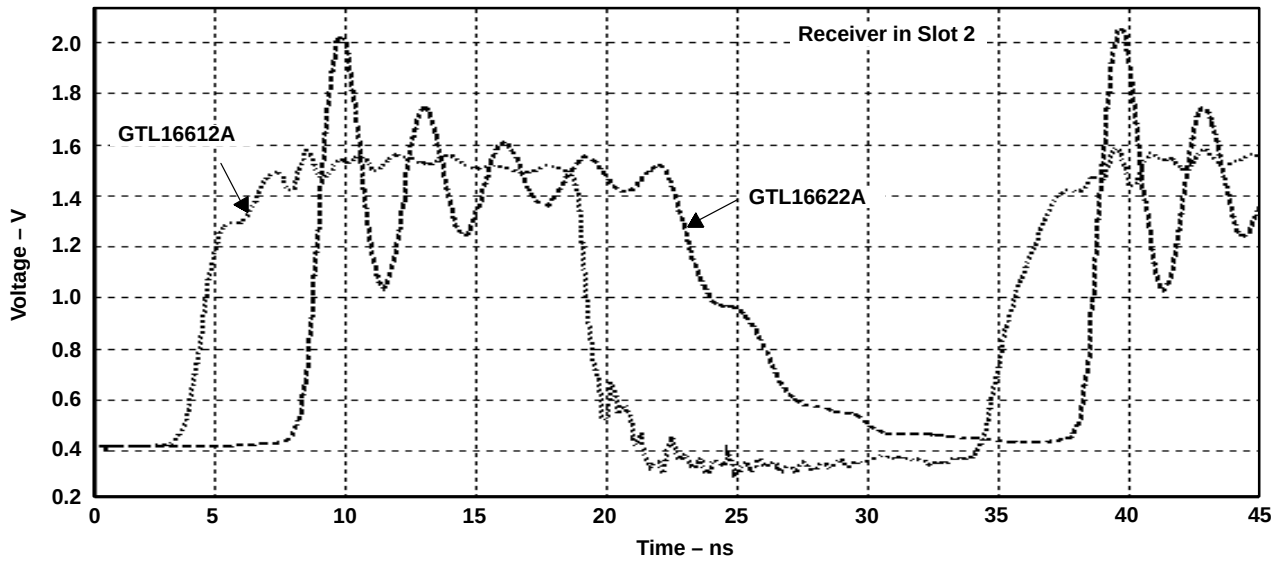

Figure 13. GTL16622A vs GTL16612A (66 MHz)

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Figure 14 shows simulation results for the GTL16612A operating at high clock rates of 80 MHz and 100 MHz. The innovative design of the 18-bit device provides for extremely high throughput on a backplane if the timing requirements of the board can be met.

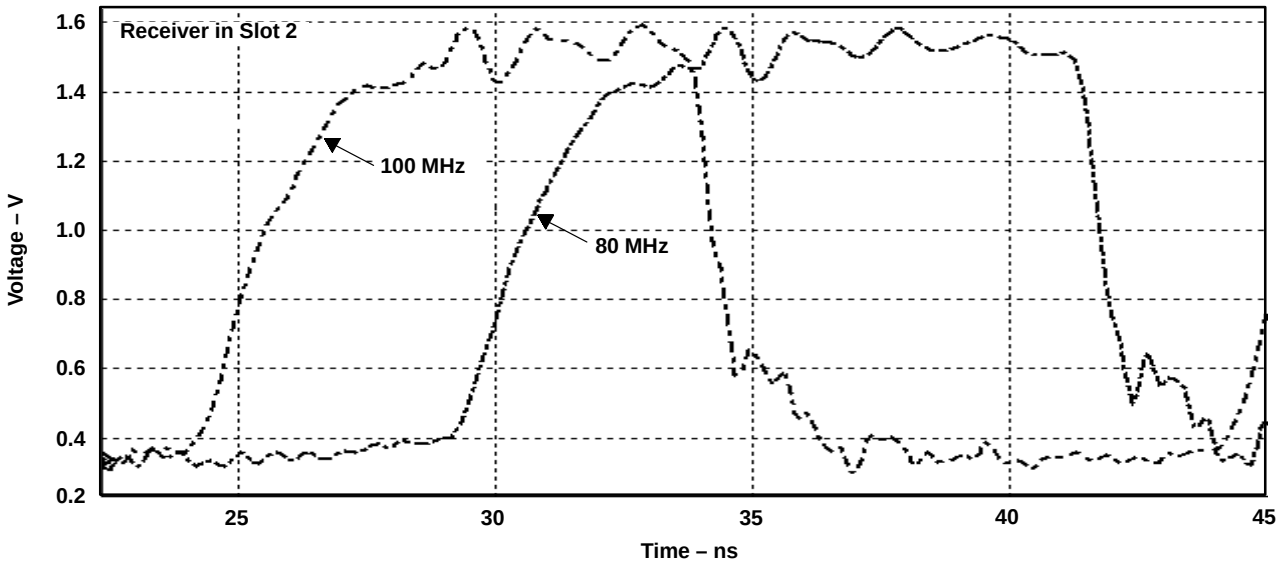

Figure 14. GTL16612A Simulation Results at 80 MHz and 100 MHz

Summary

The demonstration board has clarified backplane design issues and has provided unique insight into the capability of the GTL+ technology. With the escalation of requirements for high-speed data transfer, and a transition from low and medium performance to high performance, the backplane will be a critical component in the performance equation. The TI GTL16622A has served as a backplane driver for medium- and high-performance applications, while the new GTL16612A overcomes the problems in a very high-performance backplane to provide good signal integrity. Clearly, GTL+ is the next-generation technology, capable of accurately moving large amounts of data on the backplane with high speeds, while achieving the bit rates that will be required by new designs.

Acknowledgment

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The authors recognize the contributions and assistance provided by Adam Ley, Gene Hintershcer, and Mac McCaughey.

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5 California Micro Devices, “Termination Techniques for High Speed Buses”, *Electronic Design News*, February 1998.

Glossary

Incident-wave switching	Voltage transition that is strong enough to switch the input of the receiver on the first edge of the wave. This implies that subsequent reflections do not change the state of the receiver to its previous state.
Noise margin	Difference between the driver or receiver threshold voltage and the voltage on the bus. A noise margin comparison for the GTL/GTL+ technologies is shown in Table 1. The increased noise margin for GTL+ is preferred because it can result in better signal integrity.
Stub	Path on the board between the driver/receiver card and the backplane. This includes the trace on the board, the connectors, and the lumped capacitance of the driver or the receiver. The length from the driver/receiver to the backplane is the stub length.
Throughput	Data rate that is achieved on the bus or the backplane. It can be calculated on a parallel-bus architecture as the product of the number of bits and the frequency of transmission.