Application Note

High Quality Low-Dropout Regulator Measurement Techniques

Hannah Grace

ABSTRACT

This application note discusses the best practices for capturing quality measurements of Low Dropout (LDO) regulators. This document highlights measurements, including but not limited to line and load transients, as well as additional information regarding proper oscilloscope setup.

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1 Introduction

The *Linear and Low-Dropout (LDO) Regulators* regulates a higher input voltage to a lower output voltage, similar to a switching regulator. Unlike the switching regulator, an LDO works as a noise filter device and shows to be much simpler to implement in modern designs. To learn more about how an LDO operates, please see *Learn the Basics of Linear and Low Drop-Out Regulators (LDOs)*. With the increasing demand for low-noise parts in high-frequency power system applications, the LDO plays a significant role in meeting demand. The result of fulfilling this role means that more basic measurements are taken for debug purposes, and so on. Taking measurements can be a challenging task, so pay close attention to hardware setup and device configuration before taking a measurement. Typical measurements, include but are not limited to, load transients and line transients.

1.1 Oscilloscope Basics

While taking an oscilloscope measurement, remember these key fundamentals:

1. Before taking a measurement, understand the measurement being attempted. What are the conditions and what channels are being used?
   a. Make sure in the measurement that each condition that is necessary to see a proper measurement, such as VIN, VOUT, current, and so on, is setup for each channel.
   b. Labeling these channels on the oscilloscope, from the specified measurement conditions, helps for simple identification of each channel
2. Connect the LDO terminals to each oscilloscope channel as desired. Confirm that the oscilloscope is in high impedance mode and DC coupled. Choose probes that are matched to the oscilloscope's bandwidth for transient measurements. Verify that each oscilloscope channel shows the correct voltage and current levels in accordance to what levels are being set with the LDO.
   a. Choosing an oscilloscope probe for a measurement can be a difficult task. When choosing an oscilloscope probe it's important to choose the correct probe for the correct measurement. Please see the common oscilloscope issues section for additional information on choosing an oscilloscope probe.
   b. Be cautious when using a probe with long wires. Long cablings can cause parasitic concerns with measurements, which affect measurement readings. Please see implications of inductance to learn more about the affects of parasitics in a circuit.
3. Turn the oscilloscope on, which can take a significant amount of time.
4. Once the oscilloscope is turned on, the previously configured oscilloscope conditions for the horizontal system time scale and the vertical system voltage scale show on the screen. Adjust the horizontal time scale (seconds/div) to scale in or scale out on the time scale.
   a. Adjusting the horizontal time scale creates an affect of focusing in or focusing out of a waveform, which helps to show the full waveform around the desired signal activity. For an example of incorrect oscilloscope scaling, please see the common oscilloscope issues section.
   b. Consulting your oscilloscope's user guide can help you make setup adjustments to align with your measurement.
5. Once the oscilloscope is configured and triggered, you have your desired measurement!
   a. If you do not have your desired measurement, continue to adjust the vertical and horizontal scales, as well as, configure the Volts/div and the offset of each channel.
   b. Additionally, make sure to properly set the triggering levels in the output to enable or to a pin where the transient is being observed.
   c. Implementing a horizontal delay can allow for the waveform to reside closer to the center of the screen rather than off the screen.
6. Please read the oscilloscope's user guide for examples of taking a proper measurement.
   a. Additional resources are also available on the oscilloscope manufacturer's website. For example if using a Teledyne Lecroy oscilloscope, please see *Hands-On Guide to LeCroy Color Digital Oscilloscopes*.

Note

All channels in an oscilloscope share a common ground. Special attention is needed to avoid short circuits through the oscilloscope probe's ground.

2 Implications of Parasitics

When designing a circuit we often overlook parasitics, but in reality parasitics cause unexpected effects on measurements, which can alter data collection. What happens when these unexpected effects occur? When designing a printed circuit board (PCB), the designer must keep in mind that all traces are slightly resistive, capacitive, and inductive. These effects are otherwise known as parasitics. Especially in high frequency measurements, designing with parasitics is incredibly important to verify the LDO works as expected. Resistive parasitics can cause gain errors, create DC voltage errors, and create mismatches at the inputs of the gain amplifier that is present in an LDO. Capacitive and inductive parasitics can cause unwanted noise and signal coupling to occur. Capacitive parasitics can also cause instability to occur in the circuit. Inductive parasitics can increase the return loop inductance.

For LDOs, noise coupling and instability is especially important when taking high frequency measurements. With parasitics present in a circuit, additional ringing, oscillation, and unwanted noise coupling through a ground plane of power supply can be present in high frequency measurements. Examples of where parasitics can be present in a circuit are:

1. Microstrip Copper Traces:
   a. Microstrip copper traces are transmission lines with a copper plane typically used for high frequency signals.
2. Parallel Copper Planes
   a. Parallel copper planes are large sections of copper in the PCB intended for power signals, which are meant to carry hundreds of mA to Amps. Parallel copper planes are used as a low-impedance access to power or ground, but often create capacitive parasitics. Typically, the capacitive parasitics are created through a heat-sink.
3. Vias
   a. Vias connect signals between different layers on a PCB, but often create capacitive and inductive parasitics.
4. Adjacent Copper Traces
   a. Adjacent copper traces allow for routing to related groups of signals around a PCB, but often creates capacitive parasitics and allows for capacitive coupling of signal between traces, otherwise known as cross talk.

Before taking a measurement, we highly recommend controlling inductive and capacitive parasitics. To control inductive and capacitance parasitics, cut out copper planes and traces under sensitive test nodes, and minimize the use of vias on critical signal traces. Additionally, use short direct signal routing to minimize unwanted noise coupling, and place ground copper between adjacent traces to minimize cross talk, which is especially important when designing with dual input or dual output LDOs. To reduce inductance, the return path for high currents need to be parallel to the current carrying trace, but this can add parasitic capacitance to the circuit. Finally, we recommend reducing cabling attached to the device under test (DUT). Reducing external cabling through SMA, coaxial cables, twin axial cables, etc. minimizes the risk of parasitics on high-frequency measurements.

3 Common Oscilloscope Issues

Before a measurement can be taken, measurement set-up is crucial for device precision and specification accuracy.

3.1 Choosing an Oscilloscope Probe: Probe with Ground Clip vs SMA

Before taking a measurement, chose the correct type of oscilloscope probe for the measurement you are taking. When choosing an oscilloscope probe, note the importance to remember to choose an oscilloscope probe that is at least 10 times or greater bandwidth than the bandwidth of the LDO. Current LDOs in production can have a bandwidth up to 3-5MHz, so the oscilloscope probe you chose must have a bandwidth of 30-50MHz or greater.

Parasitics have been mentioned countless times when in accordance to taking oscilloscope measurements, and setting up / choosing a oscilloscope probe deem to be no exception to parasitics. Long probe cabling can give an inflated drop is transient tests. Capacitive 10X probes can add additional noise to the LDOs output signal. Additionally, introducing long ground loops while using a 10X probe can add additional unwanted noise to a measurement.

In this section we evaluate two scope probes, an SMA probe and a probe with a ground clip, while taking a load transient measurement. Figure 3-1 shows a load transient measurement using a probe with a GND clip. Figure 3-3 shows a load transient with an SMA probe. As seen with Figure 3-1, while using a oscilloscope probe with a GND clip, more ringing can be seen on the transient measurement, while less ringing and oscillation occurs with the SMA probe. The scope probe with a ground clip acts as an ground loop, which can add significant inductance to a measurement. Adding additional inductance can compromise the performance of a measurement, and can lead to measurement error. With a Teledyne Lecroy oscilloscope probe with a ground clip, a measurement can have as much as 40% error in peak to peak voltage.

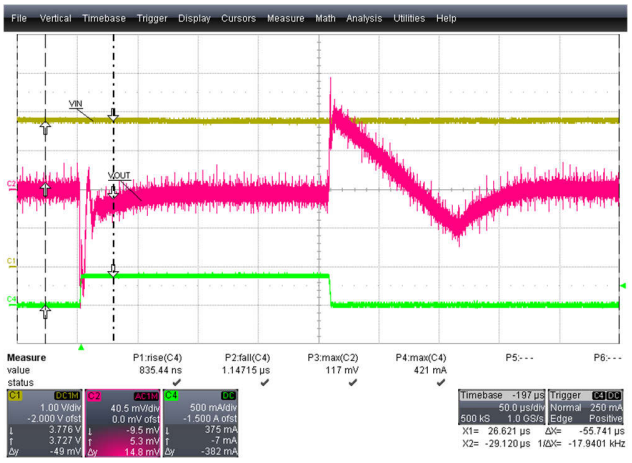

Figure 3-1. TLV737 Load Transient with Ground Clip Connection

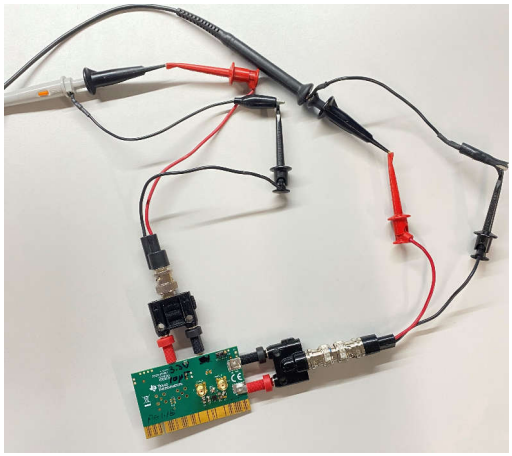

Figure 3-2. Ground Clip Setup on TLV737

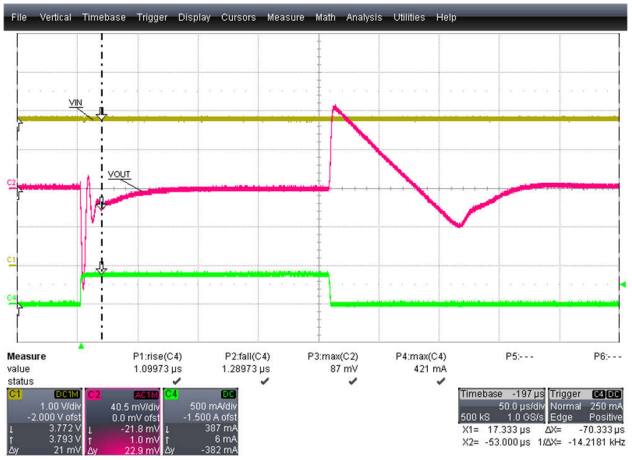

Figure 3-3. TLV737 Load Transient with SMA Connection

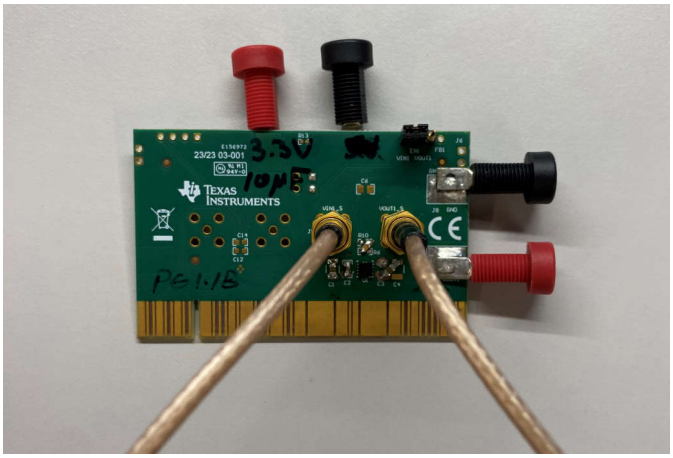

Figure 3-4. SMA Setup on TLV737

3.2 Sufficient Sampling

When taking measurements on the oscilloscope, sufficient sampling must be present for peak transients. When insufficient sampling is present while taking a waveform measurement, aliasing can occur in the measurement, which can cause inconsistent data collection. Aliasing can show a measurement to appear poorly triggered and shifted horizontally. To learn more about aliasing please see *Teledyne Lecroy Oscilloscope Basics: Sampling Rate*. Insufficient sampling can also show false peaks when conducting transients, which can also give incorrect measurement data. Insufficient sampling can also cause a lack of information to appear for data collected at the peaks of certain signals, as shown in Figure 3-5.

Additionally, when sufficient sampling is not present in a waveform, each channel is more difficult to visualize. Comparing the following images, Figure 3-5 with 500 samples and Figure 3-6 with 16M samples, Figure 3-5 with 500 samples is significantly more difficult to visualize each channel.

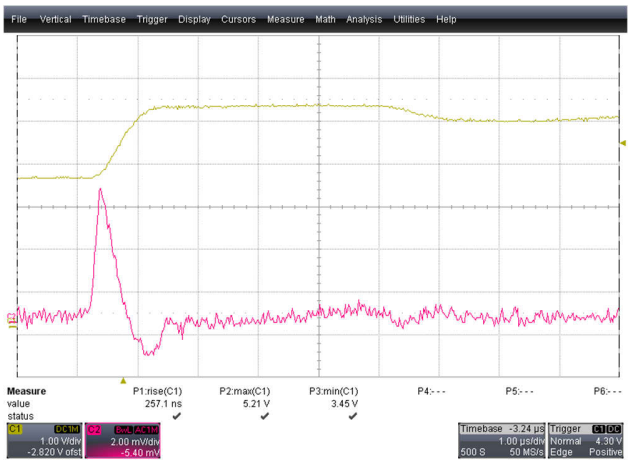

Figure 3-5. 500 Samples

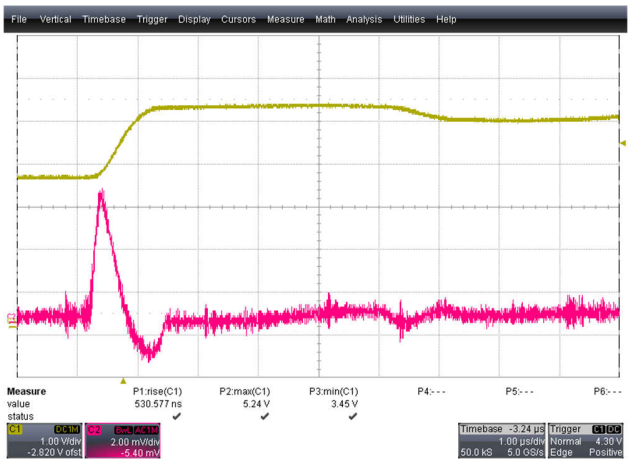

Figure 3-6. 16M Samples

Note

Not each oscilloscope is the same! There are oscilloscopes where the effective bandwidth and/or sampling is divided across channels, and can decrease when using more channels.

3.3 Visualization

Additionally, a waveform must be in visual focus to prevent picture resolution loss. When a waveform is not in visual focus, there can be difficulty distinguishing data at the rising and falling edges. When a waveform is illegible, only part of the waveform can be seen. Taking a measurement with improper visualization can lead to concerns when debugging a measurement for future development. Figure 3-7 shows a load transient measurement which is in an incorrect timebase for the measurement to be legible. Figure 3-8 shows a load transient measurement with a corrected timebase to account for distinguishing data on the rising edge. Figure 3-8 is an acceptable image for visualization.

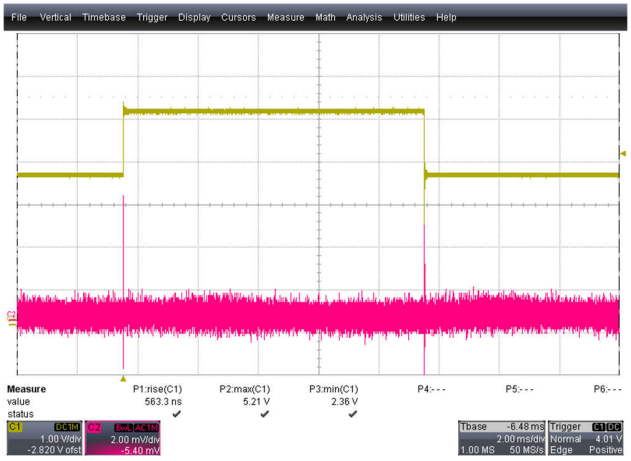

Figure 3-7. Poor Visualization

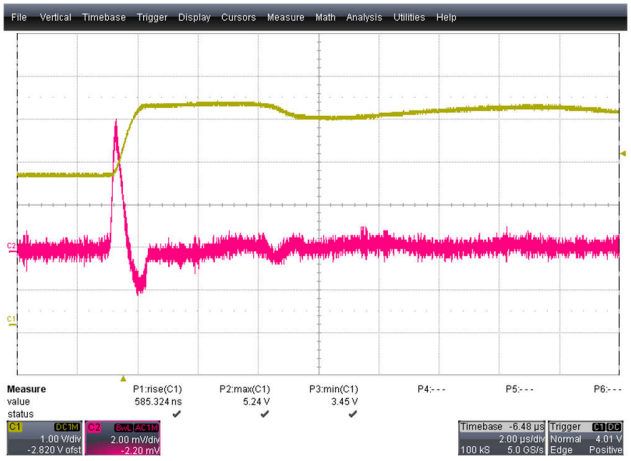

Figure 3-8. Focus on the Rising Edge

3.4 Measuring Using Current Probes

Another common measurement is taking input and output current measurements using a current probe. Typically, a current probe is used to take transient measurements. If parasitics are introduced on the current probe current path, false peaks can show on the oscilloscope shot, ultimately leading to inaccurate data collection. Load transient measurements were taken on the TPS793 device with the current probe which displays the output current on the green signal trace. Figure 3-9 shows a load transient measurement with long cabling, which introduces significant parasitics. As shown in Figure 3-9, false data peaks are taken at the output of the device. As compared withFigure 3-10, the load transient measurement includes significantly less cabling and minimal inductance, which leads to more accurate output measurement data.

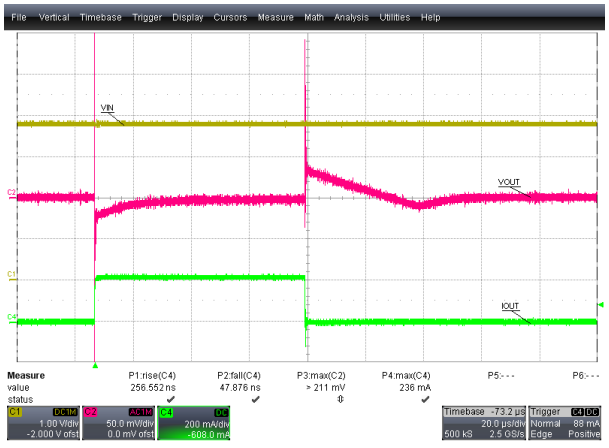

Figure 3-9. Current Probe Measurement with Long Cabling

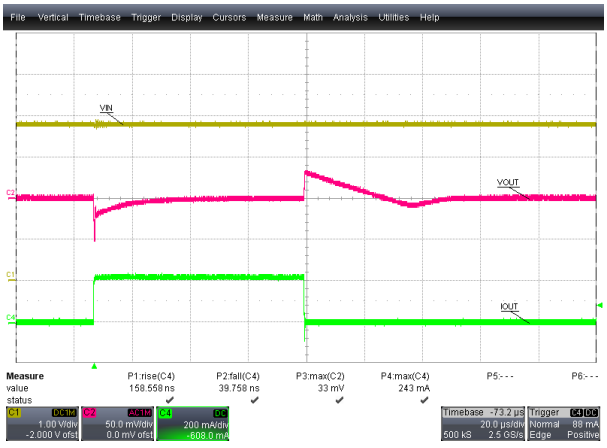

Figure 3-10. Current Probe Measurement with Shortened Cabling

3.5 Bandwidth Limiting and Averaging

Finally, integrating bandwidth limiting and averaging in a waveform reduces the full image. Although bandwidth limiting significantly reduces additional noise present in a waveform, bandwidth limiting can also reduce factors of the waveform that are important to see for debug, such as overshoot and undershoot, which can lead to inaccurate measurement readings, as seen in Figure 3-11.

Integrating averaging in a waveform can also reduce the image of the full waveform scope shot. Averaging shows a falsely better peak to peak measurement, as seen in Figure 3-12.

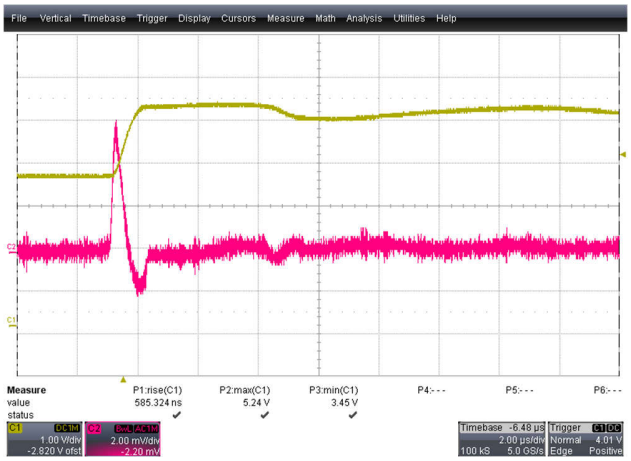

Figure 3-11. Bandwidth Limiting

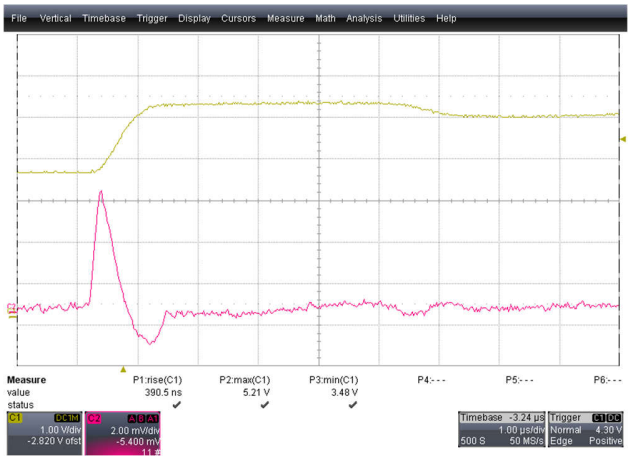

Figure 3-12. Averaging

4 Parasitic Effects on Common Measurements

4.1 Load Transients

A load transient is a sudden change in the load demand, which the LDO reacts to this condition accordingly. An unexpected voltage drop on the LDOs output can manifest when significant load transients are present. Typically with larger voltage transients, this can cause an issue with LDO operation. Effects of a load transient response are a direct result of LDO internal compensation, output capacitance, and the parasitics of the output capacitor. Since the LDOs internal compensation is fixed, the transient response can be varied through the circuit's output capacitor and parasitics. How do you know if a linear regulator responds well to load transients? A linear regulator is expected to respond to a transient in a smooth, controlled manner. For additional information on load transients please see *Understanding the Load-Transient Response of LDOs*.

In the following section, we review two load transient setup conditions. Conditions were tested using the device TPS7A96, which is a high speed LDO. With a high speed LDO, additional circuit inductance becomes apparent in a transient measurement. One condition has significant trace parasitics due to long cabling, while the other condition has limited trace parasitics and a closer connection to the DUT. Condition one shown in Figure 4-1 used a BNC cable, while condition two shown in Figure 4-2 used a close SMA connection. As seen in the following load transient conditions, with less cabling less overshoot occurred in the oscilloscope measurement. Figure 4-1 shows the maximum output voltage to settle at 39mV, while Figure 4-2 shows that the maximum output voltage settles at 11mV. Reducing parasitics for this specific load transient decreases the output voltage overshoot by 28mV. Overall, reducing parasitics in this example decreased voltage overshoot by 71%.

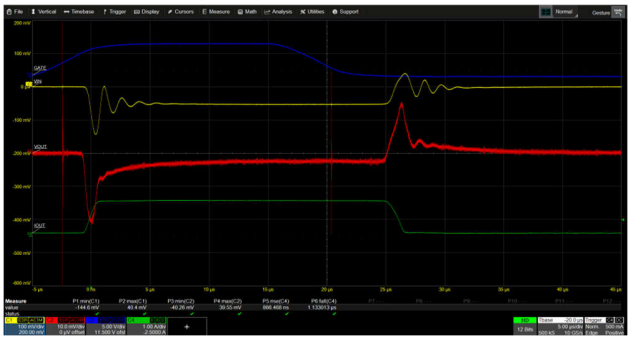

Figure 4-1. TPS7A96 Load Transient with Additional Parasitics

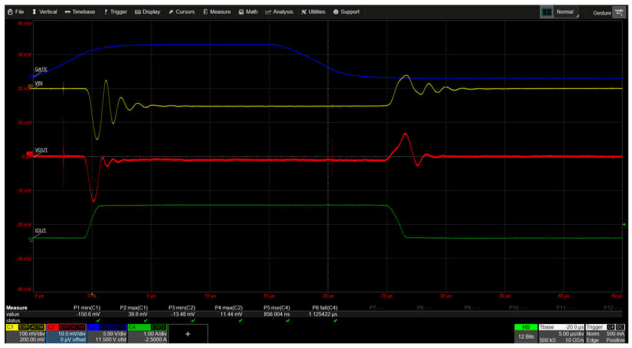

Figure 4-2. TPS7A96 Load Transient with Parasitic Limiting

4.2 Line Transients

A line transient is a sudden change in the line demand, and the LDO reacts to this condition accordingly. For additional information please see *Understanding the Terms and Definitions of LDO Voltage Regulators*.

In the following section, we review two line transient setup conditions. Conditions were tested using the device TLV773, while this device is not marketed as a high speed LDO on the market, there is still noticeable change when PCB parasitics are limited. Figure 4-3 shows significant trace parasitics due to poor PCB layout, while Figure 4-4 has limited trace parasitics and a direct connection to the DUT. Figure 4-3 shows how additional trace parasitics have a direct correlation with slower rise times and slightly higher overshoot as compared to Figure 4-4, which highlights a condition with limited trace parasitics. Figure 4-4 shows that the rise time with introduced parasitics was around 846nS, while with image blank the rise time decreased to 584nS. Reducing parasitics in this specific line transient measurement decreased the rise time by 262nS.

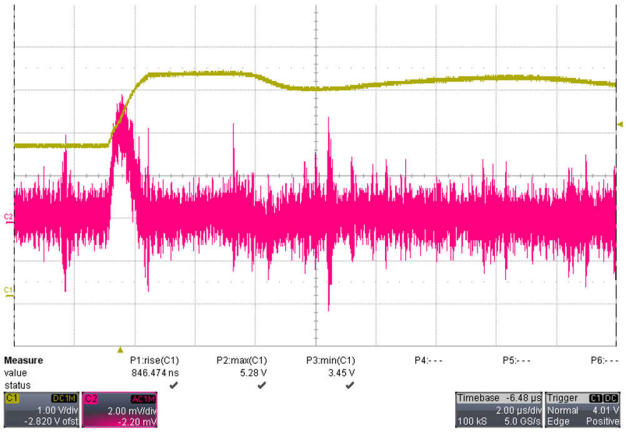

Figure 4-3. TLV773 Line Transient with Additional Parasitics

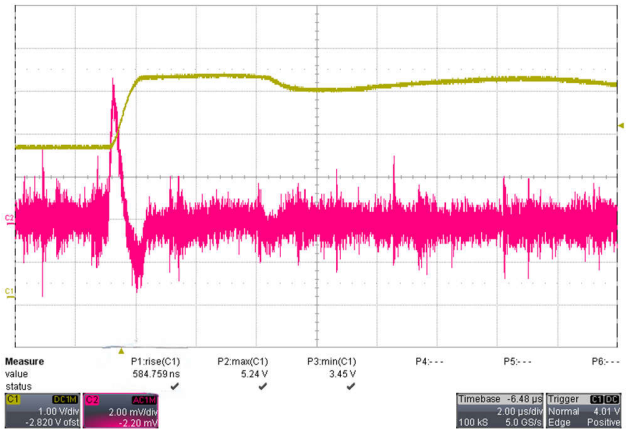

Figure 4-4. TLV773 Line Transient with Parasitic Limiting

4.3 Power Supply Rejection Ratio

Power Supply Rejection Ratio (PSRR) is a measure of how well a circuit rejects ripple injected into the input of a device, specifically an LDO. To learn more about PSRR and how to take a PSRR measurement, please see *LDO PSRR Measurement Simplified*.

In the following section, we review two PSRR measurement setup conditions taken with the TPS793 device, shown throughFigure 4-5. Condition one, shown with the red trace, shows a PSRR measurement taken with significantly longer cabling, while condition two, shown with the green trace, shows a PSRR measurement taken with significantly shorter cabling. When parasitics are introduced in a PSRR measurement, as shown with red trace, the PSRR measurement data collected at higher frequencies seems to be lower. At higher frequency measurements, especially for PSRR, the output capacitor characteristics significantly affects the measurement. With more parasitics tied to the output capacitor, the data collected at high frequencies shows the capacitor characteristics with those parasitics introduced.

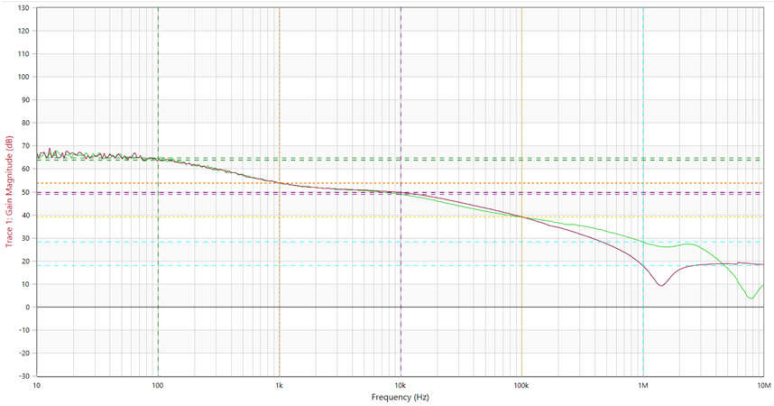

Figure 4-5. TPS793 PSRR with Additional Parasitics

4.4 Output Noise Voltage

Output noise voltage is the RMS output noise voltage over a given range of frequencies, typically 10HZ to 100kHz. Noise is measured under the conditions with constant output current and a ripple-free input voltage. To learn more about output noise voltage and how to take an LDO noise measurement, please see *How to Measure LDO Noise*.

The following sections reviews two noise measurement setup conditions. Conditions were tested on the TPS793 device. Figure 4-6 shows a noise measurement taken with significantly longer cabling, while Figure 4-7 shows a noise measurement taken with significantly shorter cabling. When parasitics are introduced in a noise measurement as seen with Figure 4-6, more cabling is introduced, which means more noise is present in the

measurement, which corresponds to the resulting data collection. With parasitics the noise collected in Figure 4-6 was found to be 69.9uVrms, while Figure 4-7, which has minimal parasitics shows data to be 68.9uVrms. Although for this specific application, the noise did not seems to change significantly, only 1uVrms, but with lower noise applications 1uVrms can have a significant impact on how the device can perform.

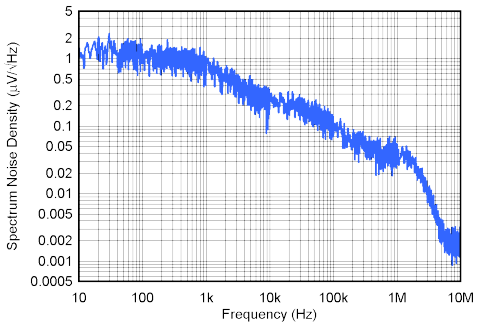

Figure 4-6. TPS793 Output Voltage Noise with Additional Parasitics

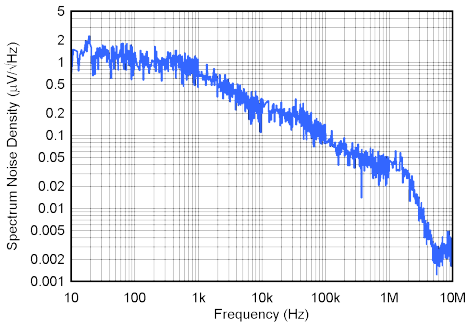

Figure 4-7. TPSS793 Output Voltage Noise with Parasitic Limiting

5 Summary

Measurement setup is important when verifying LDO device specification accuracy. Before taking a measurement, be aware of certain measurement conditions which can give false measurement data. Avoid bandwidth limiting and averaging, which can give unrealistic data, insufficient sampling which can cause aliasing and poor visualization, and choosing an incorrect oscilloscope probe that can cause additional ringing to occur in a measurement. Limit circuit inductance, with shortened cabling, to reduce voltage overshoot. Finally, make sure that the oscilloscope is properly calibrated to visualization needs by aligning the horizontal and vertical scales. Please verify measurement setup before taking a measurement on an LDO device.

6 References

- Teledyne LeCroy, *Oscilloscope Basics: Sampling Rate*.
- Texas Instruments, *Understanding the Load-Transient Response of LDOs*, technical article.
- Texas Instruments, *Understanding the Terms and Definitions of LDO Voltage Regulators*, application note.
- Texas Instruments, *LDO PSRR Measurement Simplified*, application note.
- Texas Instruments, *How to Measure LDO Noise*, application note.

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