INA250-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA250-Q1 (TSSOP-16 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

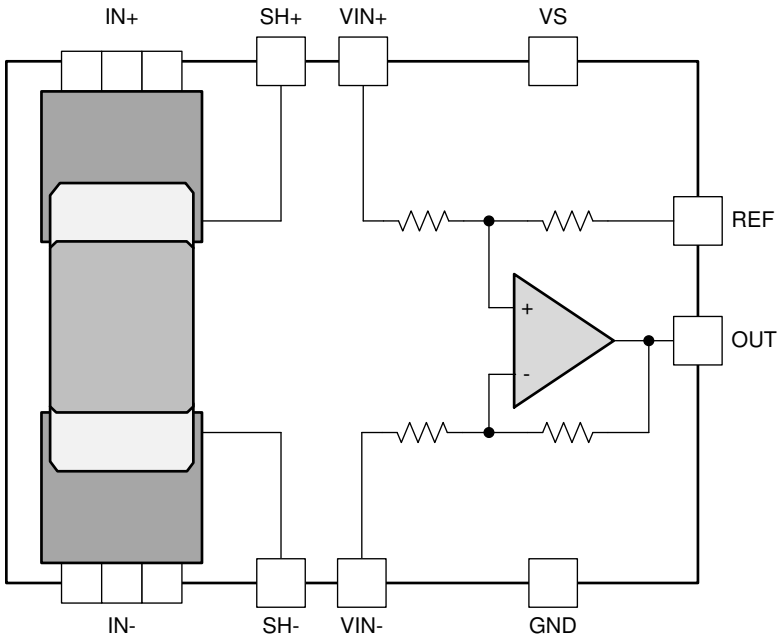

Figure 1. Functional Block Diagram

INA250-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA250-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	12
Die FIT Rate	3
Package FIT Rate	9

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 80 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Analog mixed < 50V	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA250-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT saturated to VS or GND	40%
OUT functional, not in specification	40%
Shunt resistor open pin IN+, IN-, SH+, SH-	5%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA250-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VS (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the INA250-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA250-Q1 datasheet.

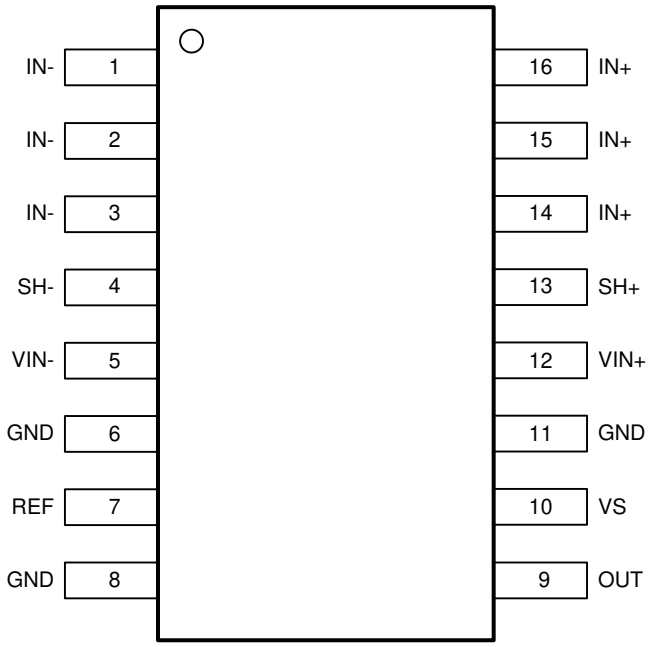

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 5 V
- V_{IN+} = 12 V
- $V_{REF} = V_S / 2$

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side
IN-	2	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side
IN-	3	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side
SH-	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. Shunt, bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
VIN-	5	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. Shunt, bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
GND	6	Normal operation.	D
REF	7	Normal operation if REF pin is at ground potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; B otherwise
GND	8	Normal operation.	D
OUT	9	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B
VS	10	Power supply shorted to GND.	B
GND	11	Normal operation.	D
VIN+	12	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. Bond wires of pins VIN+ and SH+, and die metal trace between pin IN+ and SH+ will be damaged.	A
SH+	13	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. Bond wires of pins VIN+ and SH+, and die metal trace between pin IN+ and SH+ will be damaged.	A
IN+	14	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. This will affect the system functionality but will not damage the IC.	B
IN+	15	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. This will affect the system functionality but will not damage the IC.	B
IN+	16	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. This will affect the system functionality but will not damage the IC.	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus voltage. Differential input voltage is 0V.	B
IN-	2	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus voltage. Differential input voltage is 0V.	B
IN-	3	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus voltage. Differential input voltage is 0V.	B
SH-	4	Shunt resistor is not connected to amplifier. VIN- pin may float to an unknown value. OUT will go to an unknown value not to exceed VS or GND.	B
VIN-	5	Shunt resistor is not connected to amplifier. VIN- pin may float to an unknown value. OUT will go to an unknown value not to exceed VS or GND.	B
GND	6	There are three GND pins. If all three are open, then GND is floating. Output may be incorrect as it is no longer referenced to GND.	B

Table 6. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF	7	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
GND	8	There are three GND pins. If all three are open, then GND is floating. Output may be incorrect as it is no longer referenced to GND.	B
OUT	9	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
VS	10	No power supply to device. Device may be biased through inputs. Output will be close to GND.	B
GND	11	There are three GND pins. If all three are open, then GND is floating. Output may be incorrect as it is no longer referenced to GND.	B
VIN+	12	Shunt resistor is not connected to amplifier. VIN- pin may float to an unknown value. OUT will go to an unknown value not to exceed VS or GND.	B
SH+	13	Shunt resistor is not connected to amplifier. VIN- pin may float to an unknown value. OUT will go to an unknown value not to exceed VS or GND.	B
IN+	14	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0V.	B
IN+	15	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0V.	B
IN+	16	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0V.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	2 - IN-	Normal operation.	D
IN-	2	3 - IN-	Normal operation.	D
IN-	3	4 - SH-	Measurement accuracy will be degraded.	C
SH-	4	5 - VIN-	Normal operation.	D
VIN-	5	6 - GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. Shunt, bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
GND	6	7 - REF	Normal operation if REF pin is at ground potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; B otherwise
REF	7	8 - GND	Normal operation if REF pin is at ground potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; B otherwise
GND	8	9 - OUT	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B
OUT	9	10 - VS	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B
VS	10	11 - GND	Power supply shorted to GND.	B
GND	11	12 - VIN+	A short from the bus supply to GND will occur. High current will flow from bus supply to ground. Bond wires of pins VIN+ and SH+, and die metal trace between pin IN+ and SH+ will be damaged.	A
VIN+	12	13 - SH+	Normal operation.	D
SH+	13	14 - IN+	Measurement accuracy will be degraded.	C
IN+	14	15 - IN+	Normal operation.	D
IN+	15	16 - IN+	Normal operation.	D
IN+	16	1 - IN-	Shunt resistor is bypassed, and differential input voltage will be 0V. Functionality will be affected.	B

Table 8. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	1	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low-side configuration, system functionality will be affected.	A for high-side; B for low-side
IN-	2	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low-side configuration, system functionality will be affected.	A for high-side; B for low-side
IN-	3	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low-side configuration, system functionality will be affected.	A for high-side; B for low-side
SH-	4	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt, die metal trace between pin IN- and SH- will be damaged.	A
VIN-	5	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt, die metal trace between pin IN- and SH- will be damaged.	A
GND	6	Power supply shorted to GND.	B
REF	7	Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF=VS by design; B otherwise

Table 8. Pin FMA for Device Pins Short-Circuited to VS (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	8	Power supply shorted to GND.	B
OUT	9	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self heating could cause die junction temperature to exceed 150°C.	B
VS	10	Normal operation.	D
GND	11	Power supply shorted to GND.	B
VIN+	12	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt, die metal trace between pin IN+ and SH+ will be damaged.	A
SH+	13	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt, die metal trace between pin IN+ and SH+ will be damaged.	A
IN+	14	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high-side configuration, bus supply is shorted to VS and system functionality will be affected.	A for low-side; B for high-side
IN+	15	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high-side configuration, bus supply is shorted to VS and system functionality will be affected.	A for low-side; B for high-side
IN+	16	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high-side configuration, bus supply is shorted to VS and system functionality will be affected.	A for low-side; B for high-side

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265