Functional Safety Information

INA300-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for INA300-Q1 (VSSOP-10 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

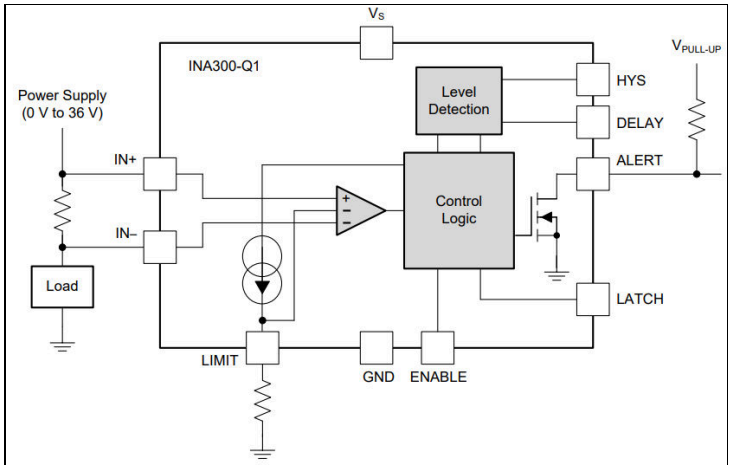

Figure 1-1. Functional Block Diagram

INA300-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA300-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA300-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Alert fails to trip	25%
Alert false trip	25%
Alert functional, trips out of specification voltage or timing	45%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA300-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the INA300-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA300-Q1 data sheet.

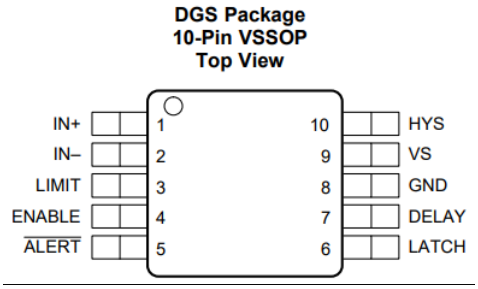

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- VS = 2.7 V to 5.5 V
- V_{IN+} = 12 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, input pins are shorted.	B
IN-	2	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to ground. In low side configuration, normal operation.	B for high-side; D for low-side
LIMIT	3	ALERT output is stuck low.	B
ENABLE	4	Device is disabled.	D if ENABLE=GND by design; C otherwise
$\overline{\text{ALERT}}$	5	ALERT output is stuck low.	B
LATCH	6	If intended connection is not GND, functionality will be affected.	D if LATCH=GND by design; C otherwise
DELAY	7	If intended connection is not GND, functionality will be affected.	D if DELAY=GND by design; C otherwise
GND	8	Normal Operation.	D
VS	9	Power supply shorted to ground.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
HYS	10	If intended connection is not GND, functionality will be affected.	D if HYS=GND by design; C otherwise

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	Differential input voltage is not well defined.	B
IN-	2	Differential input voltage is not well defined.	B
LIMIT	3	Comparator threshold is not defined.	B
ENABLE	4	Device mode is not defined.	B
$\overline{\text{ALERT}}$	5	ALERT can be left open.	C
LATCH	6	ALERT pin mode is not defined.	B
DELAY	7	If intended connection is not OPEN, functionality will be affected.	D if DELAY=OPEN by design; C otherwise
GND	8	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
VS	9	No power supply to device.	B
HYS	10	If intended connection is not OPEN, functionality will be affected.	D if HYS=OPEN by design; C otherwise

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	IN-	Input differential voltage=0V.	C
IN-	2	LIMIT	In low-side configuration, ALERT output is stuck low; In high-side configuration, device damage if common mode voltage is greater than 6V.	C for low-side; A for high-side
LIMIT	3	ENABLE	ALERT output may be stuck low, high or become unpredictable.	B
ENABLE	4	$\overline{\text{ALERT}}$	ALERT output may become unpredictable.	B
$\overline{\text{ALERT}}$	5	LATCH	ALERT output may become unpredictable.	B
LATCH	6	DELAY	ALERT output may be transparent, latched or become unpredictable.	B
DELAY	7	GND	If intended connection is not GND, functionality will be affected.	D if DELAY=GND by design; C otherwise
GND	8	VS	Power supply shorted to GND.	B
VS	9	HYS	If intended connection is not VS, functionality will be affected.	D if HYS=VS by design; C otherwise
HYS	10	IN+	In low-side configuration, HYS pin is stuck low; In high-side configuration, device damage if common mode voltage is greater than 6V.	C for low-side; A for high-side

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged.	A for High side; B for low side
IN-	2	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Device could be damaged.	A for High side; B for low side
LIMIT	3	Alert output is stuck high.	B
ENABLE	4	Device is enabled.	D if ENABLE=VS by design; C otherwise
$\overline{\text{ALERT}}$	5	Power supply could be shorted to GND though this pin.	A
LATCH	6	If intended connection is not VS, functionality will be affected.	D if LATCH=VS by design; C otherwise
DELAY	7	If intended connection is not VS, functionality will be affected.	D if DELAY=VS by design; C otherwise

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	8	Power supply shorted to GND.	B
VS	9	Normal operation.	D
HYS	10	If intended connection is not VS, functionality will be affected.	D if HYS=VS by design; C otherwise

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (October 2021) **Page**

- Added new sections and updated the numbering format for tables, figures, and cross-references throughout the document.....1
- Changed Total Component FIT Rate from: 7 to: 6.....2
- Changed Die FIT Rate from: 3 to: 2.....2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265