Application Note

Biasing GaN and LDMOS RF Power Amplifiers in Aerospace and Defense

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ABSTRACT

Biasing power amplifiers (PA) in aerospace and defense applications can be expensive, hard to scale, and require a large area of board space to implement. The AFE20408 addresses these issues by integrating eight digital-to-analog converters (DACs), an analog-to-digital converter (ADC), and fast gate bias switches into a small 5mm x 5mm package. This application note also details power-on sequencing requirements and the multiple output configurations of the AFE20408.

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Trademarks

1 Introduction

The AFE20408 is an analog front end (AFE) highly integrated PA biasing controller. The AFE combines 8 DACs, a multi-input ADC, and fast gate bias switches in a tiny 5mm x 5mm package.

The eight 13-bit DACs each have a range of 0V to 10V and –10V to 0V. The DACs are grouped in two blocks, each with a separate supply voltage. This allows for both positive and negative DAC outputs on one device, enabling one device to power both LDMOS and GaN PAs.

The AFE20408 has two groups of four fast low on-resistance switched outputs. These switched outputs allow for fast switching between two DAC channels at different voltages facilitating time-division duplexing. These switched outputs can also switch from a DAC voltage to VSS, allowing more DAC channels to be used for gate biasing. Built in redundancy allows the switches to be toggled either through software bits or hardware pins.

The AFE20408 features an integrated 16-bit ADC. The ADC has two high-voltage bus lines that measure voltages up to an 85V input and two pairs of high-side current sense inputs. Furthermore, the device has an internal temperature sensor. All of these inputs can be configured to set an alarm condition with user-defined minimum and maximum thresholds.

Other features of the AFE20408 include a flexible digital VIO voltage input from 1.8V to 5V, an auto-detectable SPI or I^2C communication interface, sixteen I^2C target addresses, a device-good pin (PAON) to indicate device readiness, and a FLEXIO pin that can be configured as RESET, ALARMOUT, ALARMIN, LDAC, DRVEN2, or a GPIO pin.

2 Application Figure

Figure 2-1 shows an example application of the AFE20408.

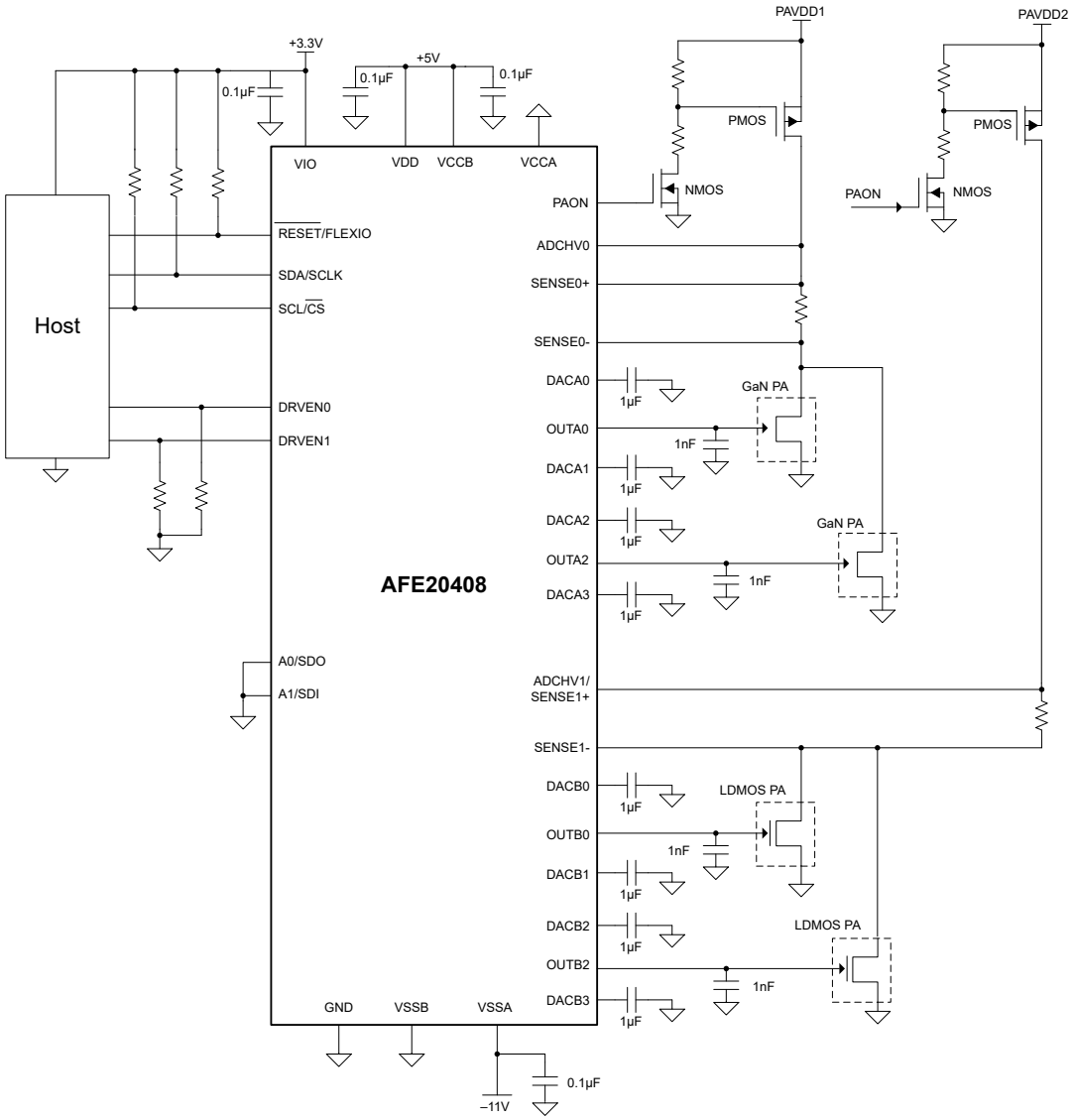

Figure 2-1. AFE20408 GaN and LDMOS PA Biasing Application

The application figure highlights how to use the various features of the AFE20408:

The PAON switch keeps the PAVDD isolated through a high voltage NMOS-PMOS switch. When PAON is low, the PMOS is disabled and the PAVDD is isolated from the PA. When PAON is high, the PMOS is enabled and the PAVDD is connected to the PA. By default, the PAON pin is low and requires the user to enable. This circuit ensures that the PA is isolated and protected during startup.

The ADC has user configurable alarm conditions used to monitor the PAVDD voltage and current. The ADCHV channels can alert the system if the PAVDD voltage is measured out of the configured thresholds and the SENSE pins can be configured with an external resistor to monitor PAVDD current. If the ADC detects an alarm condition, the PAON and DAC outputs shut off to protect the PA.

The fast switching works via capacitor charge sharing. The DAC outputs have large external capacitance while the OUT outputs have small external capacitance. When the switch toggles between different outputs, the small capacitor on the output is quickly charged by the larger DAC capacitor, allowing for very fast output switching. The output slews to 95% of the DAC voltage within 100ns. The switches have a max 400ns activation time.

3 Output Configurations

The flexibility of the switching mechanism allows the user to configure the AFE20408 in a variety of ways. For simplicity, this document refers to DACA0, DACA1, and OUTA0. All other DAC-OUT-DAC groups can be configured in the same way.

The switches can be toggled with software bits or hardware pins. By default, the switches are configured to work with software. Each DAC output has an associated DRVEN software bit that toggles the output switch or DAC buffer, depending on the DAC. Figure 3-1 shows how the OUTA0 switches are configured in the AFE20408.

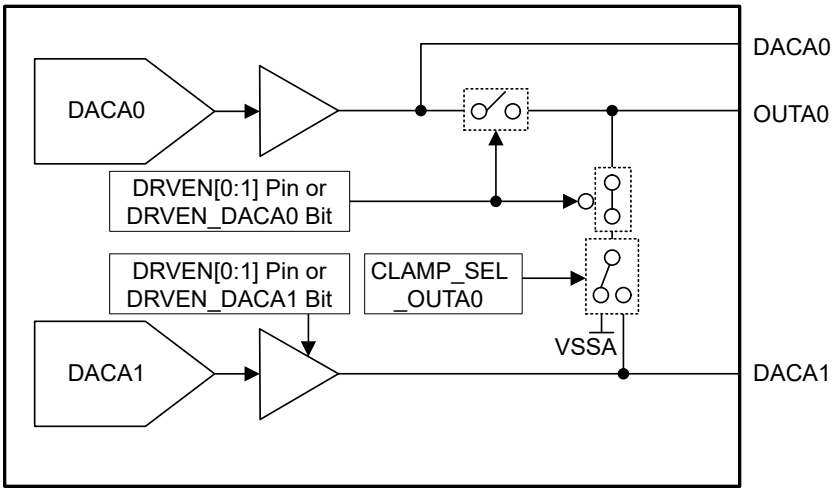

Figure 3-1. AFE20408 OUTA0 Switches

The OUTA0 pin switches between the DACA0 voltage and the CLAMP voltage with the DRVEN_DACA0 bit. When DRVEN_DACA0 is 0, OUTA0 is set to the CLAMP voltage. When DRVEN_DACA0 is 1, OUTA0 is set to DACA0. The CLAMP voltage is set to either VSSA or DACA1 through the CLAMP_SEL_OUTA0 bit. The DRVEN_DACA1 bit controls the DACA1 buffer. A digital 1 turns the DACA1 buffer on, and 0 turns the DACA1 buffer off.

The four sets of DAC-OUT-DAC groups can be configured independently, allowing for a multitude of configurations to meet the user's requirements. Table 3-1 shows a few of the possible configurations with the DACA0-OUTA0-DACA1 group using the software bits.

Table 3-1. AFE20408 Output Configurations

CLAMP_SEL_OUTA0 CLAMP Setting	DRVEN_DACA0 = 0 OUTA0 Output	DRVEN_DACA0 = 1 OUTA0 Output	DRVEN_DACA1 = 0 DACA1 Output	DRVEN_DACA1 = 1 DACA1 Output
VSSA	VSSA	DACA0	VSSA	DACA1
DACA1	DACA1	DACA0	Ignored	Ignored

There are three possible hardware pins: DRVEN0, DRVEN1, and DRVEN2. DRVEN2 is one of the selectable options of the FLEXIO pin. Each of the switches can be enabled by the hardware pins instead of software.

Figure 3-2 shows a switch configuration where DACA1 is set as the clamp voltage. The OUTA0 switch toggles the OUTA0 output voltage between on voltage DACA0 and the PA pinch-off voltage DACA1. This configuration allows for a precise gate on and off voltage to minimize wasted power and switching speed. The large capacitors on the DAC outputs allow for fast output switching, as seen in Figure 3-3. In this plot, the switch is being driven by a 1MHz signal on the DRVEN0 pin.

Table 3-2. AFE20408 Dual DAC Configuration

CLAMP Setting	OUTA0 OFF Output	OUTA0 ON Output
DACA1	DACA1	DACA0

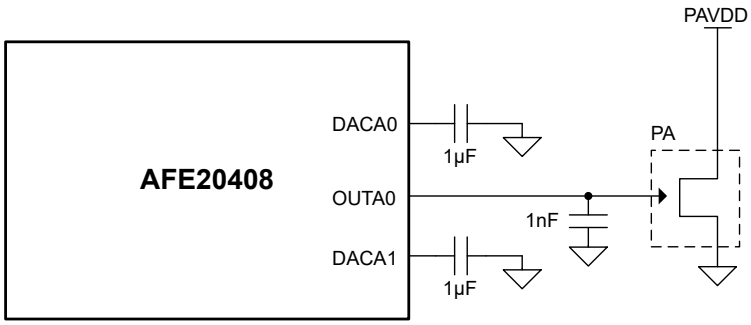

Figure 3-2. Dual DAC Configuration

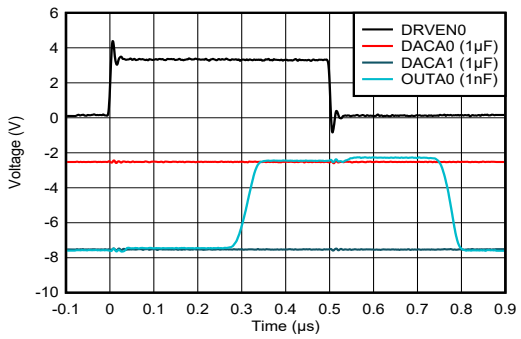

Figure 3-3. Dual DAC Switching Plot

Figure 3-4 shows a switch configuration where the clamp is set to VSSA. This configuration has the OUTA0 pin switch between on voltage DACA0 and off voltage VSSA. This configuration does not give the same precise pinch-off voltage as the dual-DAC configuration, but allows DACA1 to be used for additional gate biasing. The large capacitor on DACA0 allows for fast output switching, as seen in Figure 3-5. In this plot, the switch is being driven by a 1MHz signal on DRVEN0.

Table 3-3. AFE20408 Single DAC Configuration

CLAMP Setting	OUTA0 OFF Output	OUTA0 ON Output
VSS	VSS	DACA0

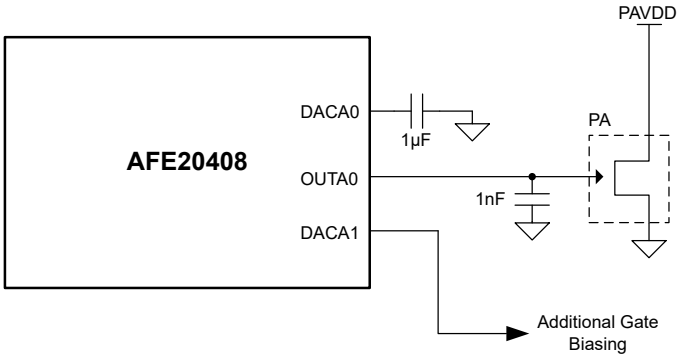

Figure 3-4. Single DAC Configuration

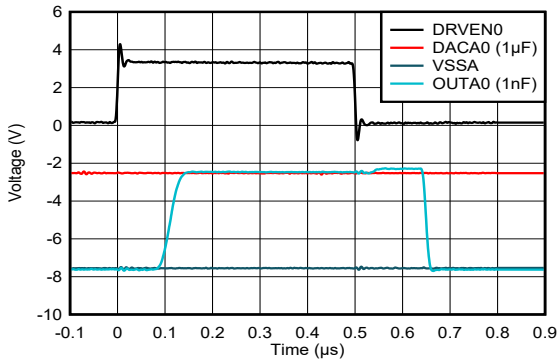

Figure 3-5. Single DAC Switching Plot

The DACA1 buffer can be configured to toggle on and off with the DRVEN pins as well. DACA1 switching is much slower, as seen in Figure 3-6. In this plot, the switch is being driven by a 80kHz signal on DRVEN0. This slow switching is due to the capacitor on DACA1 having to charge each time the switch turns on. Because of this charge time, a small capacitor is recommended for the DACA1 output.

If DACA1 is set as the CLAMP, DACA1 ignores the OFF condition and stays high.

Table 3-4. AFE20408 DACA1 Buffer Configuration

CLAMP Setting	DACA1 OFF Output	DACA1 ON Output
VSS	VSS	DACA1
DACA1	Ignored	DACA1

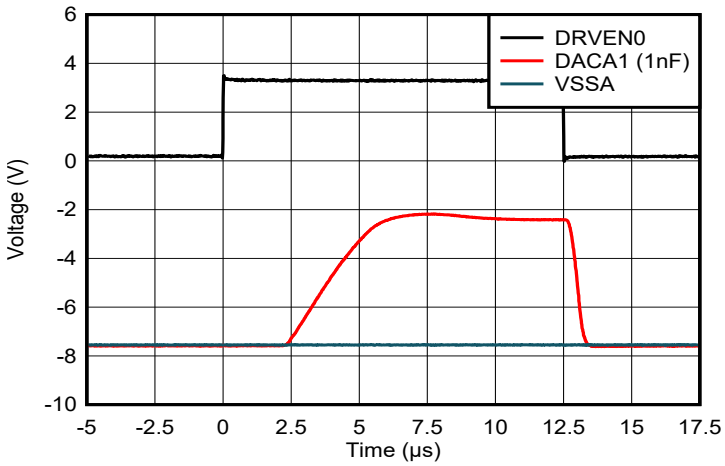

Figure 3-6. DACA1 DRVEN Switching Plot

4 Power Sequencing

Powering the PA on and off in a controlled routine is necessary to prevent the PA gate voltage from being too high when PAVDD is applied. If the gate voltage is too high, the PA can operate in saturation mode and cause thermal damage to the PA or the board the PA is mounted on. After the AFE20408 is powered up, the proper start-up sequencing for the PA requires the following steps:

1. Power on the AFE20408.
2. Set the gate voltage to the appropriate pinch-off voltage to keep the PA off while the PAVDD is applied.
3. Enable the PAVDD voltage using the AFE20408 PAON pin and PMOS-NMOS circuit or through external circuitry and signals.
4. Now that PAVDD is applied, the gate bias can be increased to set the desired power output of the PA.
5. Finally, the RF signal can be enabled. This allows the PA to transmit a signal.

The PA can be safely shut down by reversing the power-on steps:

1. Disable the RF signal from the PA.
2. Reduce the DAC outputs to the pinch-off value to turn off the PA.
3. Disable the PAVDD voltage through external circuitry or the PAON pin.
4. Disable the DAC outputs after the PA is fully disabled.
5. Turn off the power to the AFE20408.

The following sections detail output behavior during device power-up.

4.1 Power Up Positive Range

The AFE20408 power up sequence is designed to protect the PA. During start-up, the outputs are connected to ground. This ensures that the PA stays off as the AFE20408 powers up. Additionally, the PAON output stays low until the user enables the PAON output allowing the option to keep the PAVDD from connecting to the PA until the system is fully configured. Figure 4-1 shows the output glitch during start-up. The glitch for the outputs are nominally 15mV, ensuring the PA does not turn on during start-up.

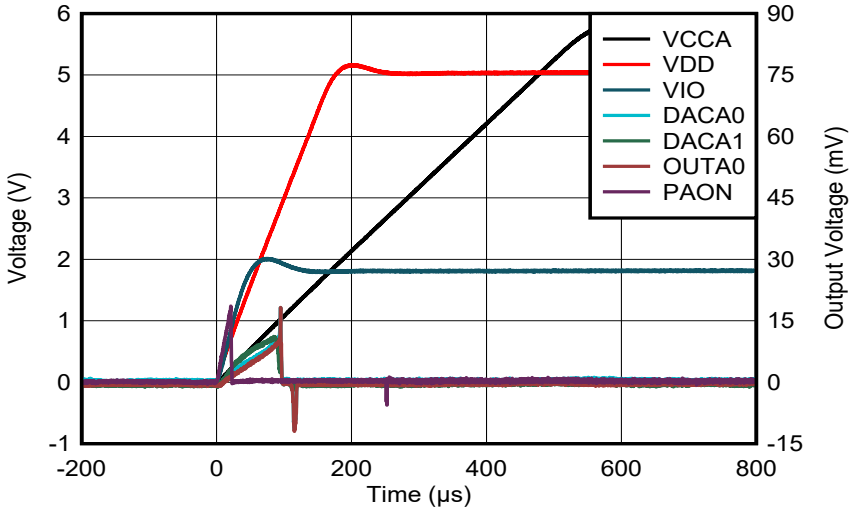

Figure 4-1. AFE20408 Positive Startup

In the case of an unplanned voltage shut off, such as one of the input voltages collapsing, the device sets all outputs to ground and disables the PAON to protect the device and the PA.

4.2 Power Up Negative Range

The power up for the negative range is similar to the positive range, but the outputs are tied to the VSS voltage during start-up. Figure 4-2 shows the start-up behavior. This means that during start-up there is a period where the outputs are within the on range of the PA. Because the PA can possibly be powered, the PA should be isolated from PAVDD so the PA does not erroneously turn on.

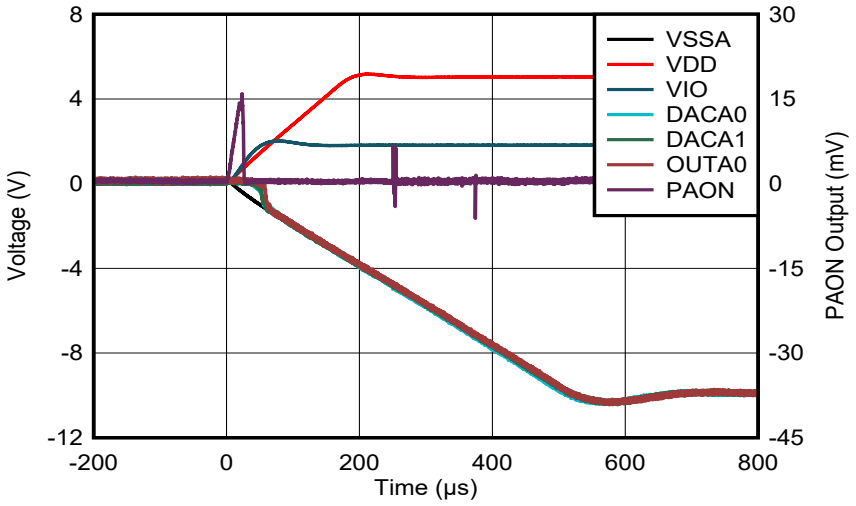

Figure 4-2. AFE20408 Negative Startup

5 Summary

The AFE20408 simplifies the circuitry required to control PA biasing and power-up sequencing while adding many beneficial features such as PAVDD current and voltage monitoring, output switching, and PAVDD voltage control. The AFE20408 is able to output positive and negative voltages at the same time which allows the device to bias both GaN and LDMOS PAs. The flexibility of the output switching configuration makes this a great device for projects that require fast switching up to 400ns, while also providing options for additional biasing or slow switching. The AFE20408 provides a flexible, robust, board space efficient design for PA biasing in aerospace and defense, such as Radar and Electronic Warfare applications.

6 References

- AFE20408EVM Product Page

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