Application Note

Working With Analog Inputs in the TLV320ADCX120 and PCMX120-Q1 Family

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ABSTRACT

The TLV320ADC5120 is a Burr-Brown™ high performance, audio analog-to-digital converter (ADC) that supports simultaneous sampling of up to two analog channels or four digital channels for the pulse density modulation (PDM) microphone input. The device supports line and microphone inputs, and allows for both single-ended and differential input configurations.

This application note describes the analog inputs of the TLV320ADCX120/PCMX120-Q1 family. This document describes AC and DC input coupling schemes possible with these ADCs as well as different application circuits with microphones. This application note also illustrates some non-audio applications for the TLV320ADCX120/PCMX120-Q1 family.

Table of Contents

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1 Introduction

The TLV320ADCX12O/PCMX120-Q1 family supports DC coupling as well as AC coupling for analog inputs. The TLV320ADCX12O/PCMX120-Q1 device consists of two pairs of analog input pins (INxP and INxM) that can be configured as differential inputs or single-ended inputs for the recording channel. Typically, voice or audio signal inputs are capacitive coupled (AC coupled) to the device; however, the device also supports an option for DC-coupled inputs.

1.1 AC Coupled Systems

- In an AC coupled system, the DC Biasing at the input of the ADC is independent of the DC level of the source. The ADC input is biased internally by the chip at an optimum DC level maintaining that ADC digitizes full scale AC input signals.
- Coupling capacitors used at the ADC input form a high-pass filter with the input impedance of the ADC limiting the low frequency response of the system. For audio applications, the capacitors are sized such that frequencies as low as 20 Hz can be digitized.
- A coupling capacitor must be charged to a steady state value on power-up. Until the time the capacitor reaches this value, the input audio signal is not passed properly to the ADC. Sometimes this situation is heard as a pop in the audio output.
- A coupling capacitor needs to behave as a short circuit for all AC signals in the audio range. In practice the capacitance value and the capacitive impedance can change with signal amplitude across the capacitor. This value can result in non-linear behavior and harmonic distortion in ADC output at low frequencies.
- Some capacitors also display microphony. When experiencing vibration, the capacitor can induce a voltage in the AC path due to the Piezo Effect.

1.2 DC Coupled System

DC coupled systems eliminate coupling capacitors. The DC coupled system has the following advantages:

- Lower bill of material cost and less board space.
- Performance degradation due to non-linear effects in capacitors can be eliminated including THD degradation at low frequency and board vibration effects.
- Start-up pop is eliminated..
- The ADC output is valid to DC which allows for the possibility to do measurements such as voltage and current for test and measurement.

DC coupling also has some disadvantages:

- The DC biasing of the input pins is not determined by the ADC circuit but by the external source. Since the biasing is not always optimum, the ADC can display a reduced signal handling.
- The Dynamic Range Extension (DRE) functionality of the ADC relies on adapting the PGA gain. This functionality can also be limited in DC coupled applications.

In DC coupling, DC differences between the INxP and INxM pins appear as an offset at the output of the ADC which can lead to saturation of the ADC output at high PGA gains. Therefore high PGA are not always possible with DC coupling.

2 AC Coupling Schemes

2.1 Equivalent Circuit

Figure 2-1 describes the equivalent circuit for the input pin. In a capacitive coupled system, the biasing of the pin is done internally by the voltage as shown in Equation 1, where k is approximately 0.5.

$$V_{INxP} = k \times V_{REF} \quad (1)$$

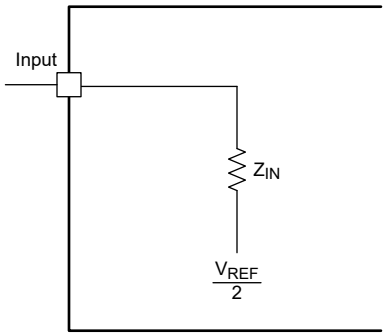

Figure 2-1. Equivalent Circuit for Input Pin for AC Coupled System

Register settings for the input pin:

- CH1_CFG0 register (address = 0x3C) Bit 4, CH1_DC=0 selects AC Coupling for channel 1. The setting also selects single-ended or differential mode.
- The DC voltage on the pin is VREF/2. The value of this reference voltage can be configured using the P0_R59_D[1:0] register bits as shown in Table 2-1.
- PO_R_60_D{3:2} are used to select the input impedance.

Table 2-1. CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1_INTYP	R/W	0h	Channel 1 input type 0d = Microphone input 1d = Line input
6-5	CH1_INSRC[1:0]	R/W	0h	Channel 1 input configuration 0d = Analog differential input (the GPI1 and GPO1 pin functions must be disabled) 1d = Analog single-ended input (the GPI1 and GPO1 pin functions must be disabled) 2d = Digital microphone PDM input (configure the GPO and GPI pins accordingly for PDMDIN1 and PDMCLK) 3d = Reserved
4	CH1_DC	R/W	0h	Channel 1 input coupling (applicable for the analog input) 0d = AC-coupled input 1d = DC-coupled input
3-2	CH1_IMP[1:0]	R/W	0h	Channel 1 input impedance (applicable for the analog input) 0d = Typical 2.5-kΩ input impedance 1d = Typical 10-kΩ input impedance 2d = Typical 20-kΩ input impedance 3d = Reserved
1	Reserved	R	0h	Reserved
0	CH1_DREEN	R/W	0h	Channel 1 dynamic range enhancer (DRE) and automatic gain controller (AGC) setting 0d = DRE and AGC disabled 1d = DRE or AGC enabled based on the configuration of bit 3 in register 108 (P0_R108)

Table 2-2. VREF Programmable Settings

P0_R59_D[1:0] : ADC_FSCALE[1:0]	VREF Output Voltage (Same as Internal ADC VREF)	Differential Full-Scale Input Supported	Single-Ended Full-Scale Input Supported	AVDD Range Requirement
00 (default)	2.75 V	2 V_{RMS}	1 V_{RMS}	3 V to 3.6 V
01	2.5 V	1.818 V_{RMS}	0.909 V_{RMS}	2.8 V to 3.6 V
10	1.375 V	1 V_{RMS}	0.5 V_{RMS}	1.7 V to 1.9 V
11	Reserved	Reserved	Reserved	Reserved

Table 2-3. Input Impedance Selection for the Record Channel

P0_R60_D[3:2] : CH1_IMP[1:0]	Channel 1 Input Impedance Selection
00 (default)	Channel 1 input impedance typical value is 2.5 kΩ on INxP or INxM
01	Channel 1 input impedance typical value is 10 kΩ on INxP or INxM
10	Channel 1 input impedance typical value is 20 kΩ on INxP or INxM
11	Reserved (do not use this setting)

2.2 Input Pin Waveforms with AC Coupling

When a 1-V RMS signal is passed through a coupling capacitor as shown in Figure 2-2, the signal rides over VREF/2.

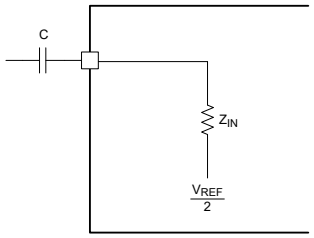

Figure 2-2. Circuit for Input Pin With AC Coupling

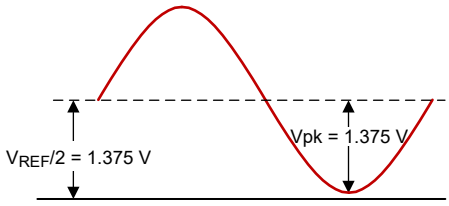

Figure 2-3. Input Pin Waveform With AVDD of 3.3 V

For a 3.3-V supply, a VREF/2 is 1.375 V. The highest point of a 1-V_{RMS} signal on the pin is 2.8 V which is lower then AVDD of 3.3 V. A signal larger then AVDD can not be given to ADC input as that can damage the input pins.

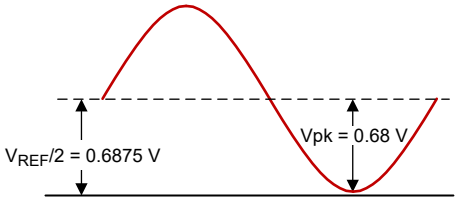

Figure 2-4. Input Pin Waveform With AVDD of 1.8 V

For a 1.8-V supply, a VREF/2 is 0.6875 V. The highest point of a 0.5-V_{RMS} signal on the pin is 1.4 V which is lower then AVDD of 1.8 V.

2.3 Selection of Coupling Capacitor

Since Vref/2 in Figure 2-2 is a DC voltage with low impedance for AC purposes, Vref/2 is considered GND as shown in Figure 2-5.

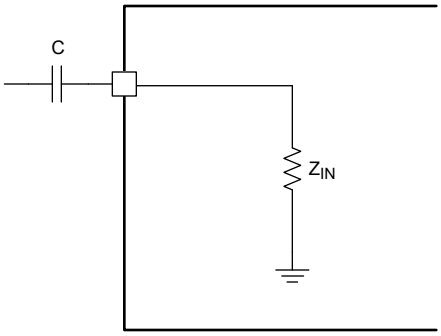

Figure 2-5. AC Equivalent Circuit of Input Pin

The coupling capacitor *C* and Z_{in} form a high pass filter. This filter blocks DC and very low frequencies from reaching the input pin. For audio frequencies the capacitor acts as a short circuit. The cutoff frequency is calculated as follows:

$$Fc = \frac{1}{2 \times 3.14 \times C \times Zin} \tag{2}$$

To pass audio frequencies audible to humans, choose F_{min} = 20 Hz

$$C > \frac{1}{2 \times 3.14 \times F_{min} \times Z_{in}} \tag{3}$$

$$C > \frac{1}{2 \times 3.14 \times 20 \times 2.5\ \text{k}\Omega} \qquad \text{For } F_{min} = 20 \text{ and } Z_{in} = 2.5\ \text{k}\Omega \tag{4}$$

$$C > 3\ \mu\text{F} \tag{5}$$

Having a smaller capacitor is possible, if input impedance is higher or F_{min} is set higher.

Table 2-4. Selection of Coupling Capacitor

F_{min}	Z_{in}	C
20	2500	3.3 u
100	20000	0.1 u

2.4 Quick Charge Circuit

On power-up, the coupling capacitor is charged to the common mode voltage. This charge is done by connecting an internal 800-Ω resistor from pin to Vref/2. This connection is done for a duration of 2.5 ms. This time is enough to charge a 1-u capacitor to Vref/2. This process is called quick charging.

The audio output from the ADC is proper only after the coupling capacitors are charged to the steady state value.

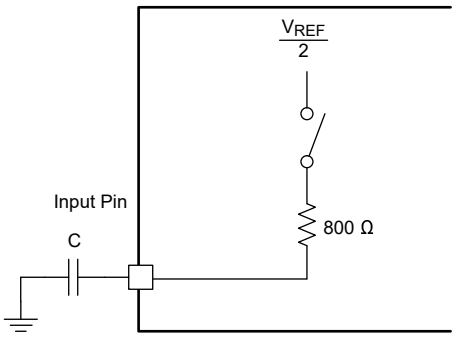

Figure 2-6. Quick Charge Circuit

If the coupling capacitor is larger then 1 uf, the time duration can be set to a higher value by SHDN_CFG Register (P0 R5).

Table 2-5. SHDN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-4	INCAP_QCHG[1:0]	R/W	0h	The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω. 0d = INxP, INxM quick-charge duration of 2.5 ms (typical) 1d = INxP, INxM quick-charge duration of 12.5 ms (typical) 2d = INxP, INxM quick-charge duration of 25 ms (typical) 3d = INxP, INxM quick-charge duration of 50 ms (typical)
3-2	SHDNZ_CFG[1:0]	R/W	1h	Shutdown configuration: 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved
1-0	DREG_KA_TIME[1:0]	R/W	1h	These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical)

The time a RC circuit takes to reach 90% of Supply Voltage is calculated as follows:

$$\mathrm{Tr} = 2.3 \times \mathrm{R} \times \mathrm{C} \quad \mathrm{R} = 800\ \Omega \tag{6}$$

$$\mathrm{Tr} = 1800 \times \mathrm{C} \tag{7}$$

$$\mathrm{Tr1} = 1800 \times \mathrm{C1} \quad \text{For another capacitor C1} \tag{8}$$

$$\mathrm{C1} = \frac{\mathrm{C} \times \mathrm{Tr1}}{\mathrm{T}} \tag{9}$$

$$\mathrm{C1} = \frac{1\ \mu\mathrm{f} \times \mathrm{TR1}}{2.5\ \mathrm{ms}} \quad \text{For TR1} = 12.5\ \mathrm{ms},\ \mathrm{C1} = 4.7\mu\mathrm{f} \tag{10}$$

Table 2-6 lists SHDN_CFG register settings for different values of the coupling capacitor.

Table 2-6. SHDN_CFG register settings

Quick Charge Time	Coupling Capacitor
2.5 ms	1 u
12.5 ms	4.7 u
25 ms	10 u
50 ms	22 u

2.5 Selection of Capacitor Type

Please refer to the *Selecting Capacitors to Minimize Distortion in Audio Applications* analog design journal for choosing a type of coupling capacitors.

2.6 Single-Ended and Differential Mode

The TLV320ADCX12O/PCMX120-Q1 family supports both single-ended and differential signals. A single-ended signal can be sent through a 2-wire connection (input signal, ground). If this signal has to be transmitted over a noisy environment then a shielded cable can be used. The shield is connected to ground acting like a Faraday cage to the signal wire. Noise picked up along the cable length is conducted by the shield to ground.

A differential signal is a 3-wire connection (positive, negative, and ground). Two equal in amplitude and phase inverted signals are sent over the positive and negative lines. The positive and negative lines need to run very close to each other. A shielded twisted pair is one way to route differential signals.

Noise signals picked up on both positive and negative lines are identical waveforms provided the lines run close to each other. These are termed Common Mode Signals. The TLV320ADCX12O/PCMX120-Q1 family has a

common mode rejection of 60 db. The differential input circuit of the ADC only processes the out-of-phase signal on the positive and negative pins. The signal attenuates the common mode noise signals by 60 db providing a great benefit by picking up a valid audio signal in an extremely noisy environment.

Table 2-7 shows the setup of the input as single-ended or differential.

Table 2-7. Input Source Selection for the Record Channel

P0_R60_D[6:5]: CH1_INSRC[1:0]	Input Channel 1 Record Source Selection
00 (default)	Analog differential input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled)
01	Analog single-ended input for channel 1 (this setting is valid only when the GPI1 and GPO1 pin functions are disabled)
10	Digital PDM input for channel 1 (configure the GPIx and GPOx pin accordingly for PDMDIN1 and PDMCLK)
11	Reserved (do not use this setting)

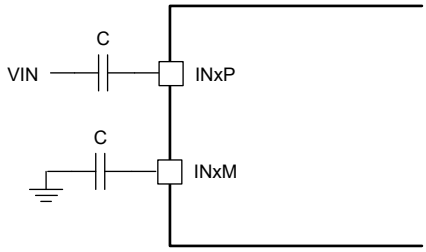

Figure 2-7. Single-Ended AC Coupled Circuit

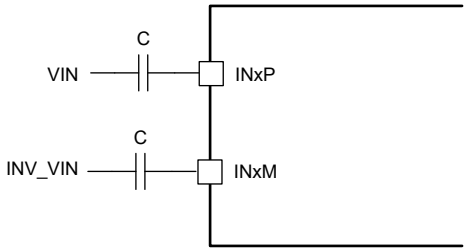

Figure 2-8. Differential AC Coupled Circuit

- DC Bias on input pins is internally fixed at Vref/2.
- For the differential mode, V_{in} and ^V_{in} are phase inverted signals.

Table 2-8 shows the analog signal levels that correspond to Full Scale Digital Value (0 dBFS).

Table 2-8. Analog Signal Levels

AVDD	VREF/2	VRMS Single Ended	VRMS Differential
3.3 V	1.375 V	1 VRMS	2 VRMS
1.8 V	0.6875 V	0.5 VRMS	1 VRMS

2.7 S.N.R in AC Coupled Circuits

The TLV320ADCX120 can also support a higher input common-mode tolerance at the expense of noise performance by a few decibels. The device supports three different modes with different common-mode tolerances, which can be configured using the CH1_INP_CM_TOL_CFG[1:0] (P0_R58_D[7:6]) register bits. Mode 0 gives the lowest noise performance.

Table 2-9. Common-Mode Tolerance Mode Selection for Record Channel

P0_R58_D[7:6] : CH1_INP_CM_TOL_CFG[1:0]	Channel 1 Input Common-Mode Tolerance
00 (default)	Channel 1 input common-mode tolerance: AC-coupled input = 100 mV_{PP}, DC-coupled input = 2.82 V_{PP}.
01	Channel 1 input common-mode tolerance: AC/DC-coupled input = 1 V_{PP}.
10 (high CMRR mode)	Channel 1 input common-mode tolerance: AC/DC-coupled input = 0-AVDD (supported only with an input impedance of 10 kΩ and 20 kΩ). For input impedance of 2.5 kΩ, the input common-mode tolerance is 0.4 V to 2.6 V.
11	Reserved, do not use this setting.

The highest performance for the ADC is obtained in AC coupling mode. To achieve the highest performance, the following setup must be implemented.

- AC coupled mode
- Differential operation
- Mode 0 in page 0, register 58
- Z_{in} = 2.5 k
- DRE Enabled
- PGA Gain -0 db

For the TLV320ADC6120 device, the performance in Table 2-10 is achieved with the prior settings.

Table 2-10. SNR Data

	SNR (DRE ON) dB	SNR (DRE OFF) dB
Single-Ended	118	111
Differential	122	112

3 DC Coupled Scheme

DC Coupled systems eliminate the need for coupling capacitors. The system has the following advantages

- Lower bill of material cost and less board space.
- Performance degradation due to imperfections in capacitors can be eliminated. This degradation includes THD degradation at low frequency and board vibration effects.
- Start-up pop is eliminated.
- The ADC works down to DC which opens up the possibility to do measurements such as voltage and current for test and measurement.

DC coupled systems have the following disadvantages:

- The DC biasing of the input pins is not determined by the ADC circuit but by the external source. Since the biasing is not always optimum, the ADC can display a reduced signal handling.
- In DC Coupling, DC differences between the INxP and INxM pins appear as an offset at the output of the ADC which can lead to saturation of the ADC output at high PGA gains; therefore, high PGA gains are not always possible with DC coupling.
- The Dynamic Range Extension (DRE) functionality of the ADC relies on adapting the PGA Gain. This functionality can also be limited in DC coupled applications.
- CH1_CFG0 Register (Address = 0x3C) Bit 4, CH1_DC=1 selects DC Coupling for Channel1.

Figure 3-1 describes the signal processing for DC Coupling.

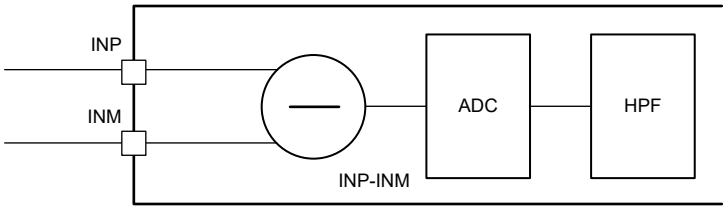

Figure 3-1. Input Signal Processing

The circuit digitizes (InxP-InxM).

For common mode signals, INxP = InxM.

InxP-InxM = 0. Common mode signals such as noise create a zero input to the ADC and are not digitized.

DC offset present in the input can be removed by the high pass filter.

3.1 Biasing the Pins

Case 1: When INxP and INxM have the same static DC voltage.

$INxP - INxN = 0$. There is no DC offset in the digitized data; however, if the DC levels on the pins are close to V_{AVDD} or V_{GND}, there is reduced headroom for AC signals. The optimum bias level for the two pins is $V_{REF}/2$. At this level, a differential range of 2 VRMS is supported.

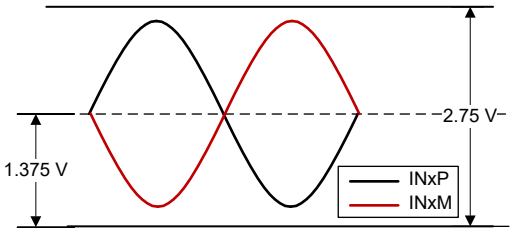

Figure 3-2. Optimum Biasing 1.375 V_{DC} on INxP and INxM Pins

As shown in Figure 3-2, a 1-Vrms signal is added on a DC voltage of 1.375 V. The waveforms at INxP and INxM are 180° out-of-phase. At no point does the waveform exceed 3.3 V or go below 0 V. Thus, the analog signal of 2-Vrms differential corresponding to full scale digital data can be given to the ADC pin without distortion.

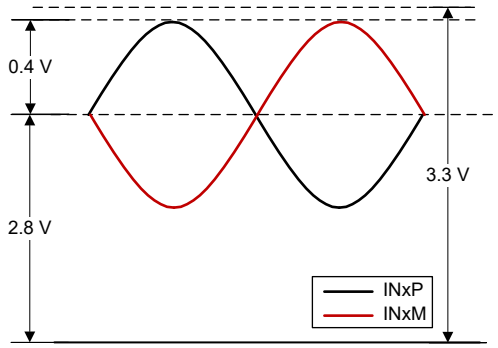

Figure 3-3. Biasing INxP and INxM at a Higher Voltage

Figure 3-3 shows the pins bias at 2.8 VDC.

A larger AC signal results in the pin waveform exceeding 3.3 V and clipping. This process results in harmonic distortion; therefore, the signal handling is reduced to 1 Vp differential.

The Figure 3-4 shows a 500-mV (peak) signal with a DC offset of 2.5 V. A larger signal results in harmonics appearing on the FFT.

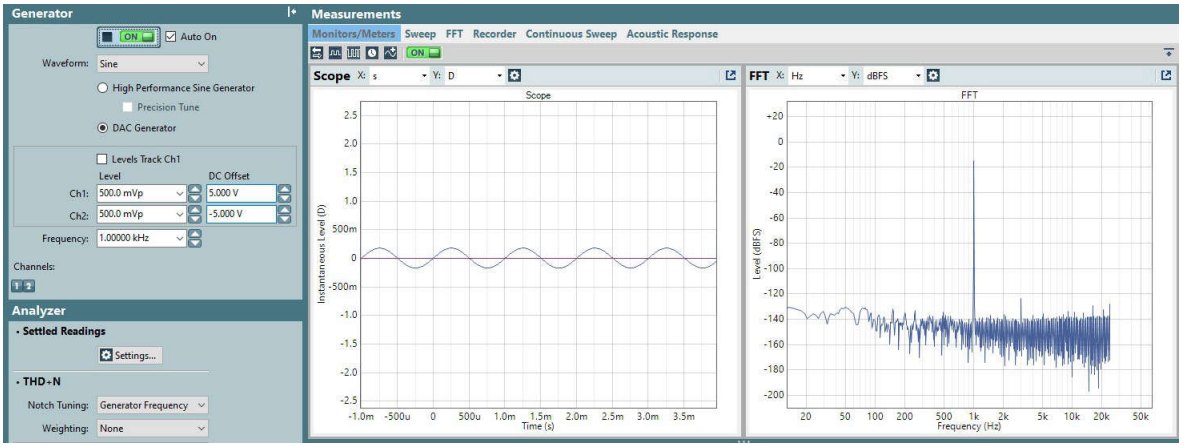

Figure 3-4. 0.5-V Pk Signal on DC Bias of 2.5-V-Input Pin Waveform and Digital Capture

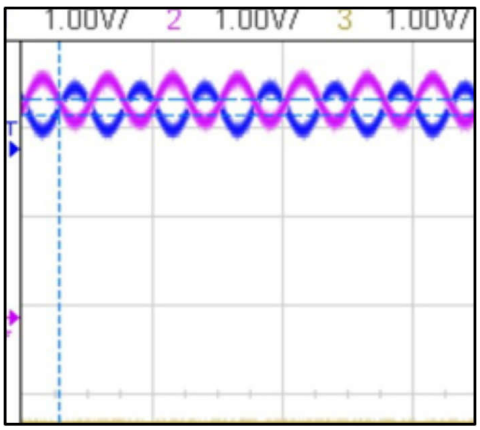

Figure 3-5. Input Pin Waveform 0.5-V Pk Signal on DC Bias of 2.5 V

Case 2: When InxP and InxM have a different static DC voltage.

INxP minus INx0 is not equal to zero. There is a DC offset. The internal Digital High Pass Filter can be used to remove this DC offset. If the DC Levels on the pins are close to AVDD or ground, there is reduced headroom for AC signals. The protection diode turns on if the voltage on the input pin exceeds AVDD or is less than ground.

Note

If given a PGA gain, the static DC level at the input also gets a gain. Setting too high a PGA gain leads to the output of the PGA saturating.

Figure 3-6 illustrates an example of pin waveforms on INxP and INxM with different static DC levels.

Let INxP = 2.25 V and INxM = 0.75 V be the static DC levels on the input pins.

Figure 3-6 shows the waveforms on the input pins. Make sure that the pin levels do not exceed 3.3 V or go below 0 V.

Figure 3-6 also shows the difference (INxP – INxM). There is a DC offset of 1.5 V which is seen in ADC output. The digital high pass filter removes this offset.

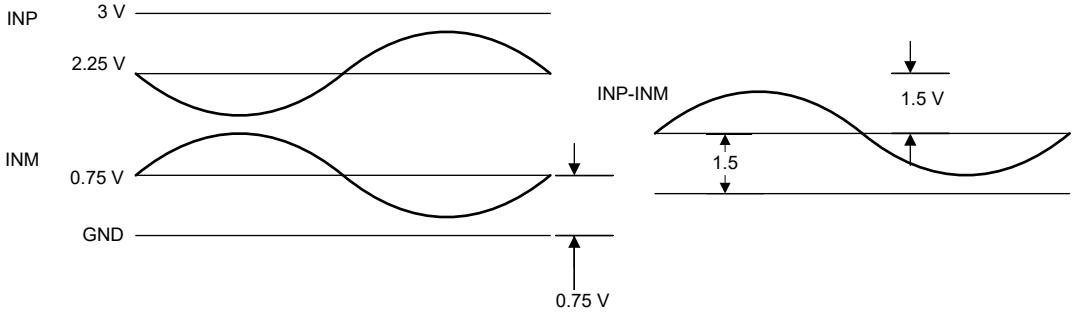

Figure 3-6. Input Pin Waveforms With Different Static DC Levels

Figure 3-7 shows a 1-Vrms signal with a DC offset of 1.5 V. A larger signal can result in harmonics appearing on the FFT.

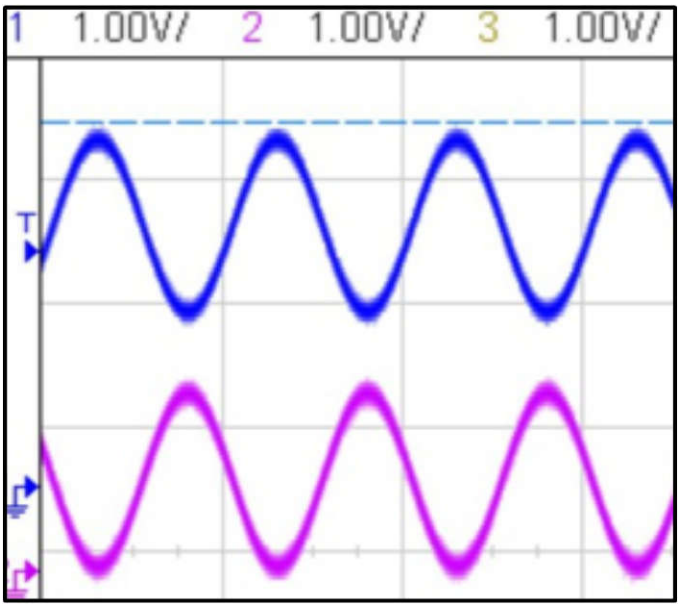

Figure 3-7. Waveforms at INxP and INxM Pins

The DC offset between the two input pins can be seen at the digital output capture if HPF_SEL has 00b which enables an all pass filter.

If HPF_SEL is set for high-pass filter, this DC component is removed in the digital output capture.

Table 3-1. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
1-0	HPF_SEL[1:0]	R/W	1h	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 × f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 × f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 × f_S (384 Hz at f_S = 48 kHz) is selected

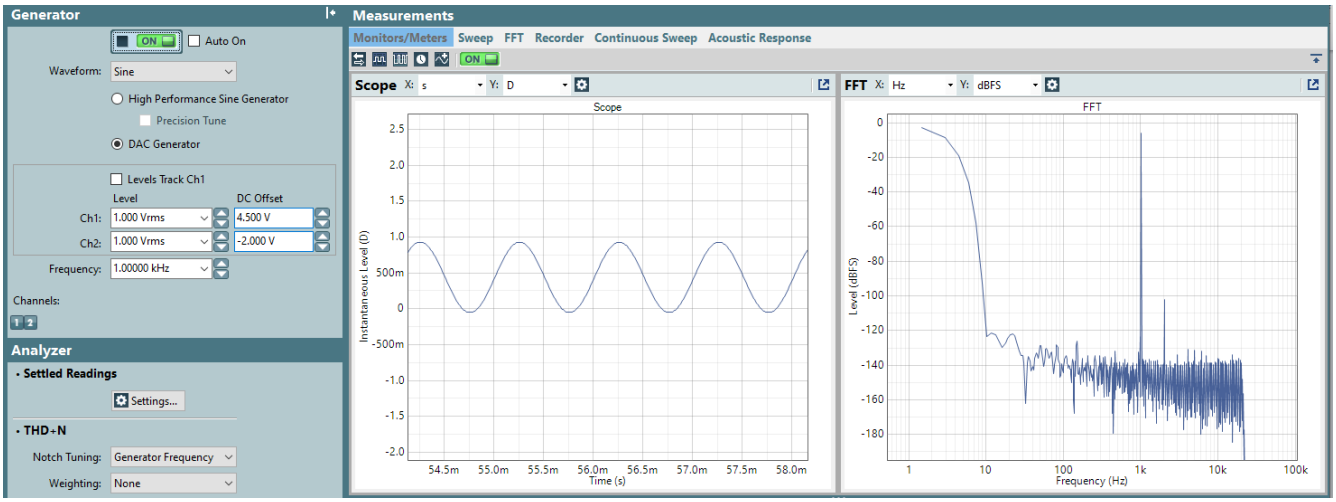

Figure 3-8. Digital Capture With All Pass Filter - DC Offset is Seen

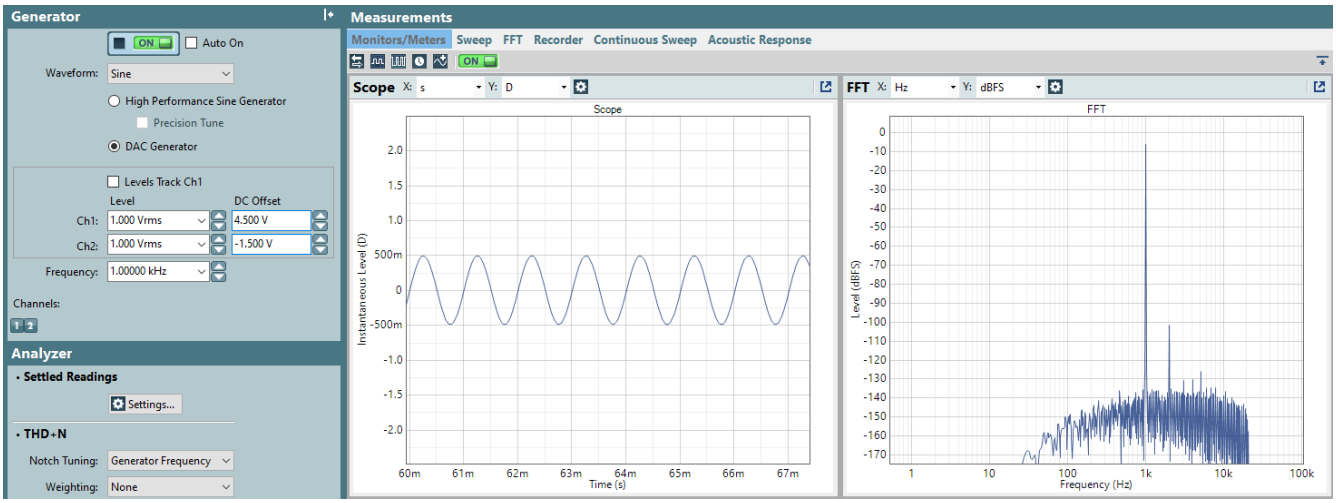

Figure 3-9. Digital Capture With Low-Pass Filter

3.2 Electrical Characteristics

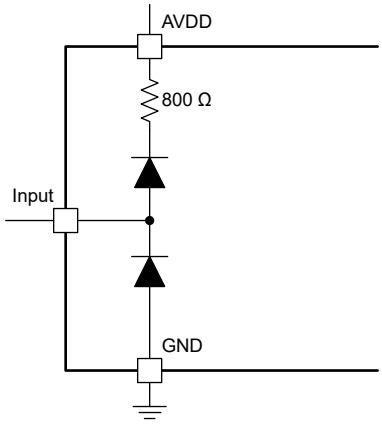

Figure 3-10. Protection Circuit on Input Pin

The input pins have protection diodes that start conducting when the pin voltage exceeds +0.3 V above AVDD or falls below –0.3 V. The maximum current that can be conducted in these diodes is 10 mA. Soft clipping begins when the voltage at the input pin exceeds 3.6 V. This clipping creates harmonic distortion. When the pin voltage falls below –0.3 V, hard clipping begins.

The voltage level on the analog input pin must stay between V_{AVDD} and V_{GND} for best performance and reliable operation.

Figure 3-11 shows the electrical model of the input pins. The source impedance must be lower than the input impedance.

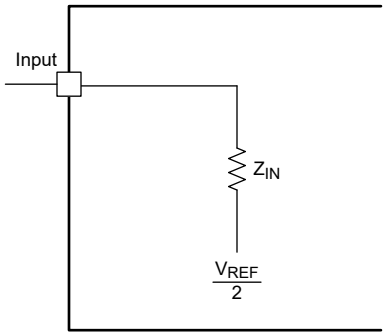

Figure 3-11. Equivalent Circuit of Input Pin

3.3 Application Circuits

For a single-ended input, the static DC bias at the input pin V_{IN} must remain between 0 and V_{ref}. An optimum static DC bias for the input pin is Vref/2. For a Vref of 2.75 V, the bias level is 1.375 V enabling a 1-Vrms signal to be coupled to the ADC.

The static DC bias of 1.375 V appears as a DC offset at the output of the ADC. Selection of the digital high-pass filter removes the DC offset from the digital data.

The static DC bias is amplified by setting a PGA gain.

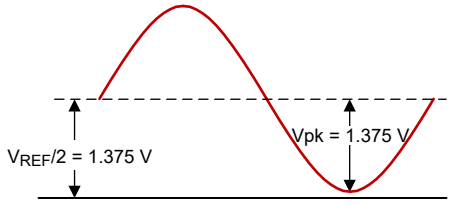

Figure 3-12. Single-Ended DC Coupled Waveform

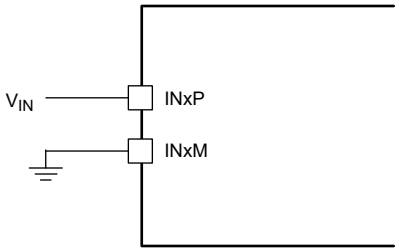

Figure 3-13. Single-Ended DC Coupled Circuit

For a differential input, the V_{IN} and INV_VIN Signals can have a static DC bias between 0 and AVDD. An optimum static bias is Vref/2 for both V_{IN} and INV_VIN signals. With a Vref of 2.75 V, the optimum static bias is 1.375 V which supports a differential 2-Vrms signal to be coupled to the ADC.

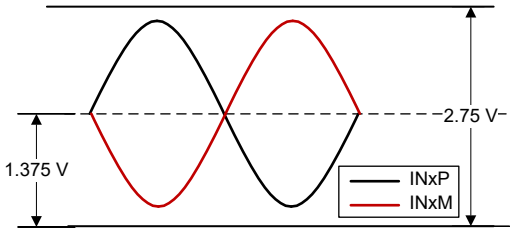

Figure 3-14. Differential DC Coupled Signal

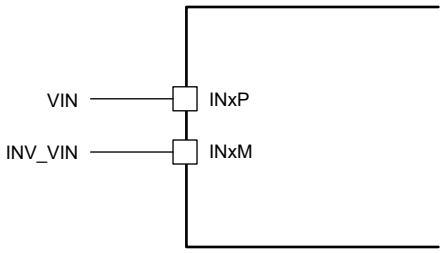

Figure 3-15. Differential DC Coupled Circuit

If V_{IN} and INV_VIN have the same static DC bias, then no DC offset exists at the output of the ADC.

The waveforms at V_{IN} and INV_VIN are 180 degrees out of phase with each other.

Table 3-2 lists input signal levels that correspond to full scale digital value.

Table 3-2. Input Signal Levels

AVDD (V)	V_{REF}/2 (V)	Vrms	
		Single Ended (V)	Differential (V)
3.3	1.375	1	2
1.8	0.6875	0.5	1

3.3.1 S.N.R in DC Coupled Circuits

A low noise performance as well as good common mode handling can be obtained by using the setup below.

- Differential operation. Static DC difference voltage between input pins is 0 V.
- Mode 1. REGISTER R58 _D(7-6)
- Z_{in} = 10 K
- DRE Enabled
- PGA gain: -0 db.

For the TLV320ADC6120 device, the SNR in Table 3-3 is achieved.

Table 3-3. SNR

SNR(DRE ON) dB	SNR(DRE OFF) dB
112	108

For a DC-coupled input, the DRE scheme can be used with limited DRE_MAXGAIN depending on the DC differential input common-mode offset.

4 Application Examples

4.1 Electret Condenser Microphone: Single Ended DC- Coupled Input

Features: Low component count

This application uses POM-2730L-HD-R microphone with TLV320ADC6120 ADC.

POM-2730L-HD-R specifications: R_O = 2200 Ω.

TLV320ADCX120 Settings:

- V_{REF} = 2.75 V
- Z_{IN} = 10 kΩ to maintain the input impedance does not load the bias circuit
- Analog single-ended
- DC coupled
- P0_R58 (7:6) is set at Mode 1
- DRE Disabled

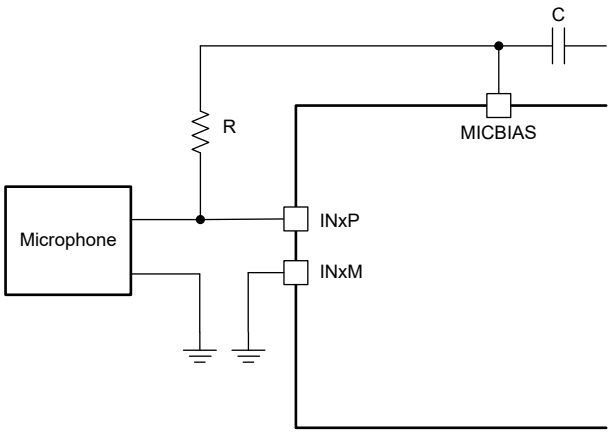

Figure 4-1. Single-Ended DC Coupled Condenser Microphone Circuit

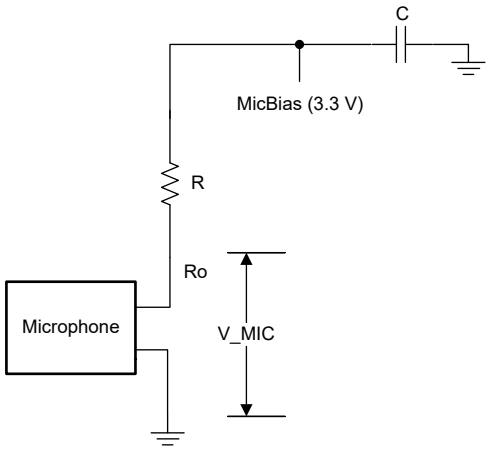

Figure 4-2. DC Bias Circuit for Microphone

Figure 4-2 shows that R_O (output impedance of mic) forms a voltage divider with the bias resistor. Bias microphone output pin to 1.375 VDC to bring ADC input to the optimum level.

$$\text{ADC input} = \frac{3.3 \times R_O}{R + R_O} = 1.375(V) \quad (11)$$

$$R = 3\ k\Omega \quad (12)$$

- A signal of 1 V_{RMS} from the microphone can be handled without clipping at the input pin.
- The ADC output has a DC offset corresponding to 1.375 V. This offset has to be removed by the internal high pass filter.

4.2 Electret Condenser Microphone: Single Ended AC Coupled Input

Features: high performance

This application uses a POM-2730L-HD-R microphone with the TLV320ADC6120 ADC.

POM-2730L-HD-R Specifications:

R_O = 2200 Ω.

LV320ADCX120 Settings:

- V_{REF} = 2.75 V
- Z_{IN} = 10 kΩ
- Analog single ended

- AC coupled
- P0_R58[7:6] set at Mode 0
- DRE enabled

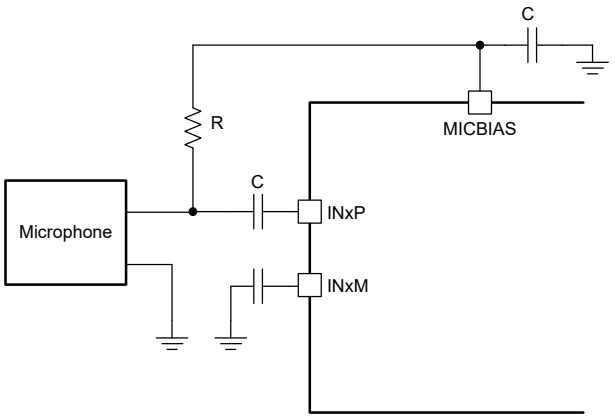

Figure 4-3. Single-Ended AC Coupled Condenser Microphone Circuit

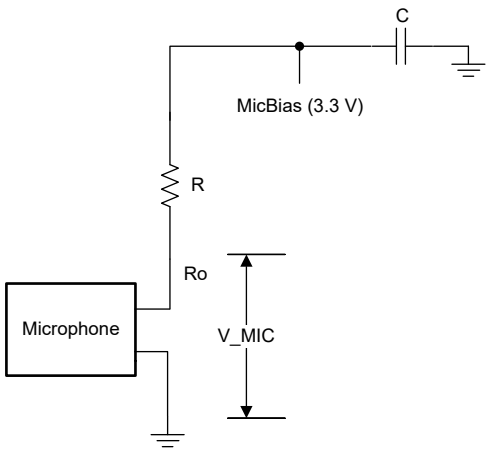

Figure 4-4. Single-Ended AC Coupled Condenser Microphone Test

As shown in Figure 4-3 and Figure 4-4, R_O (the output impedance of the microphone) forms a voltage divider with the bias resistor. The application biases the microphone output pin to 1.375 VDC to bias ADC circuit at center.

$$\text{ADC bias input} = \frac{3.3 \times R_O}{(R + R_O)} = \frac{3.3 \times 2200}{(R + 2200)} = 1.375(V) \quad (13)$$

R = 3 kΩ

Choose C = 3.3 µF to allow a frequency response as low as 20 Hz.

In this application, the open circuit voltage of the microphone is VMic.

$$V_{IN(ADC)} = \frac{V_{MIC} \times Z_{IN}}{R + Z_{IN}} \quad (14)$$

To prevent this loading, maintain Z_{IN} >>R.

4.3 Selection of a Microphone

This implementation uses the POM-2730L-HD-R microphone with TLV320ADC6120 ADC. The device is setup as a single-ended AC-coupled input.

Sensitivity: -30 db, 0 db = 1 V/Pascal with load resistor.

Output Impedance: 2.2 kΩ

SNR: 74 db, SPL of 94 db, or 1 Pascal

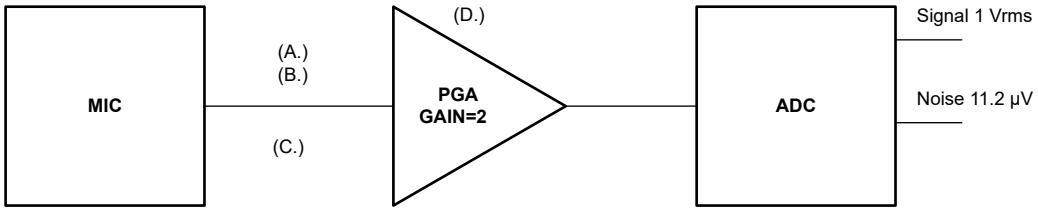

Figure 4-5. Noise in Signal Chain

A. Microphone noise = 4 µV
B. Input referred noise = 4 µV
C. Noise at input = microphone noise + input referred noise = 5.6 µV
D. Noise = 5.6 µV × 2 = 11.2 µV

For this function, DRE is disabled.

Signal Level at SPL of 94 db

$$-30\ \text{db} = 20 \times \log(\text{VsigPk}) \tag{15}$$

$$\text{VsigPk} = 31.6\ \text{mv} \tag{16}$$

Microphone Output Noise

$$20 \times \log\left(\frac{\text{Vsig}}{\text{Vnoise}}\right) = \text{SNR} \tag{17}$$

$$20 \times \text{Log}\left(\frac{31.6\ \text{mv}}{\text{Vnoise}}\right) = 74\ \text{db} \tag{18}$$

$$\text{Vnoise} = 6.4\ \text{uvpk} \tag{19}$$

$$\text{Vnoise} = 4.4\ \text{uvrms} \tag{20}$$

Dynamic Range of Mic

120 db SPL is considered the overload level for this mic.

The difference from 94 db SPL level is:

$$120\ \text{db} - 94\ \text{db} = 26\ \text{db} \tag{21}$$

94 db SPL is the reference for SNR which is 74 db.

Add 26 db to SNR to get the dynamic range.

$$\text{Dynamic range} = 74\ \text{db} + 26\ \text{db} = 100\ \text{db} \tag{22}$$

Dynamic range of mic = 100 db.

Estimation of PGA Gain

The signal level at the overload point is:

$$-30\ \text{db} + 26\ \text{db} = -4\ \text{db} \tag{23}$$

$$-4\ \text{db} = 20 \times \log(\text{Vsig Pk}) \tag{24}$$

$$\text{Vsig Pk} = 0.63\ \text{V} \tag{25}$$

For a single-ended AC-coupled input the full-scale value is 1 VRMS or 1.4 Vpk.

$$\text{PGA Gain} = \frac{1.4}{0.63} = 2.2 \tag{26}$$

Estimation of SNR of Mic + ADC

Mic noise 4.4 uvrms equals V1.

Input referred noise of ADC with PGA gain of 2:

$$4\ \text{uvrms} = \text{V2} \tag{27}$$

Effective noise at input of ADC 5.65 uvrms:

$$Ve = \sqrt{V1^2 + V2^2} \tag{28}$$

Effective noise at output of PGA 11.2 uvrms:

$$5.65\ \text{uv} \times \text{PGA Gain} \tag{29}$$

The following is the noise that is seen at the output of the ADC:

$$\text{SNR of the system SNR} = 20 \times \text{Log}\left(\frac{1}{\text{V}_\text{n}}\right) \tag{30}$$

$$\text{SNR} = 20 \times \text{Log}\left(\frac{1}{11.3\ \mu\text{v}}\right) \tag{31}$$

SNR is 98.9 db. The system is able to capture sound up to the noise floor of the microphone.

4.4 Condenser Microphone: Differential DC-Coupled Input

Features: Good common mode rejection - 80 db

This implementation uses the POM-2730L-HD-R microphone with TLV320ADC6210 ADC.

POM-2730L-HD-R Specifications:

Sensitivity -30db 0db=1V/Pascal with load resistor, output impedance 2.2 kΩ, SNR 74 db SPL of 94 db or 1 Pascal.

TLV320ADCX120 Settings:

- Vref = 2.75 V
- Z_{in} = 10 kΩ
- DC coupled
- Analog differential input
- P0_R58 (7:6) is set at mode 1
- DRE disabled

The following figures illustrate the circuit for a electret condensor microphone set up to give a differential output.

The output stage of an electret condenser microphone is a FET element. A pull-up to MicBias and pull-down to ground results in the circuit working as a phase splitter. With an incoming sound input, the INxP and INxM pins are moving in phase opposition. When the level of INxP reduces, the level of INxM increases. To achieve the maximum undistorted signal handling, the voltage difference between INxP and INxM must always be greater then zero at the peak of the signal. This keeps the FET element of the microphone working in linear range.

For maximum signal handling the static DC bias across the microphone terminal is kept at VMICBIAS/2.

$$\frac{\text{VMICBIAS} \times \text{Ro}}{2\text{R} + \text{Ro}} = \text{V MIC} \tag{32}$$

$$\text{For VMIC} = \frac{\text{VMICBIAS}}{2} \tag{33}$$

$$\text{R} = \text{Ro}/2 \tag{34}$$

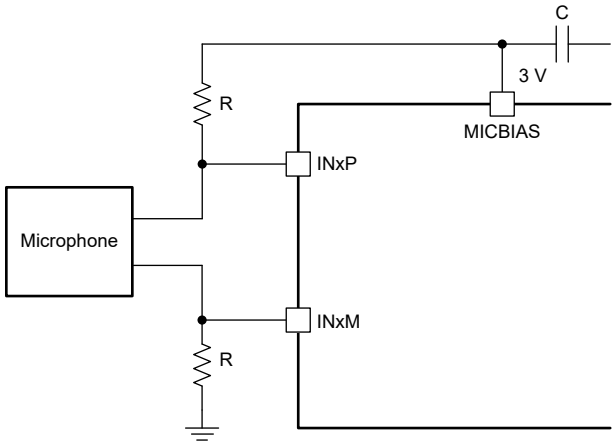

Figure 4-6. DC- Coupled Differential Microphone

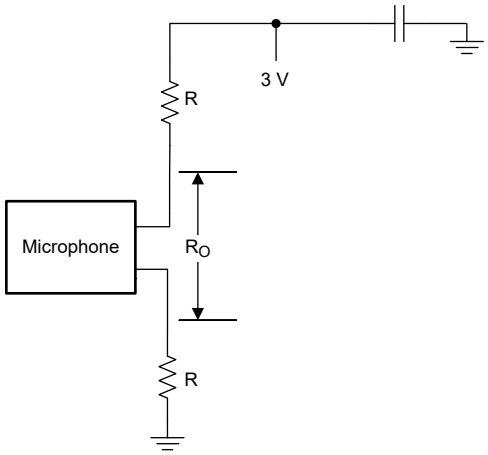

Figure 4-7. DC Bias for Microphone

In this system $\text{R} = \frac{\text{R}_\text{O}}{2} = 1100\ (\Omega)$.

$$\text{V}_\text{INXP} = \frac{3 \times (\text{R} + \text{R}_\text{O})}{(2\text{R} + \text{R}_\text{O})} = 2.25(\text{V}) \tag{35}$$

$$\text{V}_\text{INXM} = \frac{3 \times \text{R}}{(2\text{R} + \text{R}_\text{O})} = 0.75\ (\text{V}) \tag{36}$$

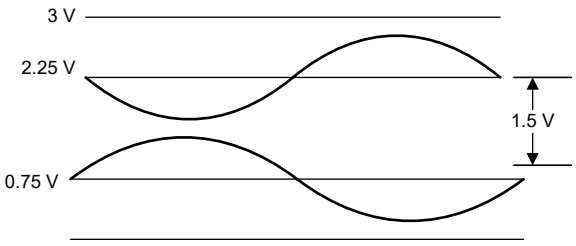

Figure 4-8. Waveform DC-Coupled Differential Microphone

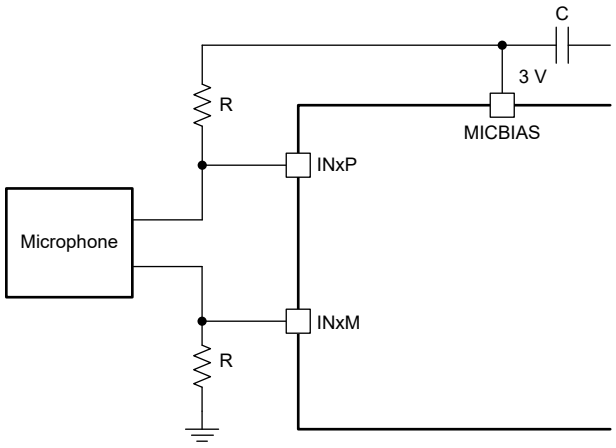

Figure 4-9. Circuit DC-Coupled Differential Microphone

The DC level on the INxP and INxM pins without any audio signal is 2.25 V and 0.75 V respectively. Sounds received by the microphone result in out-of-phase signals on the pins as shown by the figure.

1-VRMS differential signal can be digitized by this circuit.

- An economy circuit shown below uses a condenser microphone placed at a distance from the ADC.
- The connecting cable can be inexpensive twisted cable or even an ordinary two-core wire. This is a differential application which relies on the good CMRR of the device to remove noise even with an inexpensive cable.
- Microphone needs no separate PCB or power supply.

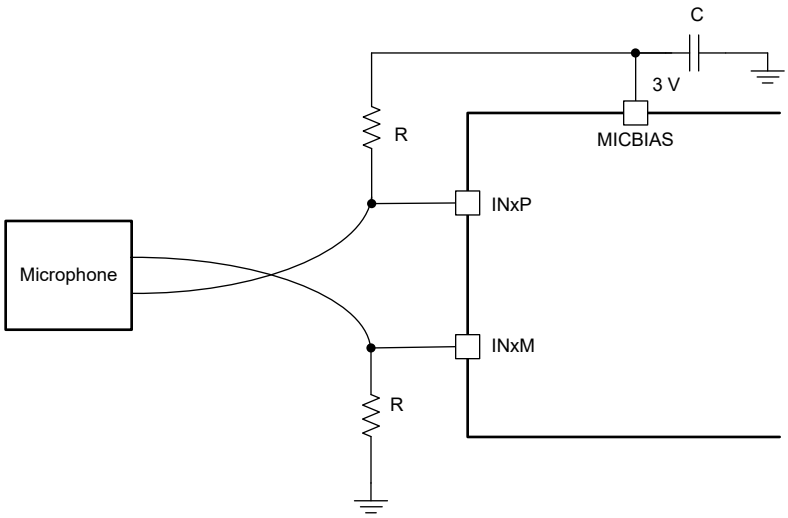

Figure 4-10. Economy Circuit

4.5 Condenser Microphone: Differential AC-Coupled Input

Features: High SNR for far field voice recording

Select the POM-2730L-HD-R microphone with TLV320ADC6120 ADC.

POM-2730L-HD-R Specifications:

Sensitivity -30 db, 0 db = 1 V/Pascal with optimum load resistor. Output Impedance 2.2k, SNR 74 db SPL of 94 db or 1 Pascal.

TLV320ADCX120 Settings:

- Vref = 2.75 V
- Z_{in} = 2.5 kΩ
- AC Coupled
- Analog differential input. P0 R58 (7:6) = mode 0
- DRE ON

The microphone can be modeled as a current source where the output current is proportional to the incoming sound pressure. The voltage of this source is IxR and the output impedance is R. I is output current and R is the biasing resistance of the mic circuit.

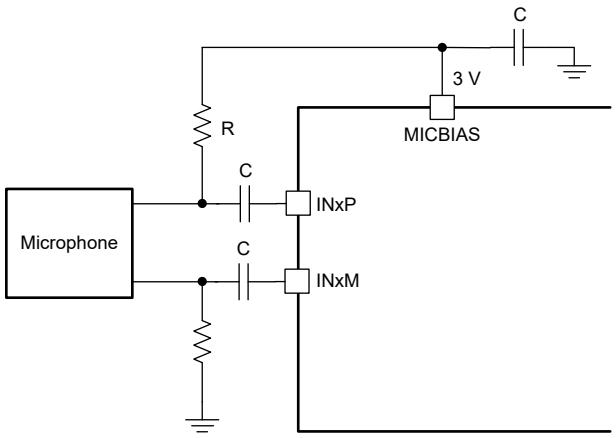

Figure 4-11. AC Coupled Differential Microphone Circuit

$$C > \frac{1}{2 \times 3.14 \times Fmin \times (Zin + R)} \tag{37}$$

$$C > \frac{1}{2 \times 3.14 \times 20 \times (2.5\text{K} + 1.1\text{K})} \quad \text{For Fmin} = 20 \text{ and Zin} = 2.5\text{k} \tag{38}$$

$$\text{C} > 2.2\text{uf} \tag{39}$$

4.6 MEMS Microphone: Differential AC Coupled Input

Specifications of ICS 40740

Output impedance = 355 ohms. Output DC Offset is 1.07 V.

Belden 8760 Cable: capacitance/m = 240 p, length is 5 m.

TLV320ADCX120 Settings:

- Vref = 2.75 V
- Zin = 2.5k
- AC coupled
- Analog differential input. P0 R58 (7:6) = Mode 0
- DRE ON

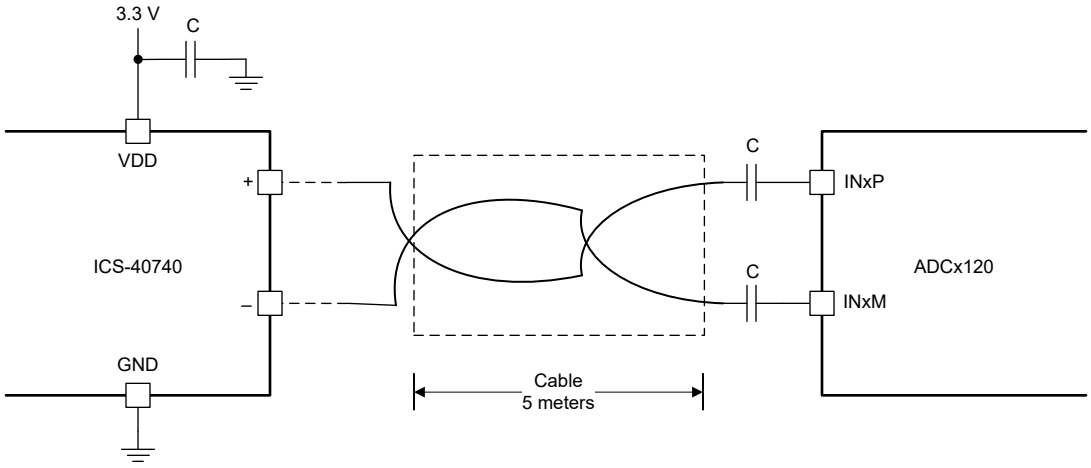

Figure 4-12. MEMS Microphone Connected Through Long Cable to ADC

The ADC can handle 1-VRMS signals that can appear from the mic. In addition, this system has excellent rejection of common mode signals.

Estimation of coupling capacitor C:

$$\text{Cutoff Frequency Fc} = \frac{1}{2 \times 3.14 \times \text{C} \times \text{Z}_{\text{in}}} \; F_C = 20 \text{ Hz} \tag{40}$$

$$\text{For } \text{Z}_{\text{in}} = 2500 \;\; \text{C} > \frac{1}{2 \times 3.14 \times 20 \times 2500} \tag{41}$$

$$\text{C} > 3 \text{ µf} \tag{42}$$

$$\text{Signal level on ADC} \;\; \text{Vin} = \text{VS} \times \frac{\text{Zin}}{\text{R}_\text{O} + \text{Zin}} \quad \text{R}_\text{O} = 355, \;\; \text{Zin} = 2500 \; \Omega \tag{43}$$

Effects of Long Cable:

A twisted pair cable such as Belden 8760 gives 240 p/m capacitance. For 5 m length this is 1.2 n. The output impedance of the mic forms a low pass filter with cable capacitance and this limits the frequency response.

The equation below indicates that long cables can drive signal from this MEMS mic into the ADC.

$$Fc = \frac{1}{2 \times 3.14 \times 1200pf \times 355} = 373khz \tag{44}$$

4.7 Circuit With No Offset and Response Down to DC

As shown in Figure 4-13 and Figure 4-14, the all-pass filter of the ADC is switched on to achieve a frequency response down to DC. Turning on the all-pass filter results in a DC offset at the output, which is controlled by the DSP_CFGO register.

Table 4-1. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-4	DECI_FILT[1:0]	R/W	0h	Decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved

Table 4-1. DSP_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CH_SUM[1:0]	R/W	0h	Channel summation mode for higher SNR 0d = Channel summation mode is disabled 1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 and a (CH3 + CH4) / 2 output 2d = 4-channel summation mode is enabled to generate a (CH1 + CH2 + CH3 + CH4) / 4 output 3d = Reserved
1-0	HPF_SEL[1:0]	R/W	1h	High-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter 1d = HPF with a cutoff of 0.00025 × f_S (12 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.002 × f_S (96 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 × f_S (384 Hz at f_S = 48 kHz) is selected

To remove the DC offset, the INxM pin DC voltage is equal to the average level on the V_{IN} pin resulting in the DC offset removed at ADC output.

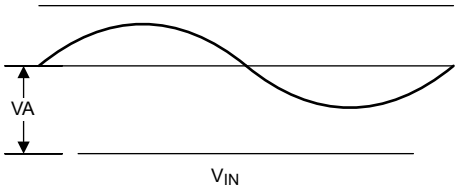

Figure 4-13. Waveform

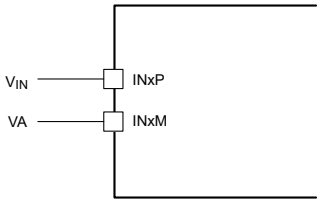

Figure 4-14. Circuit

4.8 Improving SNR by Summing the Output of 2 ADC Channels

By using P0_R107_D (3:2), we can average the digitized data of channel 1 and 2 and make the average the digitized output of the IC.

Table 4-2. Channel Summing Mode Programmable Settings

P0_R107_D[3:2] : CH_SUM[1:0]	CHANNEL SUMMING MODE FOR INPUT CHANNELS	SNR AND DYNAMIC RANGE BOOST
00 (default)	Channel summing mode is disabled	Not applicable
01	Output channel 1 = (input channel 1 + input channel 2) / 2	Around 3-dB boost in SNR and dynamic range
	Output channel 2 = (input channel 1 + input channel 2) / 2	
10	Reserved (do not use this setting)	Not applicable
11	Reserved (do not use this setting)	Not applicable

By giving the same analog input voltage to both ADC inputs on the chip, we can realize a 3 db SNR Boost.

$$\text{SNR} = \text{Full Scale Value}\frac{(\text{V})}{\text{Noise}(\text{V}_\text{n})} \tag{45}$$

$$\text{SNR} = \frac{\text{V}}{\text{V}_\text{n}} \tag{46}$$

On summing two digital outputs:

$$\text{SNR}_\text{A} = \frac{2\text{V}}{\sqrt{\text{Vn}^2 + \text{Vn}^2}} \tag{47}$$

$$\text{SNR}_\text{A} = 1.414 \times \text{SNR} \tag{48}$$

$$\frac{\text{SNR}_\text{A}}{\text{SNR}} = 3 \text{ db} \tag{49}$$

A 3 db boost in SNR is achieved.

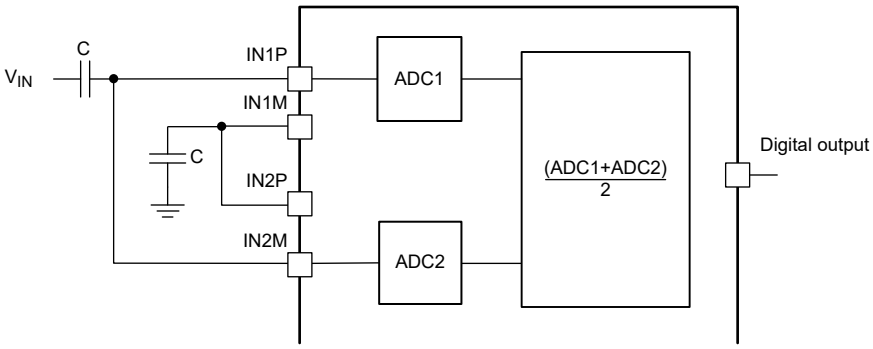

Figure 4-15. Summing Circuit to Improve SNR

Shorting two inputs reduces the input impedance by half. For a Zin of 2.5 K, the effective Zin becomes:

$$\frac{2.5\,K}{2} = 1.25\,K \tag{50}$$

$$C = \frac{1}{2 \times 3.14 \times FM_{in} \times Z_{in}} \tag{51}$$

$$C > \frac{1}{2 \times 3.14 \times 20 \times 1250}\ C > 6.3\ \mu f \tag{52}$$

4.9 Measure a High Voltage Waveform (+-50 V)

Use the below arrangement in Figure 4-16. Vin is a +-50 V waveform. This arrangement uses mic bias to create the 1.375 V which determines the common mode at the input of the ADC.

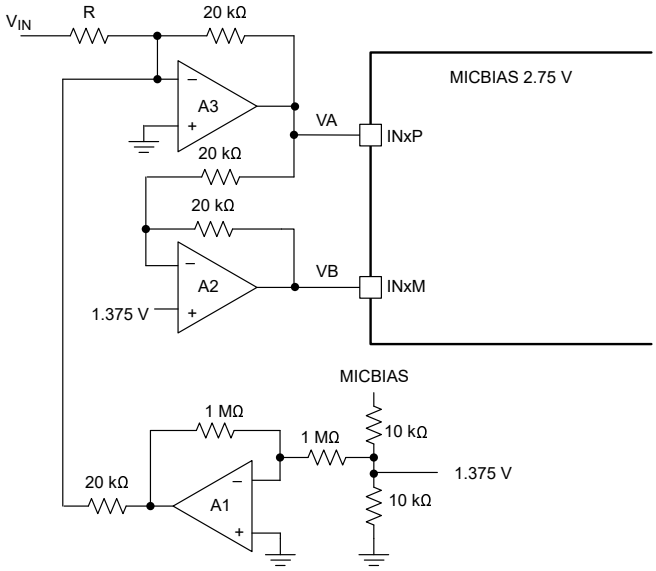

Figure 4-16. Circuit to Digitize 100 V PP Signal

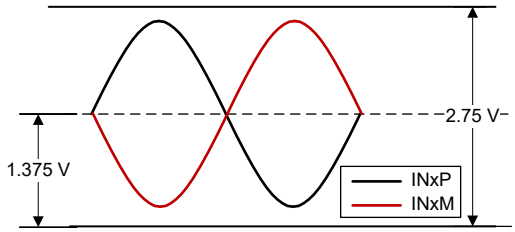

Figure 4-17. Input Pin Waveforms at INxP and INxM

Operate the OP AMP with a +- 3.3V dual supply.

Op amp A3 creates -1.375 V at the output and at INxP, creating a current of 1.375/20 kΩ into the input pin of A3. This creates a DC Level of 1.375 V on the output of A3. The output of A2 is also biased at 1.375 V.

A 50-V positive signal brings the INxP point from 1.375 V to 0 V. As shown in the equations below a R of 720 KΩ is used with a +-50 V input signal.

$$\frac{V_{in}}{R} = \text{In Inverting pin of A3 is at virtual gnd}. \quad (53)$$

$$\text{In} \times 20\ \text{k}\Omega = 1.375\ \text{V}.\ \text{This brings output of A3 from 1.375 V to zero}. \quad (54)$$

$$V_{in} \times \frac{20\ \text{k}\Omega}{R} = 1.375\ \text{V} \quad (55)$$

$$R = V_{in} \times 20\ \text{k}\Omega / 1.375\ \text{V} \quad (56)$$

4.10 I2C Listing

Condenser Microphone: Single Ended DC Coupled Input

The circuit below is of a DC coupled condenser microphone. A MicBias of 3.3 V is setup and a biasing resistor of 3 k is used setting up a Static DC level of 1.375 V on INxP pin. AVDD is 3.3 V. Sound signals picked up by the microphone create variations over this static DC bias.

The high pass filter is used to remove the static DC level from the digital output. The digital output capture shown below is for a 1-Vrms input riding over a DC bias of 1.375 V.

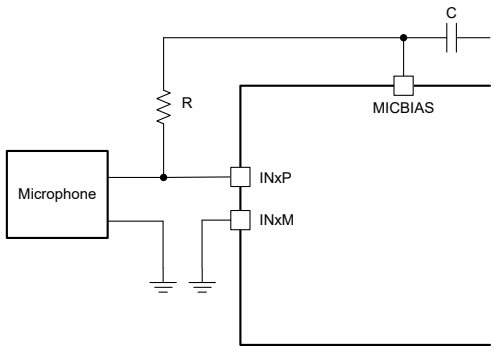

Figure 4-18. Single Ended DC Coupled Microphone Circuit

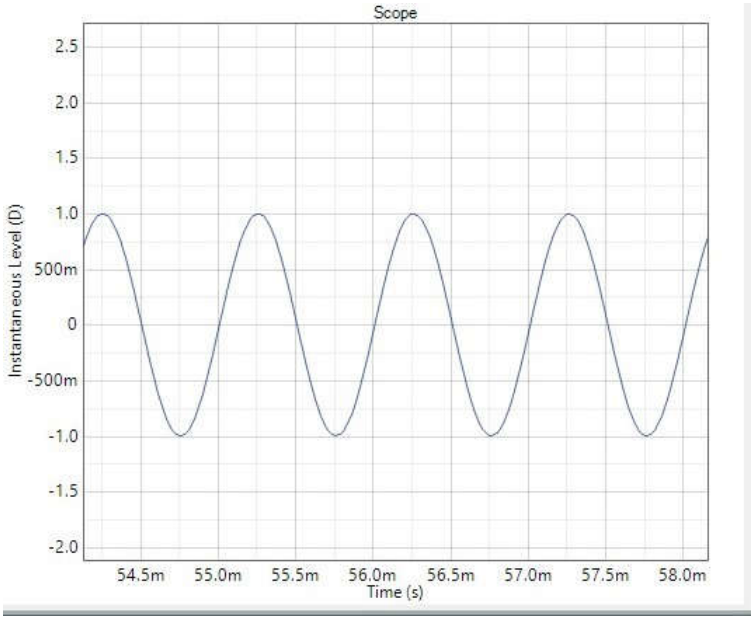

Figure 4-19. Digital Output Capture (Vin = 1 VRMS)

```
Input Timing: 32 bit TDM, FSYNC = 48-kHz, BCLK = 12.288 Mhz.
w 9c 00 00 # Select Page 0
w 9c 01 01 # Reset Device
# 1mS Delay.
w 9c 00 00 # Select Page 0
w 9c 02 81 # Wake up and Enable AREG
w 9c 05 15 # ASI Channel configuration
w 9c 0c 01
w 9c 0d 02
w 9c 0e 03
w 9c 3b 60 # MicBias = 3.3 V
w 9c 3c b4 # Channel 1 configuration
w 9c 41 b4 # Channel 2 configuration
w 9c 74 c0 # input and output Configuration
# High pass filter coefficients
w 9c 49 e6
w 9c 4a 48
w 9c 4b c6
w 9c 4c 80
w 9c 4d 19
w 9c 4e b7
w 9c 4f 3a
w 9c 50 7f
w 9c 51 cc
w 9c 52 91
w 9c 53 8b
w 9c 00 06 # Select page 6
w 9c 1d 04
w 9c 1e b0
w 9c 7e 2d
w 9c 00 00 # Power up/down
w 9c 75 E0
```

Condenser Microphone: Differential DC Coupled Input

The circuit below is of a differential DC-coupled condenser microphone. A mic bias of 3.3 V is setup and biasing resistors R of 1.1 K is used setting up a static DC level of 2.25-V on INxP and 0.75 V on INxM pin. AVDD is 3.3 V. Sound signals picked up by the microphone create variations over these static DC bias levels.

The high pass filter is used to remove the static DC level from the digital output. The digital output capture shown below is for a 1-Vrms differential input.

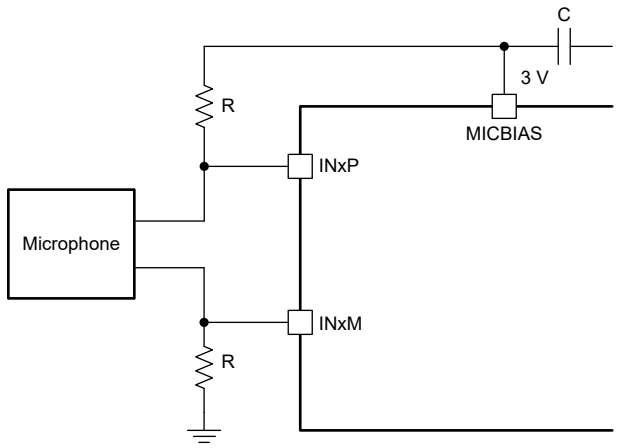

Figure 4-20. Differential DC Coupled Circuit for Condenser Mic

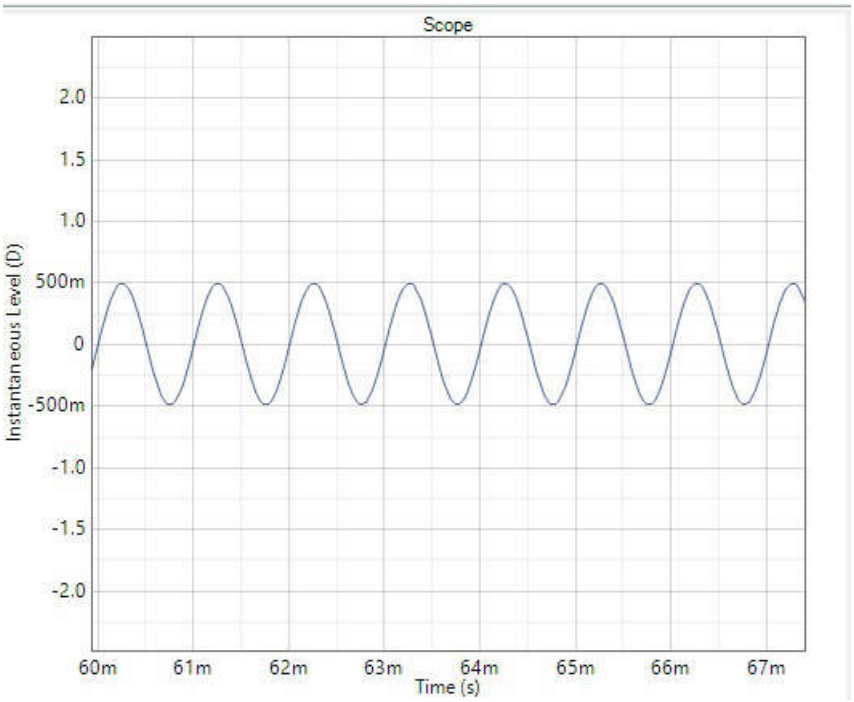

Figure 4-21. Digital Capture (Analog Differential Input of 1 Vrms)

```
Input Timing: 32 bit TDM, FSYNC = 48-kHz, BCLK = 12.288 Mhz.
w 9c 00 00 #Select Page 0
w 9c 01 01 # Reset Device
# 1mS Delay
w 9c 00 00 # Select Page 0
w 9c 02 81 # Wake up and Enable AREG
w 9c 05 15
w 9c 0c 01 # ASI Channel configuration
w 9c 0d 02
w 9c 0e 03
9c 3b 60 # MicBias = 3.3 V
w 9c 3c 90 # Channel 1 configuration
w 9c 41 90 # Channel 2 configuration
w 9c 74 c0 # input and output Configuration
w 9c 00 04 # Select page 4
# High pass filter coefficients
w 9c 49 e6
w 9c 4a 48
w 9c 4b c6
w 9c 4c 80
w 9c 4d 19
w 9c 4e b7
w 9c 4f 3a
w 9c 50 7f
w 9c 51 cc
w 9c 52 91
w 9c 53 8b
w 9c 00 06 # Select page 6
w 9c 1d 04
w 9c 1e b0
w 9c 7e 2d
w 9c 00 00 # Select page 0
w 9c 75 E0
```

5 Summary

Many applications in consumer and industrial markets involve the digitizing of microphone signals. Microphone systems today must detect a range of field sounds from quite and far to loud and near. Such a wide range of field sounds demands a system with a high dynamic range. This application note showcases the functionality of the analog input of the TLV320ADCX120/PCMX120 families while also discussing design considerations for choosing a microphone and associated application circuits to create a high performance microphone front-end.

6 References

- PUI Audio Incorporated, POM-2730L-HD-R data sheet.

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